Application Note

Benefiting from Step-Down Converters with an I²C Communication Interface

Dorian Brillet de Candé

ABSTRACT

This application report shows the benefits of using a step-down converter with an I²C communication interface. Several applications benefit from controlling features and reading status information from a power management device. TI offers step-down converters with an I²C communication interface, which focus on design flexibility while keeping a small solution size.

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Trademarks

1 Introduction

When it comes to power management, many systems benefit from step-down converters with already built-in features. However, adding more features requires more pins to implement them. Offering more features can be at odds with the need to increase the power density. To achieve both, some buck converters use an I^2C interface, which enables digital communication to control such features, read status information or adjust the buck converter control modes depending on the system operating conditions .

2 Step-Down Converter with an I^2C Interface Selection Table

Table 2-1 highlights the latest low input voltage (< 7 V) DC/DC converters with an I^2C communication interface. The devices offer different operating modes and features over a wide range of output current.

Table 2-1. DC/DC Converters Suggestion Using an I^2C Communication Interface

OPN	Current Rating	Switching Frequency (typical)	Features	I^2C Addressable Parameters	IC Size x/y/z	Solution size
TPS62860 TPS62861	0.6A 1A	1.5 MHz 4 MHz	0.35-mm pitch WCSP package, VSEL pin Options,	Output discharge, Software Enable, PSM/FPWM Mode, Voltage Ramp Speeds	0.7x1.4 mm 0.4 mm height	Down to 6 mm^2 possible
TPS62864 TPS62866	4A 6A	2.4MHz	0.35-mm pitch WCSP package, Resistor-selectable start-up voltage, VID pin, /PG pin,	Output discharge, Software Enable, PSM/FPWM Mode, HICCUP Short-Circuit Protection, Voltage Ramp Speeds, Enable FPWM Mode during Output Voltage Change, Thermal Warning	1.05x1.78 mm 0.5 mm height	Down to 22 mm^2 possible
TPS62868 TPS62869	4A 6A	2.4MHz	QFN package, Resistor-selectable start-up voltage, Output voltage range options, VID pin, PG pin,	Output discharge, Software Enable, PSM/FPWM Mode, HICCUP Short-Circuit Protection, Voltage Ramp Speeds, Enable FPWM Mode during Output Voltage Change, Thermal Warning	1.5x2.5 mm 1.0 mm height	Down to 27 mm^2 possible
TPS62870-Q1 TPS62871-Q1 TPS62872-Q1 TPS62873-Q1	6A 9A 12A 15A	1.5MHz/ 2.25MHz/ 2.5MHz/ 3MHz Resistor-selectable	QFN package, Differential remote sensing, Optional stacked operation, Resistor-selectable start-up voltage, PG pin, External compensation, External clock synchronization	Output discharge, Software Enable, PSM/FPWM Mode, HICCUP Short-Circuit Protection, Voltage Ramp Speeds, Spred spectrum Clocking, Output voltage range options, Soft-Start ramp time, Enable FPWM Mode during Output Voltage Change, Thermal Warning, Power-bad Over/Undervoltage	2.55x 3.55 mm 1.0 mm height	NA

3 Smart Routing and Tiny IC Packages

A proper pinout assignment is critical to ensure a simple component placement and a small solution size. It is also important to provide an easy access to all available pins on the package of the device. To integrate an I^2C communication interface, two additional logic pins, SDA and SCL, need to be added. To allow easy routing without expensive microvias, the I^2C pins should be added on the outside of the device.

The TPS62861 combines a flexible design and a small solution size. The TPS62861 is housed in a 8-pin tiny 0.7x1.4mm wafer chip scale package (WCSP). Figure 3-1 shows the PCB layout of the TPS62861 which is optimized for its solution size of 12mm²and has all pins accessible from the outside of the package. No vias are required for connecting to the IC.

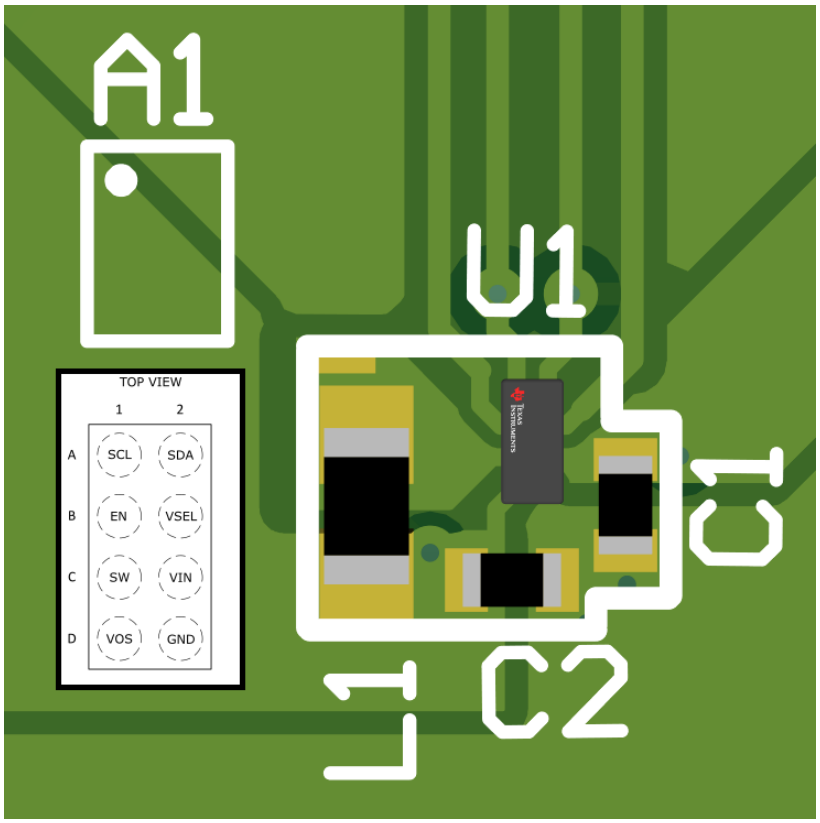

Figure 3-1. TPS62861 Layout Connecting all Pins Without Vias

Layout Matters: Solving Pinout Assignment Issues for DC/DC Converters in WCSP Packages is a technical article describing how a good pinout assignment can help for a small and simple implementation of a DC/DC converter with an I^2C communication interface.

4 Selectable Forced-PWM/PSM operation

Battery-powered applications require step-down converters to provide high efficiency numbers at light loads to save power and ensure a long battery run time. Therefore, many step-down converters implement a Power Save Mode (PSM) operation which automatically reduces the switching frequency when in a light load condition. However, this switching frequency reduction increases the output voltage ripple. The higher output voltage ripple magnitude as well as the lower switching frequency may not be acceptable for some sensitive loads.

An *Enable FPWM Mode* bit is available in the Control Register of TPS62866. Enabling this bit forces PWM mode operation to achieve smallest output voltage ripple. Figure 4-1 shows the TPS62866 efficiency curves difference, while Figure 4-1 shows the output-ripple difference. The 4µA I_Q of TPS62866 enables high light-load efficiency for many portable applications.

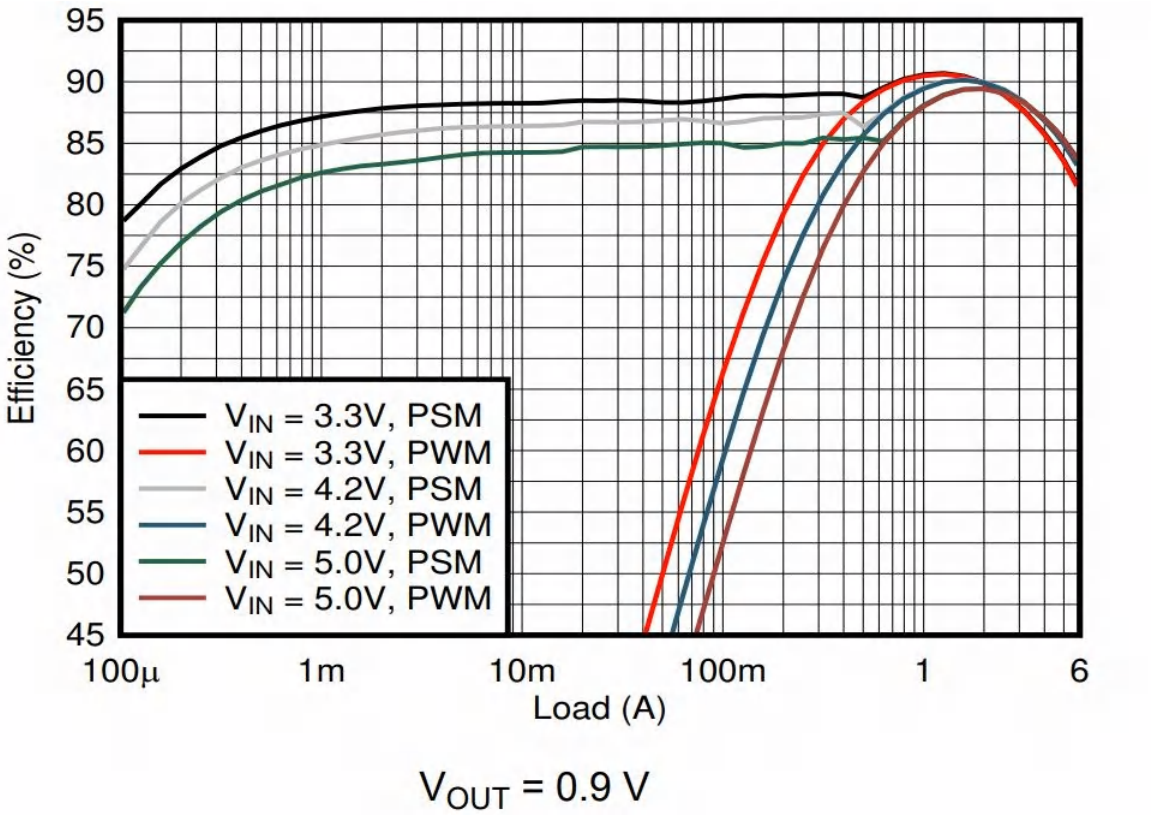

Figure 4-1. TPS62866 Efficiency Versus Load Current with Power Save-Mode and Forced PWM Mode

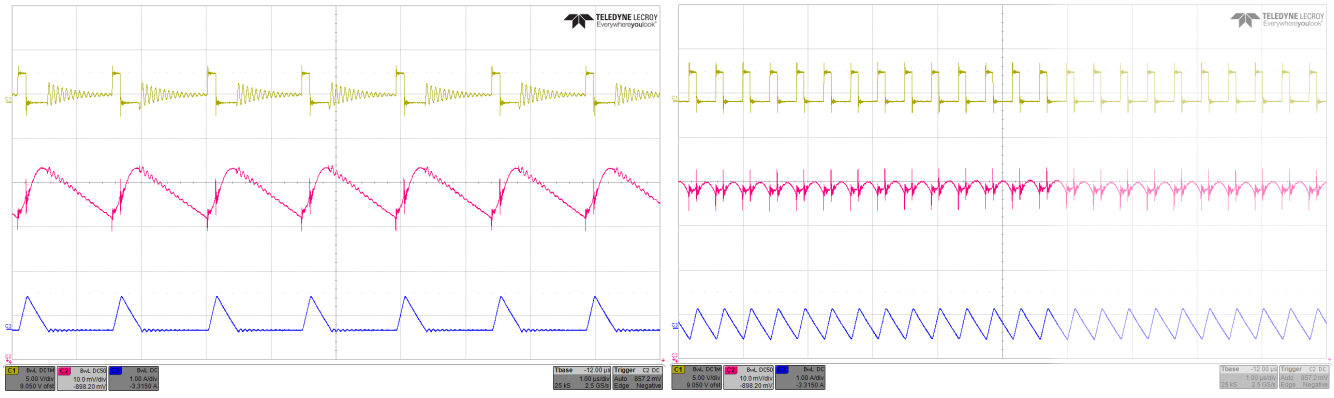

Figure 4-2. TPS62866 Output Voltage Ripple with Power-Save Mode (left) and Forced PWM Mode (right)

Operating Conditions: VIN=3.3V, Vout=0.9V and Iout= 100 mA

5 Dynamic Output Voltage Adjustment During Operation

The I²C interface allows adjustment of the output voltage during operation. One or more I²C registers usually sets the output voltage, and these can be directly re-written during operation. Some devices also contain VID or VSEL pins, which switch between two or more output voltages. In this case, the registers can still be re-written as needed during operation, or can be written once to specific operating voltages.

For example, LPDDR5 DRAMs VDDQ rail can be set to either 0.5 V or 0.3 V. This voltage change is accomplished by either rewriting the I²C register to change the output voltage or using the VID pin to change to a different I²C register with its different output voltage. LPDDR5 DRAMs provide additional power-savings compared to previous generations. In an idle condition when the LPDDR5 DRAM is in a low-power operating state, the memory controller can reduce both the supply voltage and frequency of operation using the dynamic voltage and frequency scaling VDDQ (DVFSQ) feature of the LPDDR5 DRAM.

Figure 5-1 shows a typical block diagram for powering LPDDR5 memory, with dynamic output voltage adjustment on the VDDQ rail.

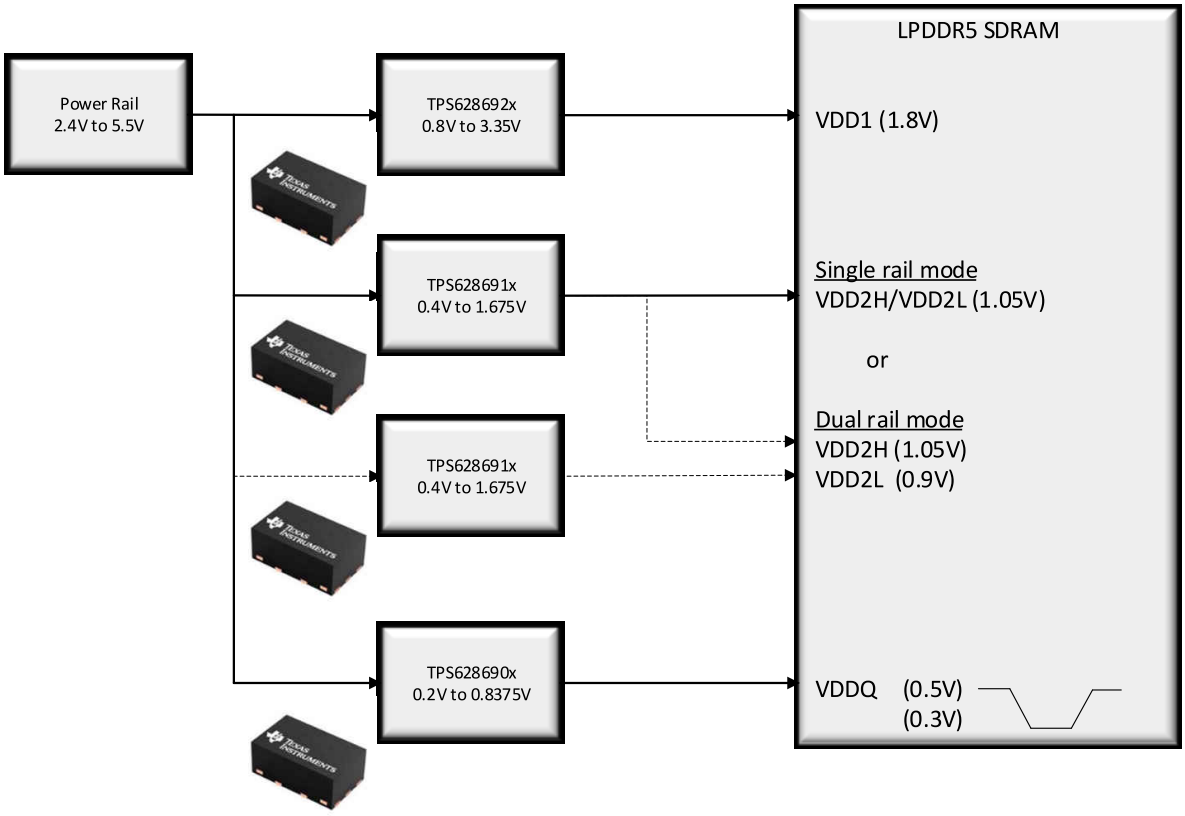

Figure 5-1. The TPS62869 Powers all Rails on LPDDR5 DRAM with Dynamic Output Voltage Adjustment on the VDDQ Rail

The system design determines if dual rail mode will be used for additional power savings. Unlike the VDDQ rail – which can be changed dynamically – VDD2H/L are always operated at fixed voltages, regardless of whether single rail or dual rail mode is used.

TPS62869 provides different voltage ramp speeds to enable system engineers to select the right conditions for a DVFSQ low-to-high transition. For instance, if a fast response is required when VDDQ is returned to a 0.5 V nominal level for high-speed operations, TPS62869 can adapt its Voltage Ramp Speed from 1mV/us up to 20mV/us.

Table 5-1 shows the maximum VDDQ Ramp Rates for a DVFSQ transition.

Table 5-1. VDDQ Ramp Rates for DVFSQ transition

VDDQ Slew Rate	Max Value	Units
Fast response mode (high current)	20	mV/us
Normal operation (default)	4,8	mV/us

Furthermore, operating parameters for example, *Forced PWM mode during output voltage change* can be enabled to address strict timing requirements during the Low-to-High transition of VDDQ. This provides a fast transition in a lower operating state and can prevent the slow discharge of the output stage to limit the voltage ramp speed in a low load condition.

Figure 5-2 shows an example of a 0.5 V to 0.3 V transition with and without Forced PWM mode during output voltage change at a 100 mA load condition.

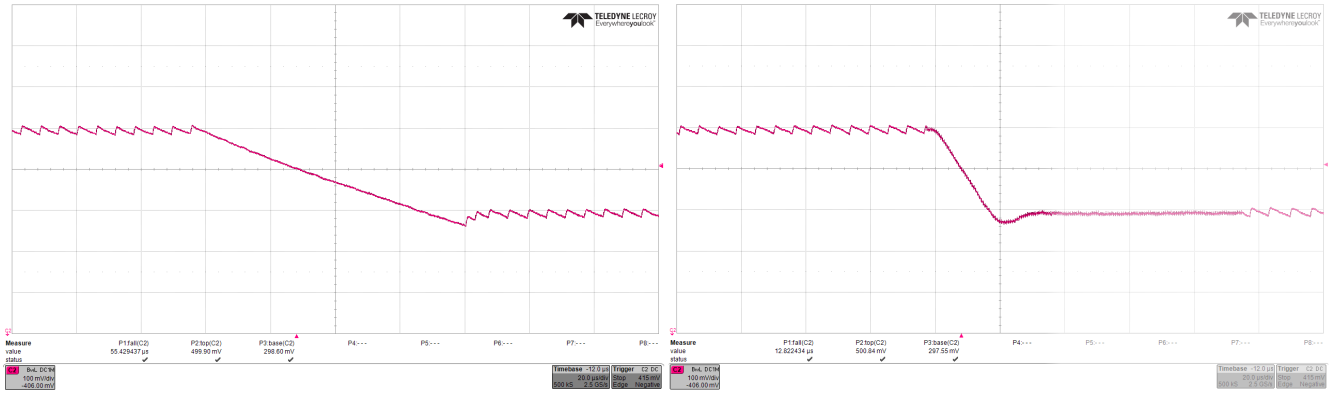

Figure 5-2. 0.5 V to 0.3 V Output Transition in a 20 mV/us Slew Rate, IOUT=100mA Without FPWM During Change Enabled (left) and With (right)

6 Thermal Considerations

In some space-constrained applications, thermal performance of power management devices comes under close scrutiny. Controlling, on-the-fly, the output voltage and operating parameters in order to influence the heat dissipation is a highly valuable feature. Thermal adjustments can be achieved by adapting the output voltage as well as the load current during operation. Placing the memory controller in a lower power operating state enables significant power savings and subsequently reduces the system temperature .

A further benefit of thermal adjustments is to determine thermal margin in a design. Some I^2C devices such as TPS62873-Q1 contain a thermal warning bit, which acts as an upper limit to take preventive measures and keep away from excessive heating or even thermal shutdown. As long as the junction temperature of the device is below the thermal warning threshold, the thermal warning bit is Low in the status register. If the junction temperature exceeds that temperature, the thermal warning bit goes High.

Furthermore, TPS62873-Q1 can operate in stacked mode to spread the power dissipation across multiple spots on the PCB and minimize a single device junction temperature. In a stacked configuration the output current capability is increased. A two TPS62873-Q1 stack is shown in Figure 6-1, this configuration can deliver higher current up to 30 A.

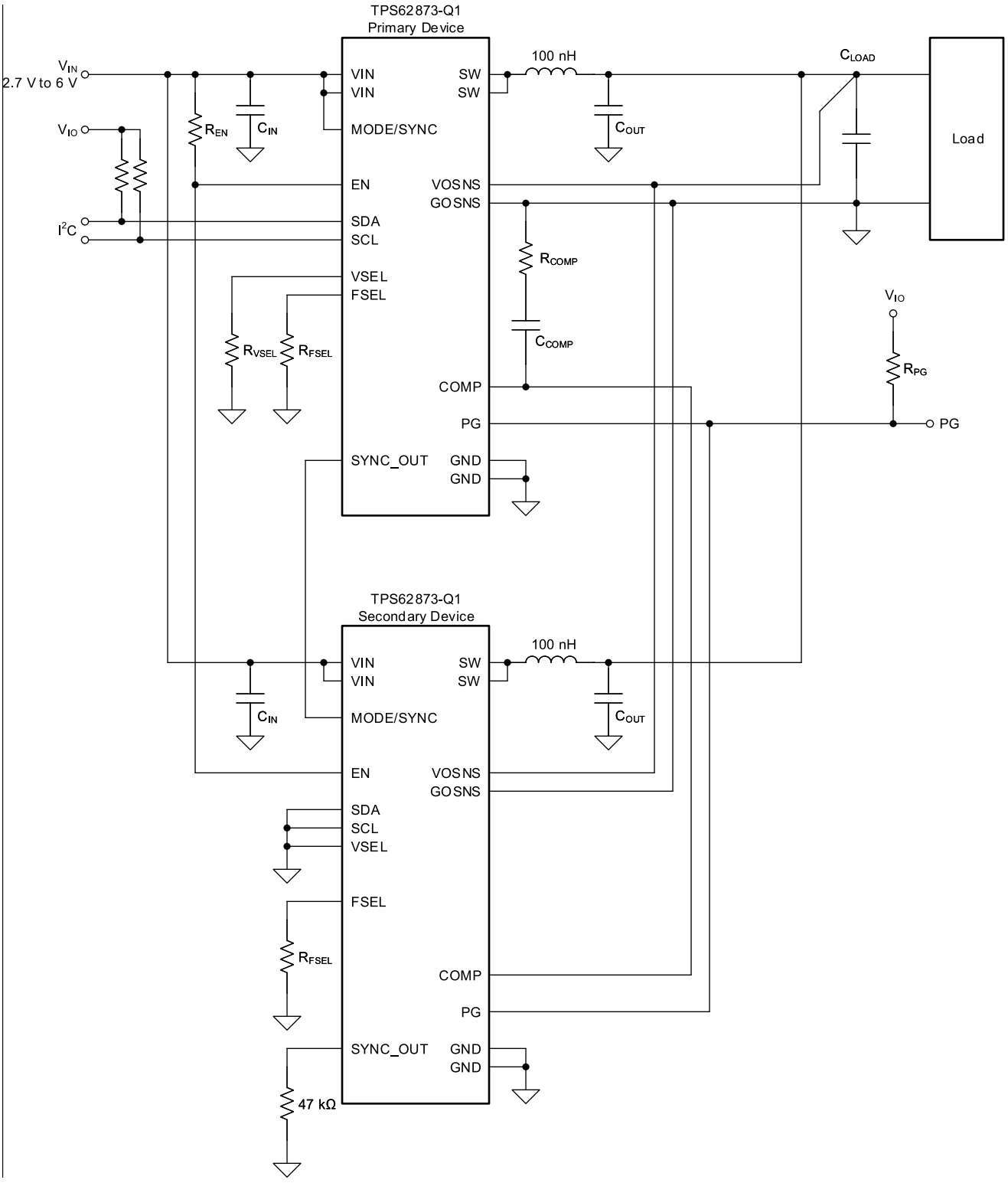

Figure 6-1. Two TPS62873-Q1 Devices in a Stacked Configuration

7 Conclusion

TI offers high performance, simple to layout step-down converters with an I^2C interface, easing trade-off considerations between design flexibility and higher power density. Having more integrated features, through the I^2C interface, reduces the number of external components, lowering the system BOM cost and pin count. A more flexible design can address more rails within a system and therefore lower development efforts by providing a greater pricing advantage due to the economies of scale.

8 References

- Texas Instruments, *Methods of Output-Voltage Adjustment for DC/DC Converters* analog design journal.
- Texas Instruments, *Enabling Higher Data Rates for Optical Modules With Small and Efficient Power and Data-Converter Solutions* technical white paper.
- Texas Instruments, *Thermal Performance Optimization of High Power Density Buck Converters* application report.
- Texas Instruments, *Layout Matters: Solving Pinout Assignment Issues for DC/DC Converters in WCSP Packages*.

9 Revision History

Changes from Revision * (May 2021) to Revision A (April 2022)	Page
• Updated DC/DC Converters Suggestion Using an I^2C Communication Interface table	2

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