TEXAS INSTRUMENTS

TPS630250
TPS630251, TPS630252

SLVSBJ9B – MAY 2014 – REVISED MARCH 2015

TPS63025x High Current, High Efficiency Single Inductor Buck-Boost Converter

1 Features

- Real Buck or Boost Operation with Automatic and Seamless Transition Between Buck and Boost Operation
- 2.3 V to 5.5 V input voltage range
- 2 A Continuous Output Current : V_{IN}≥ 2.5 V, V_{OUT}= 3.3 V
- Adjustable and Fixed Output Voltage
- Efficiency up to 95% in Buck or Boost Mode and up to 97% when V_{IN}=V_{OUT}
- 2.5MHz Typical Switching Frequency
- 35-µA Operating Quiescent Current
- Integrated Soft Start
- Power Save Mode
- True Shutdown Function
- Output Capacitor Discharge Function
- Over-Temperature Protection and Over-Current Protection
- Wide Capacitance Selection
- Small 1.766 mm x 2.086 mm, 20-pin WCSP and 2.5 mm x 3 mm, 14-pin Hot Rod

2 Applications

- Cellular Phones, Smart Phones
- Tablets PC
- PC and Smart Phone accessories
- Point of load regulation
- Battery Powered Applications

3 Description

The TPS63025x are high efficiency, low quiescent current buck-boost converters suitable for application where the input voltage is higher or lower than the output. Output currents can go as high as 2 A in boost mode and as high as 4 A in buck mode. The maximum average current in the switches is limited to a typical value of 4 A. The TPS63025x regulates the output voltage over the complete input voltage range by automatically switching between buck or boost mode depending on the input voltage ensuring a seamless transition between modes. The buck-boost converter is based on a fixed frequency, pulse-width-modulation (PWM) controller using synchronous rectification to obtain highest efficiency. At low load currents, the converter enters Power Save Mode to maintain high efficiency over the complete load current range. There is a PFM/PWM pin that allows the user to choose between automatic PFM/PWM mode operation and forced PWM operation. During PWM mode a fixed-frequency of typically 2.5 MHz is used. The output voltage is programmable using an external resistor divider, or is fixed internally on the chip. The converter can be disabled to minimize battery drain. During shutdown, the load is disconnected from the battery. The device is packaged in a 20-pin WCSP package measuring 1.766 mm x 2.086mm and 14-pin HotRod package measuring 2.5 mm x 3mm.

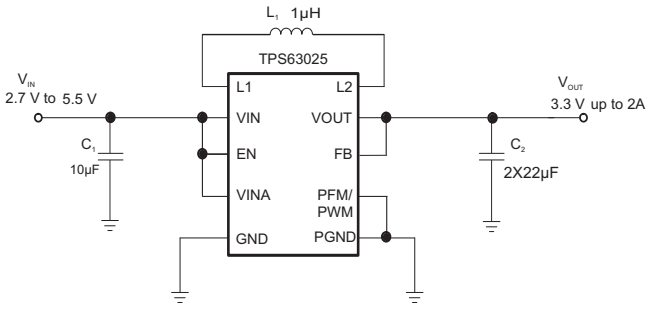
Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS63025x	DSBGA (20)	1.766 mm × 2.086 mm
	VQFN (14)[(2)]	2.5 mm x 3 mm

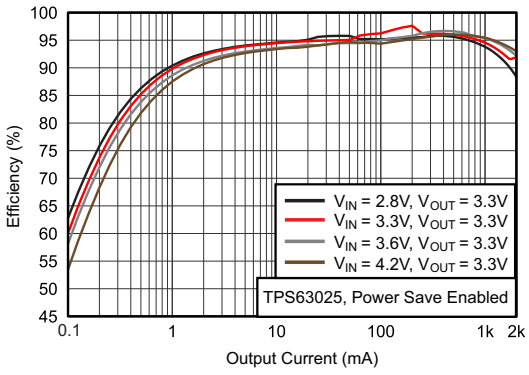
(1) For all available packages, see the orderable addendum at the end of the datasheet.

(2) Product Preview

4 Typical Application



Efficiency vs Output Current



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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2014) to Revision B — **Page**

- Added VQFN (RNC) package option ... 3
- Changed UVLO in the *Electrical Characteristics* From: MAX = 1.9 V To: 2 V ... 5

Changes from Original (May 2014) to Revision A — **Page**

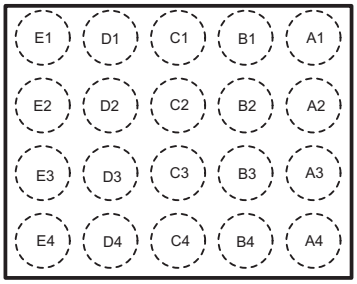
- Added devices TPS630250, TPS630251, and TPS630252 voltage options ... 1
- Added Specifications, Detailed Description section, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section; and, changed status to Production Data. ... 4
- Changed Load Regulation Typ spec from "125 mV/A" to "2.5 mV/A" ... 6

6 Device Comparison Table

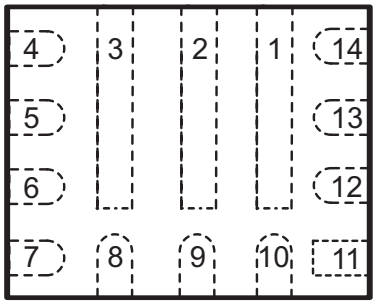
PART NUMBER	VOUT
TPS630250	Adjustable
TPS630251	2.9 V
TPS630252	3.3 V

7 Pin Configuration and Functions

DSBGA 20-Pin
YFF Package
Top View



VQFN 14-Pin
RNC Package
Top View



Product Preview

Pin Functions

PIN			I/O	DESCRIPTION
NAME	DSBGA	RNC		
VOUT	A1,A2,A3	12, 13, 14	PWR	Buck-Boost converter output
FB	A4	11	IN	Voltage feedback of adjustable version, must be connected to VOUT on fixed output voltage versions
L2	B1,B2,B3	1	PWR	Connection for Inductor
PFM/PWM	B4	10	IN	set low for PFM mode, set high for forced PWM mode. It must not be left floating
PGND	C1,C2,C3	2	PWR	Power Ground
GND	C4	9	PWR	Analog Ground
L1	D1,D2,D3	3	PWR	Connection for Inductor
EN	D4	8	IN	Enable input. Set high to enable and low to disable. It must not be left floating.
VIN	E1,E2,E3	4, 5, 6	PWR	Supply voltage for power stage
VINA	E4	7	PWR	Supply voltage for control stage.

8 Specifications

8.1 Absolute Maximum Ratings(1)

over junction temperature range (unless otherwise noted)

		VALUE		
		MIN	MAX	UNIT
Voltage(2)	VIN, L1, EN, VINA, PFM/PWM	–0.3	7	V
	VOUT, FB	–0.3	4	V
	L2(3)	–0.3	4	V
	L2(4)	-0.3	5.5	V
Input current	Continuos average current into L1(5)		2.7	A
T_J	Operating junction temperature	–40	125	°C
T_{stg}	Storage temperature range	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.
(3) DC voltage rating.
(4) AC voltage rating.
(5) Maximum continuos average input current 3.5A, under those condition do not exceed 105°C for more than 25% operating time.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±700	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions(1)

		MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range	2.3		5.5	V
V_{OUT}	Output Voltage	2.5		3.6	V
L	Inductance (2)	0.5	1	1.3	µH
C_{out}	Output Capacitance(3)	20			µF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating virtual junction temperature	–40		125	°C

(1) Refer to the Application Information section for further information
(2) Effective inductance value at operating condition. The nominal value given matches a typical inductor to be chosen to meet the inductance required.
(3) Due to the dc bias effect of ceramic capacitors, the effective capacitance is lower then the nominal value when a voltage is applied. This is why the capacitance is specified to allow the selection of the nominal capacitor required with the dc bias effect for this type of capacitor. The nominal value given matches a typical capacitor to be chosen to meet the minimum capacitance required.

8.4 Thermal Information

THERMAL METRIC[1]		TPS63025x		UNIT
		YFF (DSBGA)	RNC (VQFN)[2]	
		20 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	71.1	69.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.5	38.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	11.4	12.7	
ψ_{JT}	Junction-to-top characterization parameter	2	1.9	
ψ_{JB}	Junction-to-board characterization parameter	11.3	12.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Product Preview

8.5 Electrical Characteristics

V_{IN}= 2.3V to 5.5V, T_J= –40°C to 125°C, typical values are at T_A= 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY							
V_{IN}	Input voltage range			2.3		5.5	V
V_{IN_Min}	Minimum input voltage to turn on into full load		I_{OUT} = 2A		2.8		V
I_{OUT}	Continuos Output Current (1)		V_{IN} >=2.5V, V_{OUT}=3.3V		2		A
I_Q	Quiescent current	V_{IN}	I_{OUT} = 0mA, EN = V_{IN} = 3.6V, V_{OUT} = 3.3V T_J = -40°C to 85°C, not switching		35	70	µA
		V_{OUT}				12	µA
I_{sd}	Shutdown current		EN = low, T_J = -40°C to 85°C		0.1	2	µA
UVLO	Under voltage lockout threshold		V_{IN} falling	1.6	1.7	2	V
	Under voltage lockout hysteresis				180		mV
	Thermal shutdown		Temperature rising		140		°C
	Thermal Shutdown hysteresis				20		°C
LOGIC SIGNALS EN, PFM/PWM							
V_{IH}	High level input voltage		V_{IN} = 2.3V to 5.5V	1.2			V
V_{IL}	Low level input voltage		V_{IN} = 2.3V to 5.5V			0.4	V
I_{lkg}	Input leakage current		EN = GND or V_{IN}		0.01	0.2	µA
OUTPUT							
V_{OUT}	Output Voltage range			2.3		3.6	V
V_{FB}	Feedback regulation voltage				0.8		V
V_{FB}	Feedback voltage accuracy		PWM mode, TPS630250	-1%		1%	
V_{FB}	Feedback voltage accuracy (2)		PFM mode, TPS630250	-1%	1.3%	+3%	
V_{OUT}	Output voltage accuracy		PWM mode, TPS630251	2.871	2.9	2.929	V
V_{OUT}	Output voltage accuracy(2)		PFM mode, TPS630251	2.871	2.938	2.987	V
V_{OUT}	Output voltage accuracy		PWM mode, TPS630252	3.267	3.3	3.333	V
V_{OUT}	Output voltage accuracy(2)		PFM mode, TPS630252	3.267	3.343	3.399	V
$I_{PWM/PFM}$	Output current to enter PFM mode		V_{IN} = 3V; V_{OUT} = 3.3V		350		mA
I_{FB}	Feedback input bias current		V_{FB} = 0.8V		10	100	nA
$R_{DS\_Buck(on)}$	High side FET on-resistance		V_{IN} = 3.0V, V_{OUT} = 3.3V		35		mΩ
	Low side FET on-resistance		V_{IN} = 3.0V, V_{OUT} = 3.3V		50		mΩ
$R_{DS\_Boost(on)}$	High side FET on-resistance		V_{IN} = 3.0V, V_{OUT} = 3.3V		25		mΩ
	Low side FET on-resistance		V_{IN} = 3.0V, V_{OUT} = 3.3V		50		mΩ

(1) For minimum output current in a specific working point see Figure 5 and Equation 1 trough Equation 4.
(2) Conditions: L = 1 µH, C_{OUT} = 2 × 22 µF.

Electrical Characteristics (continued)

V_{IN}= 2.3V to 5.5V, T_J= –40°C to 125°C, typical values are at T_A= 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IN}	Average input current limit (3)	V_{IN} = 3.0V, V_{OUT} = 3.3V T_J = 65°C to 125°C	3.5	4.5	5	A
f_s	Switching Frequency			2.5		MHz
R_{ON_DISC}	Discharge ON-Resistance	EN = low		120		Ω
	Line regulation	V_{IN} = 2.8V to 5.5V, I_{OUT} = 2A		7.4		mV/V
	Load regulation	V_{IN}= 3.6V, I_{OUT} = 0A to 2A		5		mV/A

(3) For variation of this parameter with Input voltage and temperature see Figure 5.

8.6 Timing Requirements

V_{IN}= 2.3 V to 5.5 V, T_J= –40°C to 125°C, typical values are at T_A= 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
t_{SS}	Soft-start time	V_{OUT}=EN=low to high, Buck mode V_{IN}=3.6V, V_{OUT}=3.3V, I_{OUT}=2A		450		µs
		V_{OUT}=EN=low to high, Boost mode V_{IN}=2.8V, V_{OUT}=3.3V, I_{OUT}=2A		700		µs
t_d	Start up delay	Time from when EN=high to when device starts switching		100		µs

8.7 Typical Characteristics

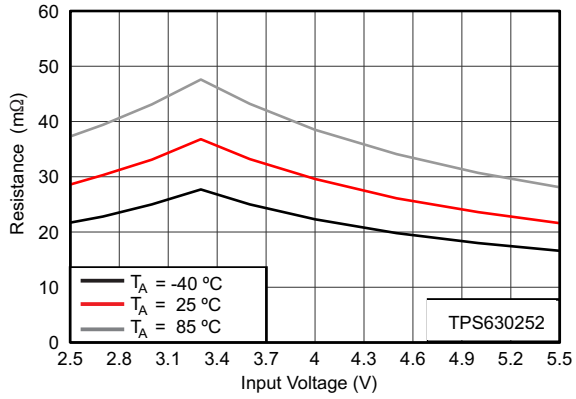


Figure 1. High Side FET On-Resistance vs Input Voltage

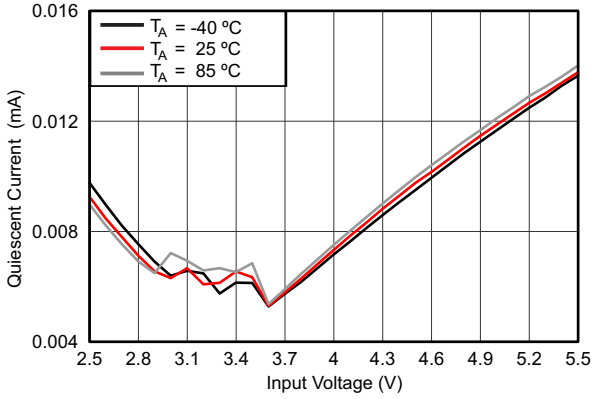


Figure 2. Quiescent Current vs Input Voltage

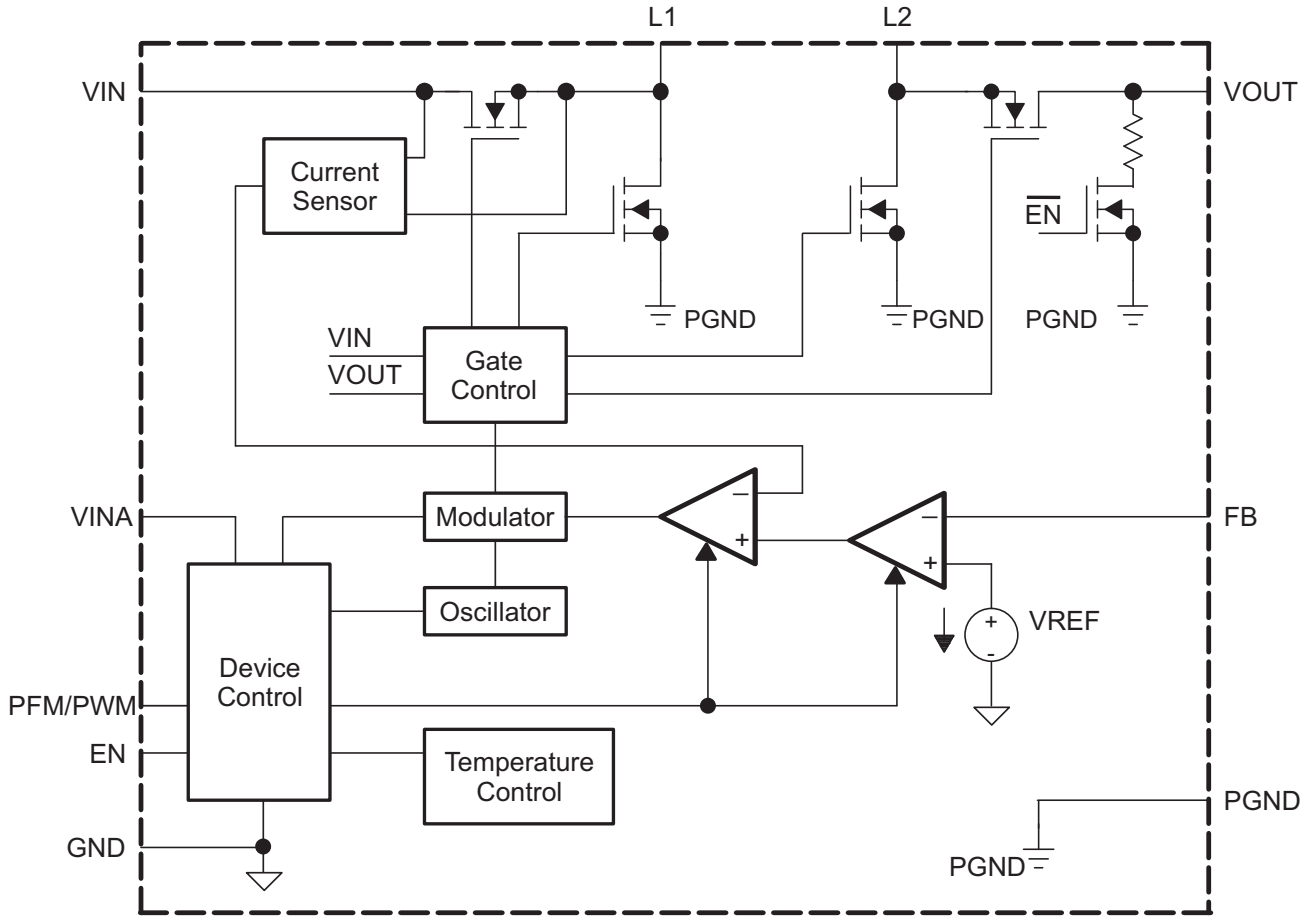
9 Detailed Description

9.1 Overview

The TPS63025x use 4 internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over the complete input voltage and output power range. To regulate the output voltage at all possible input voltage conditions, the device automatically switches from buck operation to boost operation and back as required by the configuration. It always uses one active switch, one rectifying switch, one switch is held on, and one switch held off. Therefore, it operates as a buck converter when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. There is no mode of operation in which all 4 switches are switching at the same time. Keeping one switch on and one switch off eliminates their switching losses. The RMS current through the switches and the inductor is kept at a minimum, to minimize switching and conduction losses. Controlling the switches this way allows the converter to always keep higher efficiency.

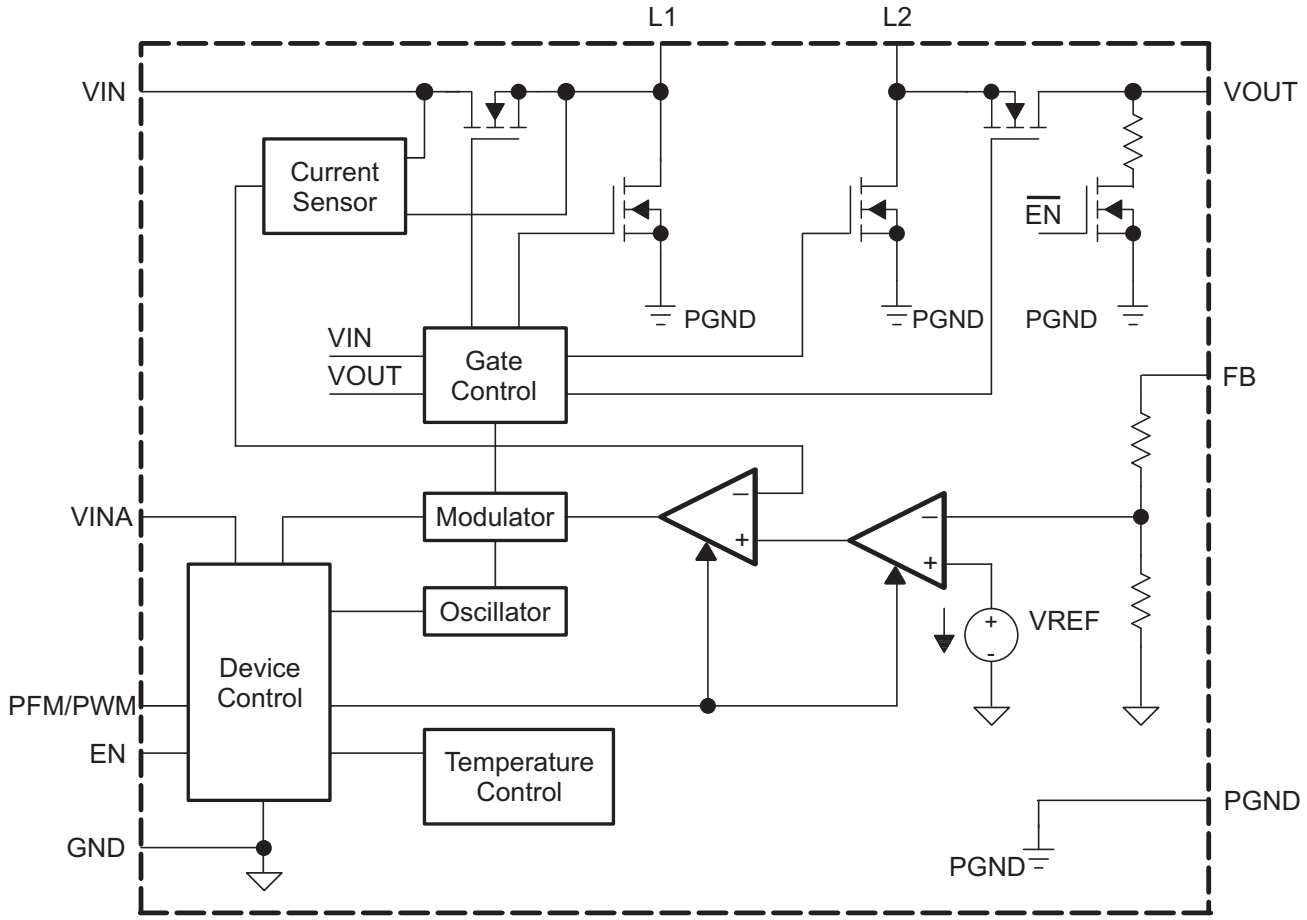
The device provides a seamless transition from buck to boost or from boost to buck operation.

9.2 Functional Block Diagram



Functional Block Diagram (Adjustable Output Voltage)

Functional Block Diagram (continued)



Functional Block Diagram (Fixed Output Voltage)

9.3 Feature Description

9.3.1 Undervoltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages, an undervoltage lockout is included. UVLO shuts down the device at input voltages lower than typically 1.7 V with a 180 mV hysteresis.

9.3.2 Output Discharge Function

When the device is disabled by pulling enable low and the supply voltage is still applied, the internal transistor use to discharge the output capacitor is turned on, and the output capacitor is discharged until UVLO is reached. This means, if there is no supply voltage applied the output discharge function is also disabled. The transistor which is responsible of the discharge function, when turned on, operates like an equivalent 120-Ω resistor, ensuring typically less than 10ms discharge time for 20-µF output capacitance and a 3.3 V output.

9.3.3 Thermal Shutdown

The device goes into thermal shutdown once the junction temperature exceeds typically 140°C with a 20°C hysteresis.

Feature Description (continued)

9.3.4 Softstart

To minimize inrush current and output voltage overshoot during start up, the device has a Softstart. At turn on, the input current raises monotonic until the output voltage reaches regulation. During Softstart, the input current follows the current ramp charging the internal Softstart capacitor. The device smoothly ramps up the input current bringing the output voltage to its regulated value even if a large capacitor is connected at the output.

The Softstart time is measured as the time from when the EN pin is asserted to when the output voltage has reached 90% of its nominal value. There is typically a 100µs delay time from when the EN pin is asserted to when the device starts the switching activity. The Softstart time depends on the load current, the input voltage, and the output capacitor. The Softstart time in boost mode is longer then the time in buck mode. The total typical Softstart time is 1ms.

The inductor current is able to increase and always assure a soft start unless a real short circuit is applied at the output.

9.3.5 Short Circuit Protection

The TPS63025x provides short circuit protection to protect itself and the application. When the output voltage does not increase above 1.2V, the device assumes a short circuit at the output and limits the input current to 4 A.

9.4 Device Functional Modes

9.4.1 Control Loop Description

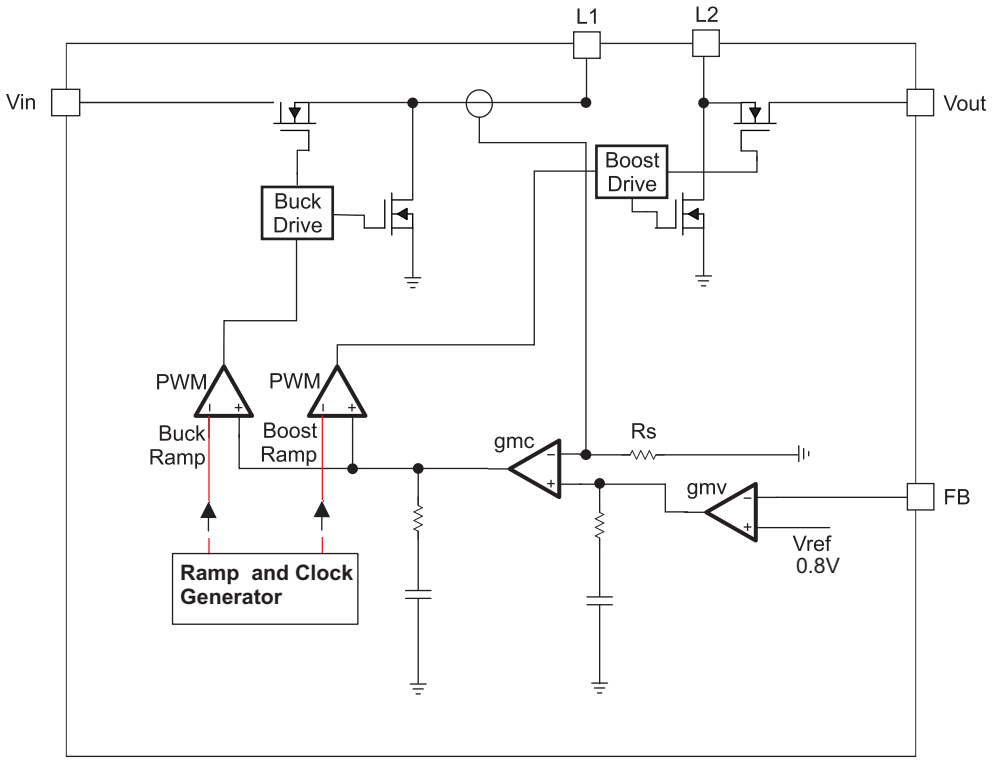


Figure 3. Average Current Mode Control

The controller circuit of the device is based on an average current mode topology. The average inductor current is regulated by a fast current regulator loop which is controlled by a voltage control loop. *Figure 3* shows the control loop.

The non inverting input of the transconductance amplifier, gmv, is assumed to be constant. The output of gmv defines the average inductor current. The inductor current is reconstructed by measuring the current through the high side buck MOSFET. This current corresponds exactly to the inductor current in boost mode. In buck mode the current is measured during the on time of the same MOSFET. During the off time, the current is reconstructed internally starting from the peak value at the end of the on time cycle. The average current and the feedback from the error amplifier gmv forms the correction signal gmc. This correction signal is compared to the buck and the boost sawtooth ramp giving the PWM signal. Depending on which of the two ramps the gmc output crosses either the Buck or the Boost stage is initiated. When the input voltage is close to the output voltage, one buck cycle is always followed by a boost cycle. In this condition, no more than three cycles in a row of the same mode are allowed. This control method in the buck-boost region ensures a robust control and the highest efficiency.

Device Functional Modes (continued)

9.4.2 Power Save Mode Operation

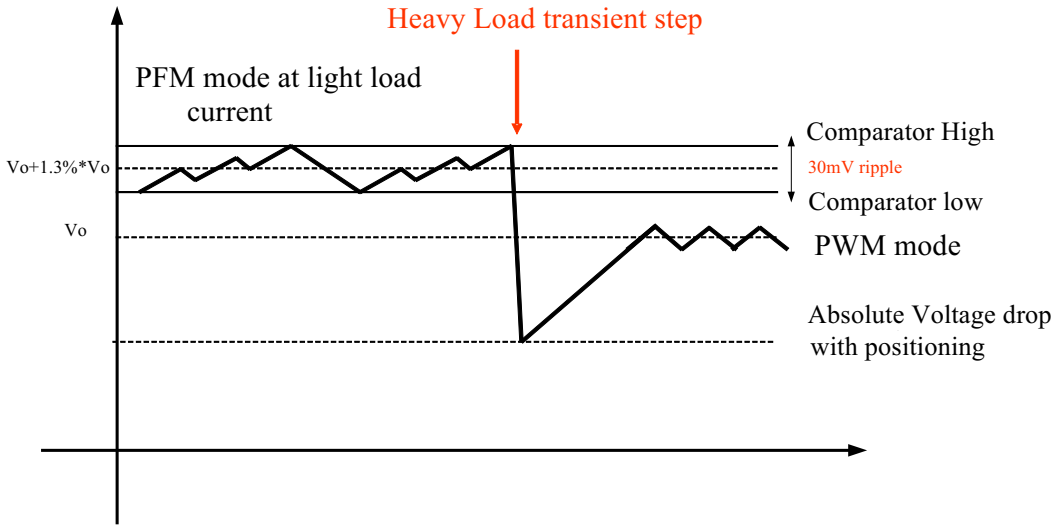


Figure 4. Power Save Mode Operation

Depending on the load current, in order to provide the best efficiency over the complete load range, the device works in PWM mode at load currents of approximately 350mA or higher. At lighter loads, the device switches automatically into Power Save Mode to reduce power consumption and extend battery life. The PFM/PWM pin is used to select between the two different operation modes. To enable Power Save Mode, the PFM/PWM pin must be set low.

During Power Save Mode, the part operates with a reduced switching frequency and lowest supply current to maintain high efficiency. The output voltage is monitored with a comparator at every clock cycle by the thresholds comp low and comp high. When the device enters Power Save Mode, the converter stops operating and the output voltage drops. The slope of the output voltage depends on the load and the output capacitance. When the output voltage reaches the comp low threshold, at the next clock cycle the device ramps up the output voltage again, by starting operation. Operation can last for one or several pulses until the comp high threshold is reached. At the next clock cycle, if the load is still lower than about 350mA, the device switches off again and the same operation is repeated. Instead, if at the next clock cycle, the load is above 350mA, the device automatically switches to PWM mode.

In order to keep high efficiency in PFM mode, there is only one comparator active to keep the output voltage regulated. The AC ripple in this condition is increased, compared to the PWM mode. The amplitude of this voltage ripple in the worst case scenario is 50mV pk-pk, (typically 30 mV pk-pk), with 2-µF effective output capacitance. In order to avoid a critical voltage drop when switching from 0A to full load, the output voltage in PFM mode is typically 1.3% above the nominal value in PWM mode. This is called Dynamic Voltage Positioning and allows the converter to operate with a small output capacitor and still have a low absolute voltage drop during heavy load transients.

Power Save Mode is disabled by setting the PFM/PWM pin high.

Device Functional Modes (continued)

9.4.3 Current Limit

The current limit variation depends on the difference between the input and output voltage. The maximum current limit value is at the highest difference.

Given the curves provided in *Figure 5*, it is possible to calculate the output current reached in boost mode, using *Equation 1* and *Equation 2* and in buck mode using *Equation 3* and Equation 4.

Duty Cycle Boost $$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (1)$$

Output Current Boost $$I_{OUT} = \eta \times I_{IN} (1-D) \quad (2)$$

Duty Cycle Buck $$D = \frac{V_{OUT}}{V_{IN}} \quad (3)$$

Output Current Buck $$I_{OUT} = (\eta \times I_{IN}) / D \quad (4)$$

With,

η = Estimated converter efficiency (use the number from the efficiency curves or 0.90 as an assumption)
I_{IN}= Minimum average input current (Figure 5)

9.4.4 Supply and Ground

The TPS63025x provides two input pins (VIN and VINA) and two ground pins (PGND and GND).

The VIN pin supplies the input power, while the VINA pin provides voltage for the control circuits. A similar approach is used for the ground pins. GND and PGND are used to avoid ground shift problems due to the high currents in the switches. The reference for all control functions is the GND pin. The power switches are connected to PGND. Both grounds must be connected on the PCB at only one point, ideally, close to the GND pin.

9.4.5 Device Enable

The device starts operation when the EN pin is set high. The device enters shutdown mode when the EN pin is set low. In shutdown mode, the regulator stops switching, all internal control circuitry is switched off, and the load is disconnected from the input.

10 Application and Implementation

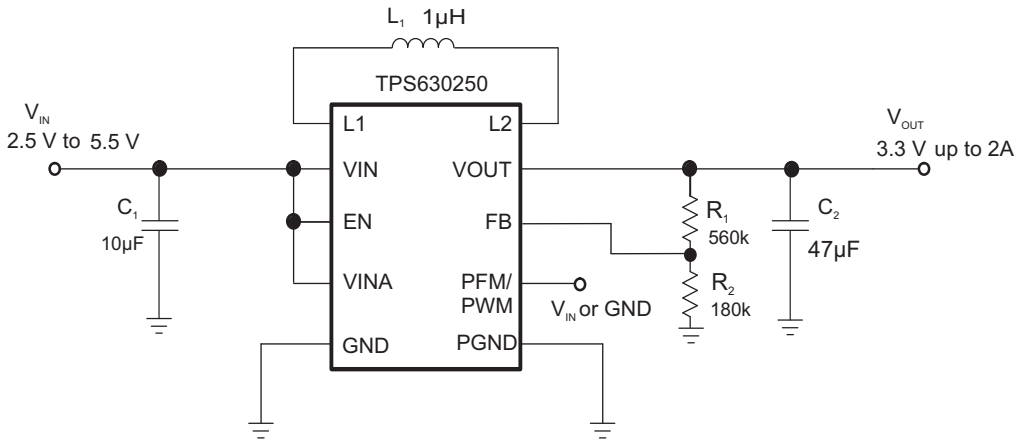
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS63025x are high efficiency, low quiescent current buck-boost converters suitable for application where the input voltage is higher, lower or equal to the output. Output currents can go as high as 2A in boost mode and as high as 4A in buck mode. The maximum average current in the switches is limited to a typical value of 4 A.

10.2 Typical Application



3.3V Adjustable Version

10.2.1 Design Requirements

The design guideline provides a component selection to operate the device within the recommended operating conditions.

Table 1 shows the list of components for the Application Characteristic Curves.

Table 1. Components for Application Characteristic Curves(1)

REFERENCE	DESCRIPTION	MANUFACTURER
	TPS630250	Texas Instruments
L1	1 µH, 8.75A, 13mΩ, SMD	XAL4020-102MEB, Coilcraft
C1	10 µF 6.3V, 0603, X5R ceramic	Standard
C2	47 µF 6.3V, 0603, X5R ceramic	Standard
R1	560kΩ	Standard
R2	180kΩ	Standard

(1) See *Third-Party Products Discalimer*

10.2.2 Detailed Design Procedure

The first step is the selection of the output filter components. To simplify this process Table 2 outlines possible inductor and capacitor value combinations.

10.2.2.1 Output Filter Design

Table 2. Matrix of Output Capacitor and Inductor Combinations

NOMINAL INDUCTOR VALUE [µH](1)	NOMINAL OUTPUT CAPACITOR VALUE [µF](2)				
	44	47	66	88	100
0.680	+	+	+	+	+
1.0	+(3)	+	+	+	+
1.5			+	+	+

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by 20% and –30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by 20% and –50%.
(3) Typical application. Other check mark indicates recommended filter combinations

10.2.2.2 Inductor Selection

The inductor selection is affected by several parameter like inductor ripple current, output voltage ripple, transition point into Power Save Mode, and efficiency. See Table 3 for typical inductors.

Table 3. List of Recommended Inductors(1)

INDUCTOR VALUE	COMPONENT SUPPLIER	SIZE (LxWxH mm)	Isat/DCR
1 µH	Coilcraft XAL4020-102ME	4 X 4 X 2.10	4.5A/10mΩ
1 µH	Toko, DFE322512C	3.2 X 2.5 X 1.2	4.7A/34mΩ
1 µH	TDK, SPM4012	4.4 X 4.1 X 1.2	4.1A/38mΩ
1 µH	Wuerth, 74438334010	3 X 3 X 1.2	6.6A/42.10mΩ
0.6 µH	Coilcraft XFL4012-601ME	4 X 4 X 1.2	5A/17.40mΩ
0.68µH	Wuerth,744383340068	3 X 3 X 1.2	7.7A/36mΩ

(1) See *Third-Party Products Desclaimer*

For high efficiencies, the inductor should have a low dc resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a high impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, the peak current for the inductor in steady state operation is calculated using Equation 6. Only the equation which defines the switch current in boost mode is shown, because this provides the highest value of current and represents the critical current value for selecting the right inductor.

$$\text{Duty Cycle Boost} \qquad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{5}$$

$$I_{PEAK} = \frac{Iout}{\eta \times (1 - D)} + \frac{Vin \times D}{2 \times f \times L} \tag{6}$$

Where,

D =Duty Cycle in Boost mode
f = Converter switching frequency (typical 2.5MHz)
L = Inductor value
η = Estimated converter efficiency (use the number from the efficiency curves or 0.90 as an assumption)
Note: The calculation must be done for the minimum input voltage which is possible to have in boost mode

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. It's recommended to choose an inductor with a saturation current 20% higher than the value calculated using *Equation 6*. Possible inductors are listed in *Table 3*.

10.2.2.3 Capacitor Selection

10.2.2.3.1 Input Capacitor

At least a 10µF input capacitor is recommended to improve line transient behavior of the regulator and EMI behavior of the total power supply circuit. An X5R or X7R ceramic capacitor placed as close as possible to the VIN and PGND pins of the IC is recommended. This capacitance can be increased without limit. If the input supply is located more than a few inches from the TPS63025x converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

10.2.2.3.2 Output Capacitor

For the output capacitor, use of a small ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC is recommended. The recommended nominal output capacitance value is 20 µF with a variance as outlined in *Table 2*.

There is also no upper limit for the output capacitance value. Larger capacitors causes lower output voltage ripple as well as lower output voltage drop during load transients.

10.2.2.4 Setting The Output Voltage

When the adjustable output voltage version TPS63025x is used, the output voltage is set by an external resistor divider. The resistor divider must be connected between VOUT, FB and GND. When the output voltage is regulated properly, the typical value of the voltage at the FB pin is 800 mV. The current through the resistive divider should be about 10 times greater than the current into the FB pin. The typical current into the FB pin is 0.1 µA, and the voltage across the resistor between FB and GND, R_2, is typically 800 mV. Based on these two values, the recommended value for R2 should be lower than 180 kΩ, in order to set the divider current at 4µA or higher. It is recommended to keep the value for this resistor in the range of 180kΩ. From that, the value of the resistor connected between VOUT and FB, R1, depending on the needed output voltage (V_{OUT}), can be calculated using *Equation 7*:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (7)$$

10.2.3 Application Curves

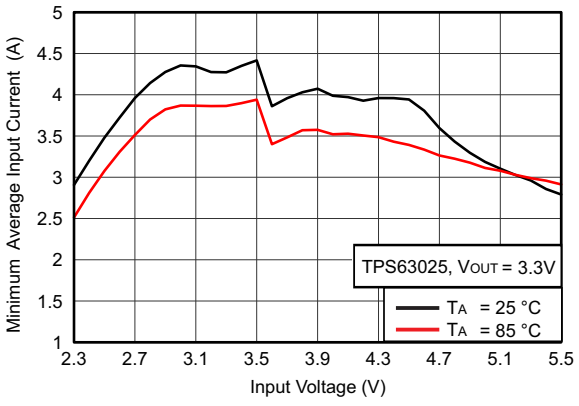


Figure 5. Minimum Average Input Current vs Input Voltage

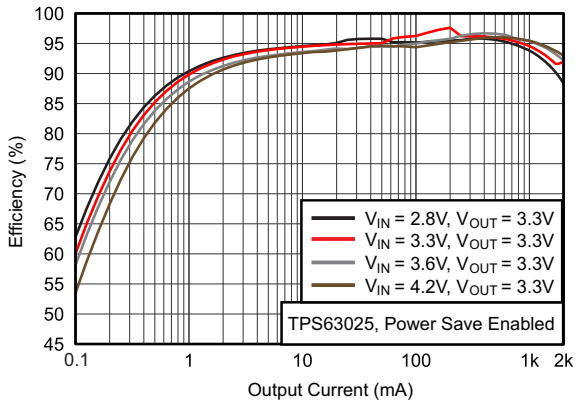


Figure 6. Efficiency vs Output Current

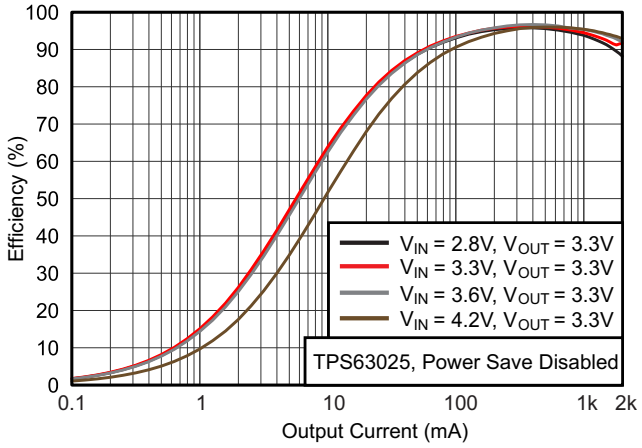


Figure 7. Efficiency vs Output Current

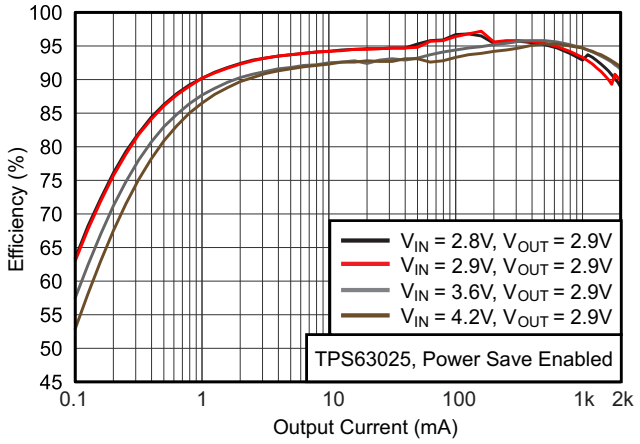


Figure 8. Efficiency vs Output Current

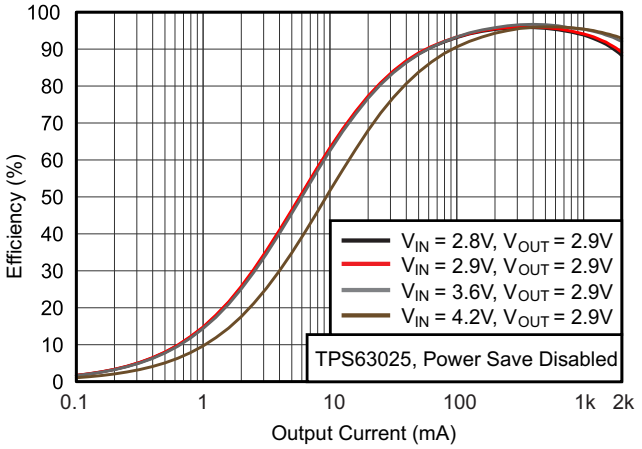


Figure 9. Efficiency vs Output Current

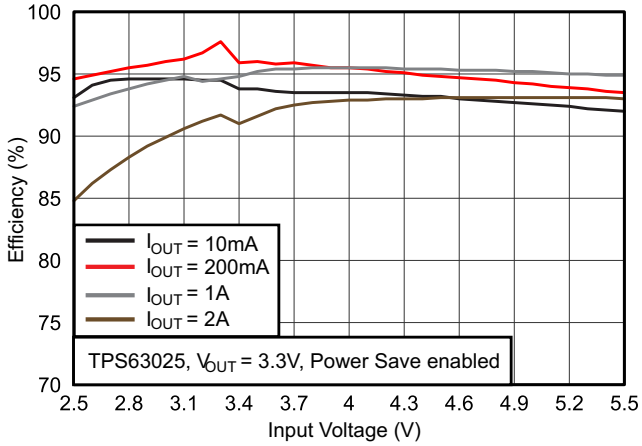


Figure 10. Efficiency vs Input Voltage

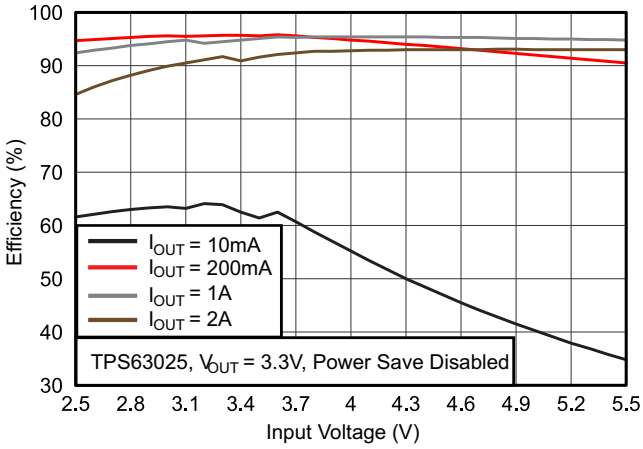


Figure 11. Efficiency vs Input Voltage

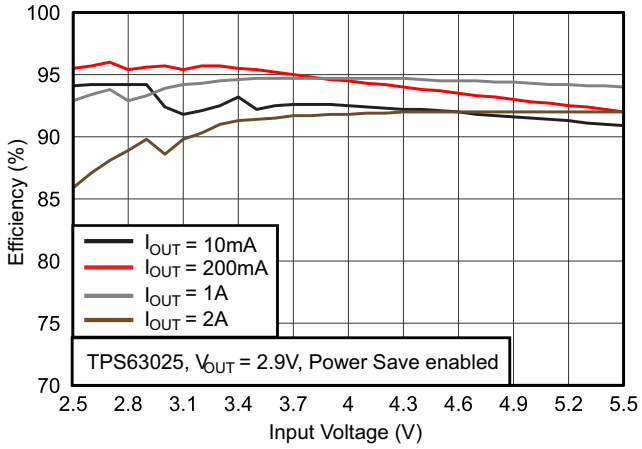


Figure 12. Efficiency vs Input Voltage

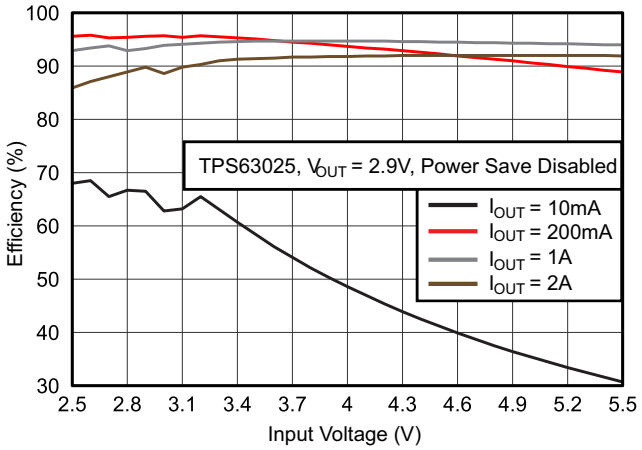


Figure 13. Efficiency vs Input Voltage

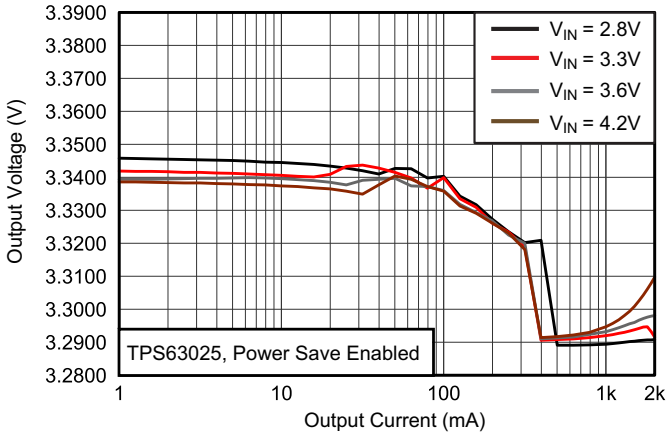


Figure 14. Output Voltage vs Output Current

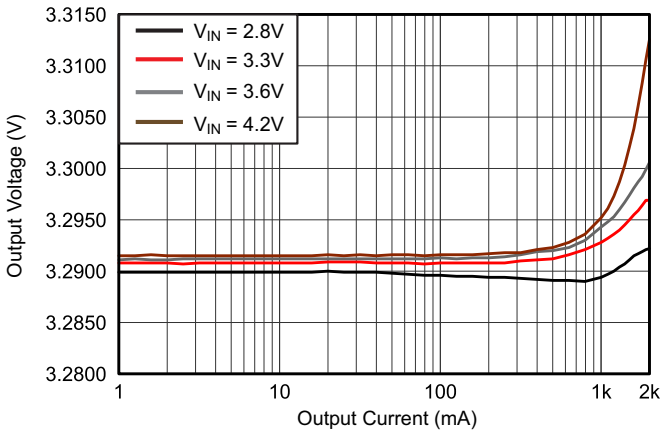


Figure 15. Output Voltage vs Output Current

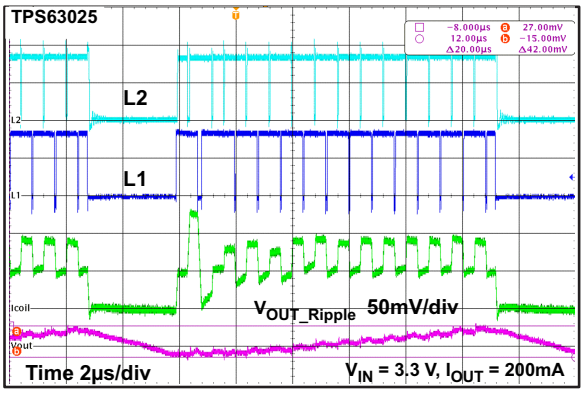


Figure 16. Output Voltage Ripple in Buck-Boost Mode and PFM to PWM Transition

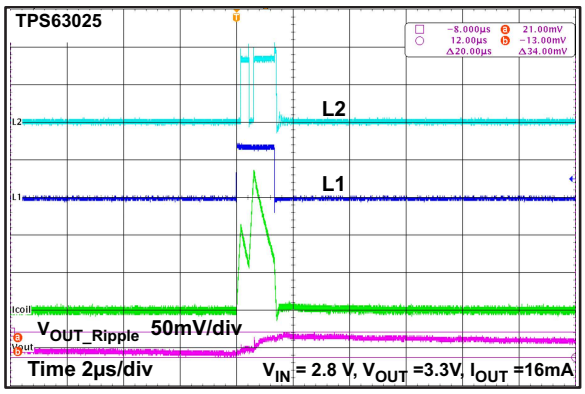


Figure 17. Output Voltage Ripple in Boost Mode and PFM Operation

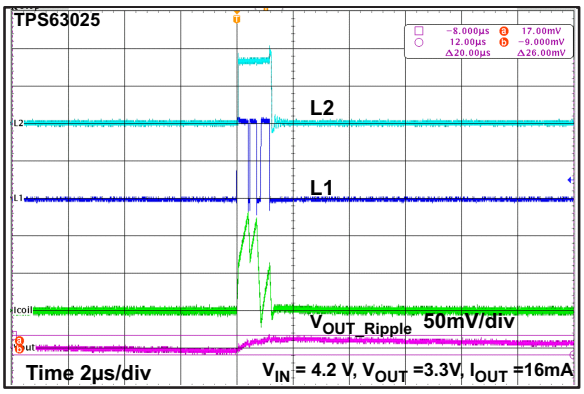


Figure 18. Output Voltage Ripple in Buck Mode and PFM Operation

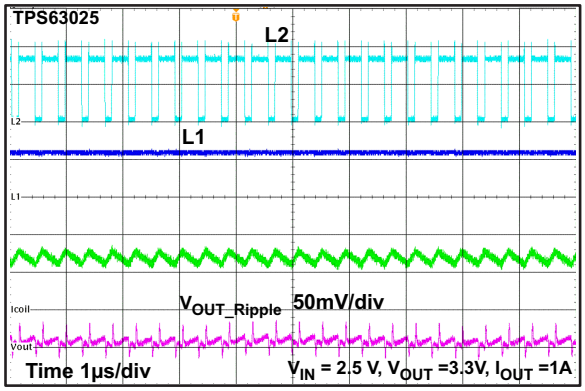


Figure 19. Switching Waveforms in Boost Mode and PWM Operation

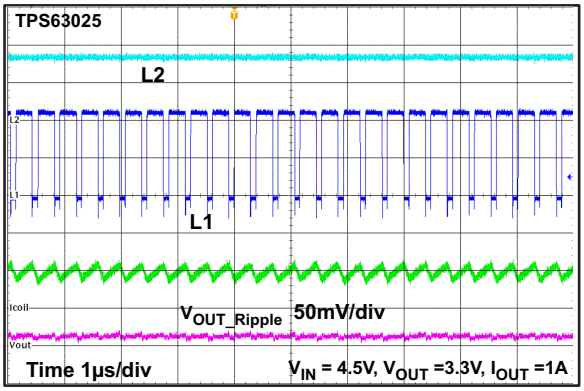


Figure 20. Switching Waveforms in Buck Mode and PWM Operation

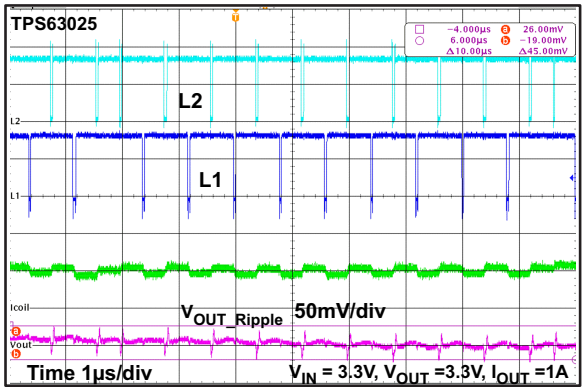


Figure 21. Switching Waveforms in Buck-Boost Mode and PWM Operation

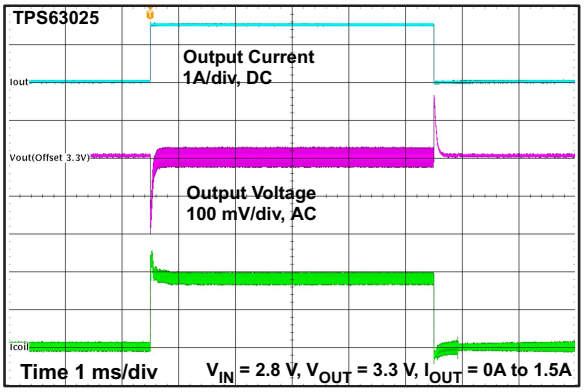


Figure 22. Load Transient Response Boost Mode

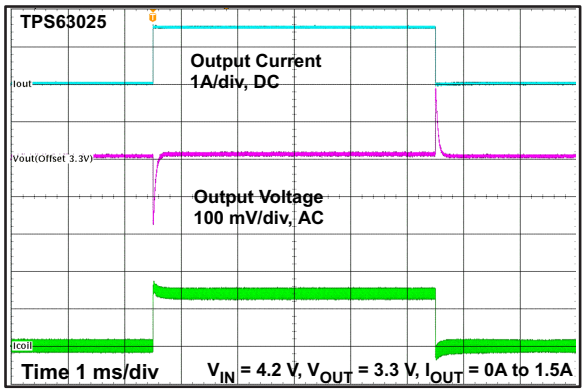


Figure 23. Load Transient Response Buck Mode

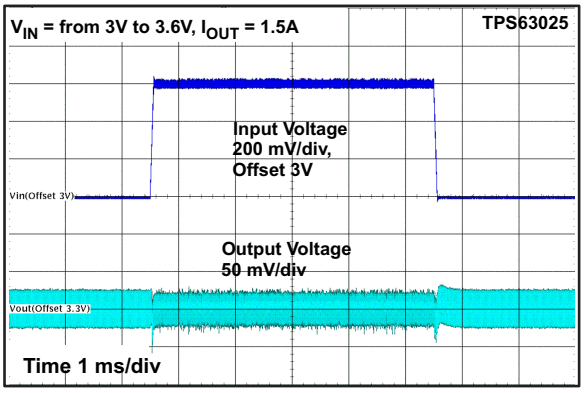


Figure 24. Line Transient Response

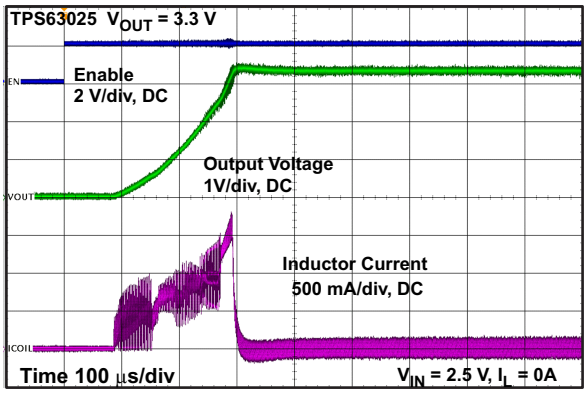


Figure 25. Start Up After Enable

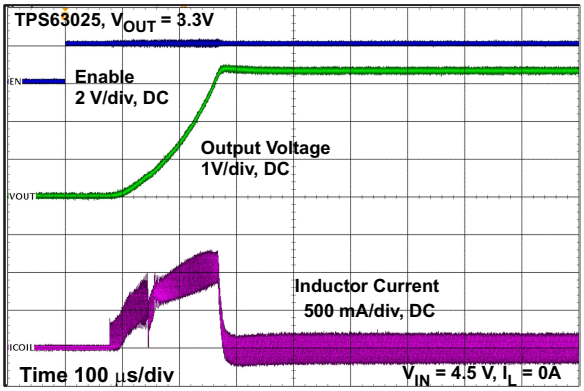


Figure 26. Start Up After Enable

11 Power Supply Recommendations

The TPS63025x device family has no special requirements for its input power supply. The input power supply's output current needs to be rated according to the supply voltage, output voltage and output current of the TPS63025x.

12 Layout

12.1 Layout Guidelines

The PCB layout is an important step to maintain the high performance of the TPS63025x devices.

- Place input and output capacitors as close as possible to the IC. Traces need to be kept short. Routing wide and direct traces to the input and output capacitor results in low trace resistance and low parasitic inductance.
- Use a common-power GND
- Use separate traces for the supply voltage of the power stage; and, the supply voltage of the analog stage.
- The sense trace connected to FB is signal trace. Keep these traces away from L1 and L2 nodes.

12.2 Layout Example

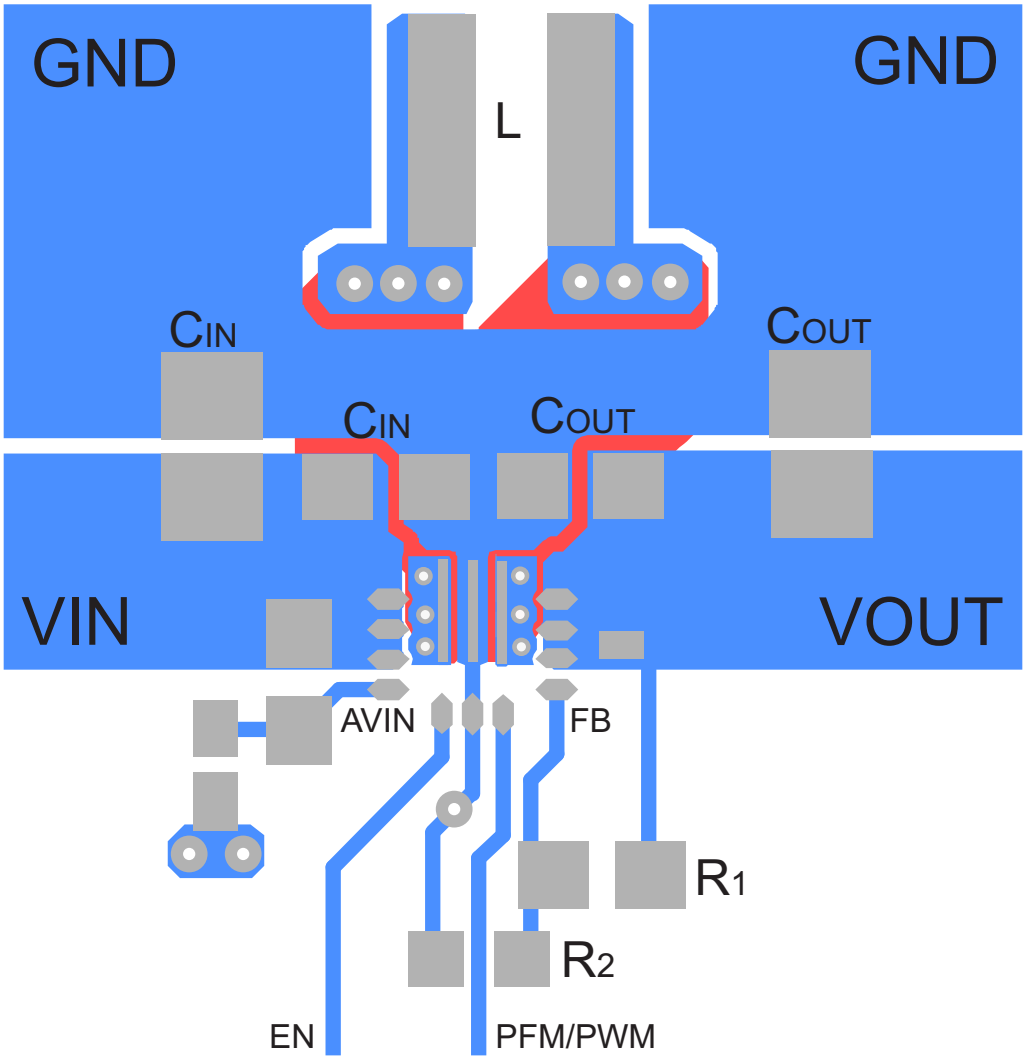


Figure 27. TPS63025x RNC Package Layout

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

TPS63025EVM-553 User's Guide, TPS63025 High Current, High Efficiency Single Inductor Buck-Boost Converter, SLVUA24

13.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS630250	Click here	Click here	Click here	Click here	Click here
TPS630251	Click here	Click here	Click here	Click here	Click here
TPS630252	Click here	Click here	Click here	Click here	Click here

13.4 Trademarks

All trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS630250RNCR	ACTIVE	VQFN-HR	RNC	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	63025P	Samples
TPS630250RNCT	ACTIVE	VQFN-HR	RNC	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	63025P	Samples
TPS630250YFFR	ACTIVE	DSBGA	YFF	20	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS 630250	Samples
TPS630250YFFT	ACTIVE	DSBGA	YFF	20	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS 630250	Samples
TPS630251YFFR	ACTIVE	DSBGA	YFF	20	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS 630251	Samples
TPS630251YFFT	ACTIVE	DSBGA	YFF	20	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS 630251	Samples
TPS630252YFFR	ACTIVE	DSBGA	YFF	20	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS 630252	Samples
TPS630252YFFT	ACTIVE	DSBGA	YFF	20	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS 630252	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

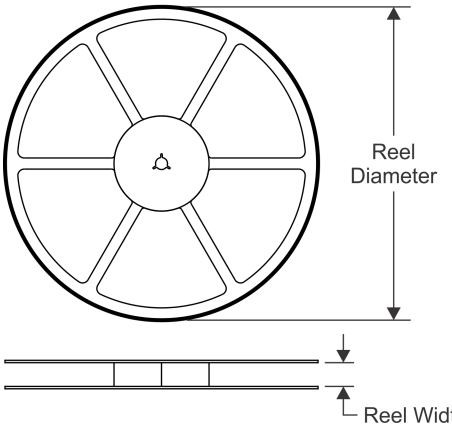
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

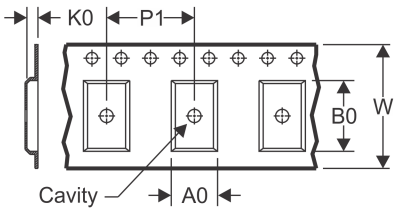
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

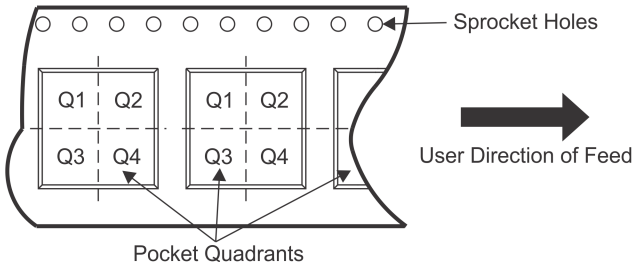


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

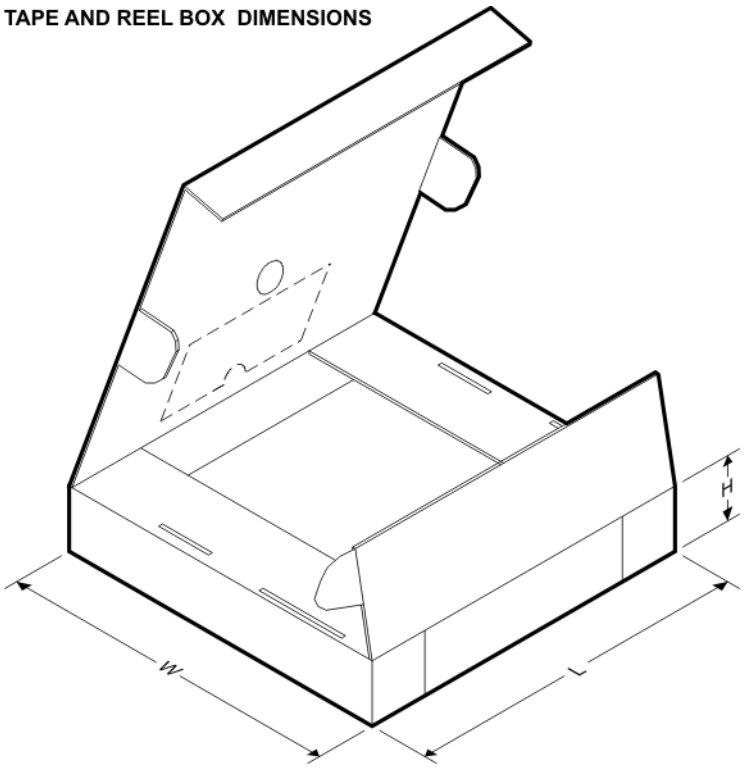
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS630250RNCR	VQFN-HR	RNC	14	3000	330.0	12.4	2.8	3.3	1.2	8.0	12.0	Q1
TPS630250RNCT	VQFN-HR	RNC	14	250	180.0	12.4	2.8	3.3	1.2	8.0	12.0	Q1
TPS630250YFFR	DSBGA	YFF	20	3000	180.0	8.4	1.89	2.2	0.69	4.0	8.0	Q1
TPS630250YFFT	DSBGA	YFF	20	250	180.0	8.4	1.89	2.2	0.69	4.0	8.0	Q1
TPS630251YFFR	DSBGA	YFF	20	3000	180.0	8.4	1.89	2.2	0.69	4.0	8.0	Q1
TPS630251YFFT	DSBGA	YFF	20	250	180.0	8.4	1.89	2.2	0.69	4.0	8.0	Q1
TPS630252YFFR	DSBGA	YFF	20	3000	180.0	8.4	1.89	2.2	0.69	4.0	8.0	Q1
TPS630252YFFT	DSBGA	YFF	20	250	180.0	8.4	1.89	2.2	0.69	4.0	8.0	Q1

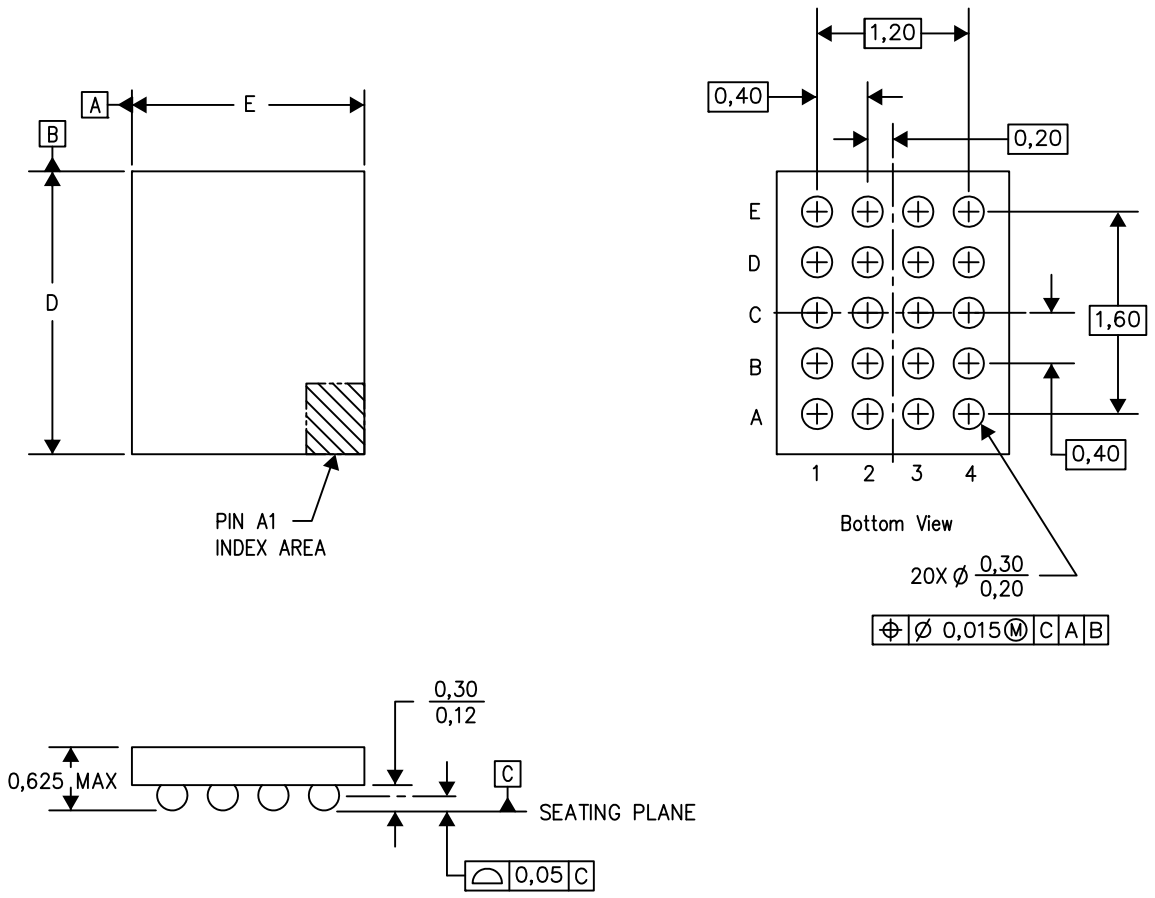
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS630250RNCR	VQFN-HR	RNC	14	3000	367.0	367.0	35.0
TPS630250RNCT	VQFN-HR	RNC	14	250	182.0	182.0	20.0
TPS630250YFFR	DSBGA	YFF	20	3000	182.0	182.0	20.0
TPS630250YFFT	DSBGA	YFF	20	250	182.0	182.0	20.0
TPS630251YFFR	DSBGA	YFF	20	3000	182.0	182.0	20.0
TPS630251YFFT	DSBGA	YFF	20	250	182.0	182.0	20.0
TPS630252YFFR	DSBGA	YFF	20	3000	182.0	182.0	20.0
TPS630252YFFT	DSBGA	YFF	20	250	182.0	182.0	20.0

YFF (R–XBGA–N20) DIE–SIZE BALL GRID ARRAY



D: Max = 2.116 mm, Min =2.056 mm

E: Max = 1.796 mm, Min =1.736 mm

4207625–9/AO 12/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

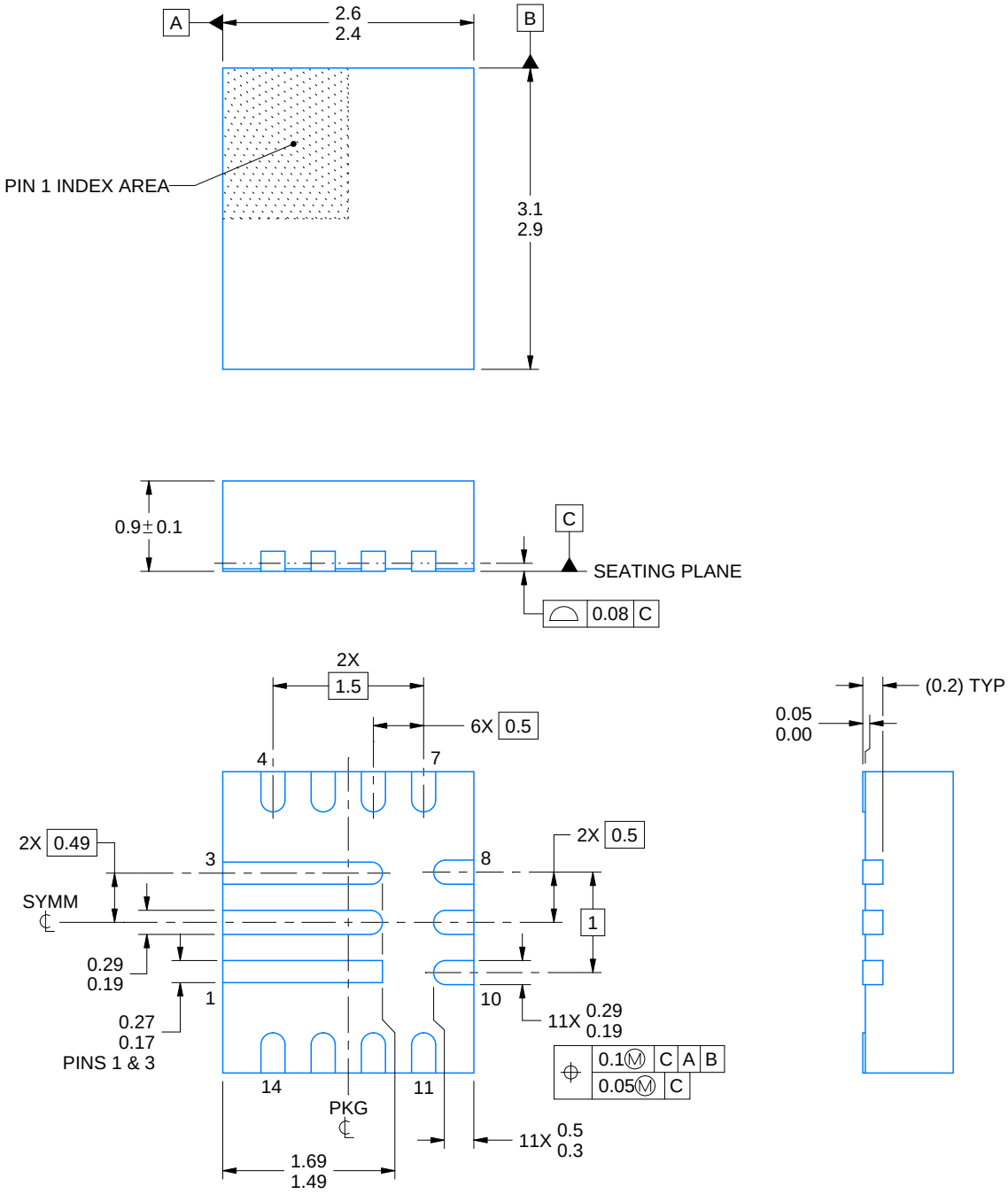
NanoFree is a trademark of Texas Instruments.

PACKAGE OUTLINE

RNC0014A

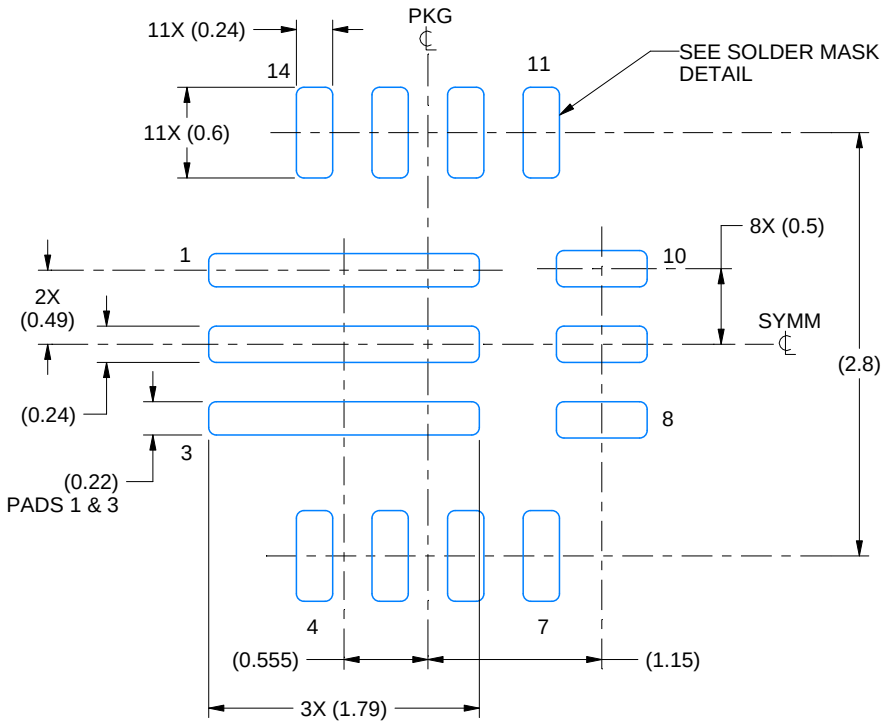
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

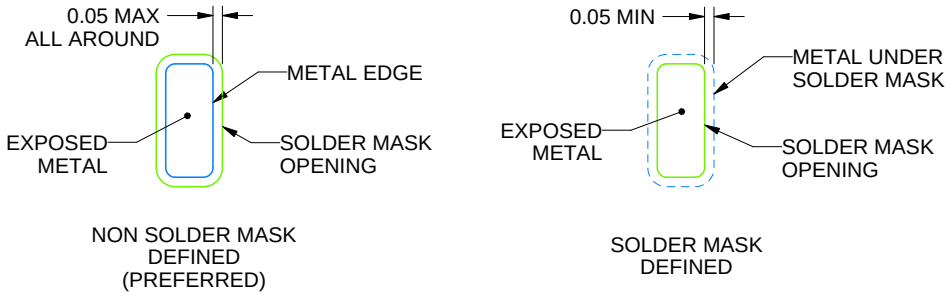


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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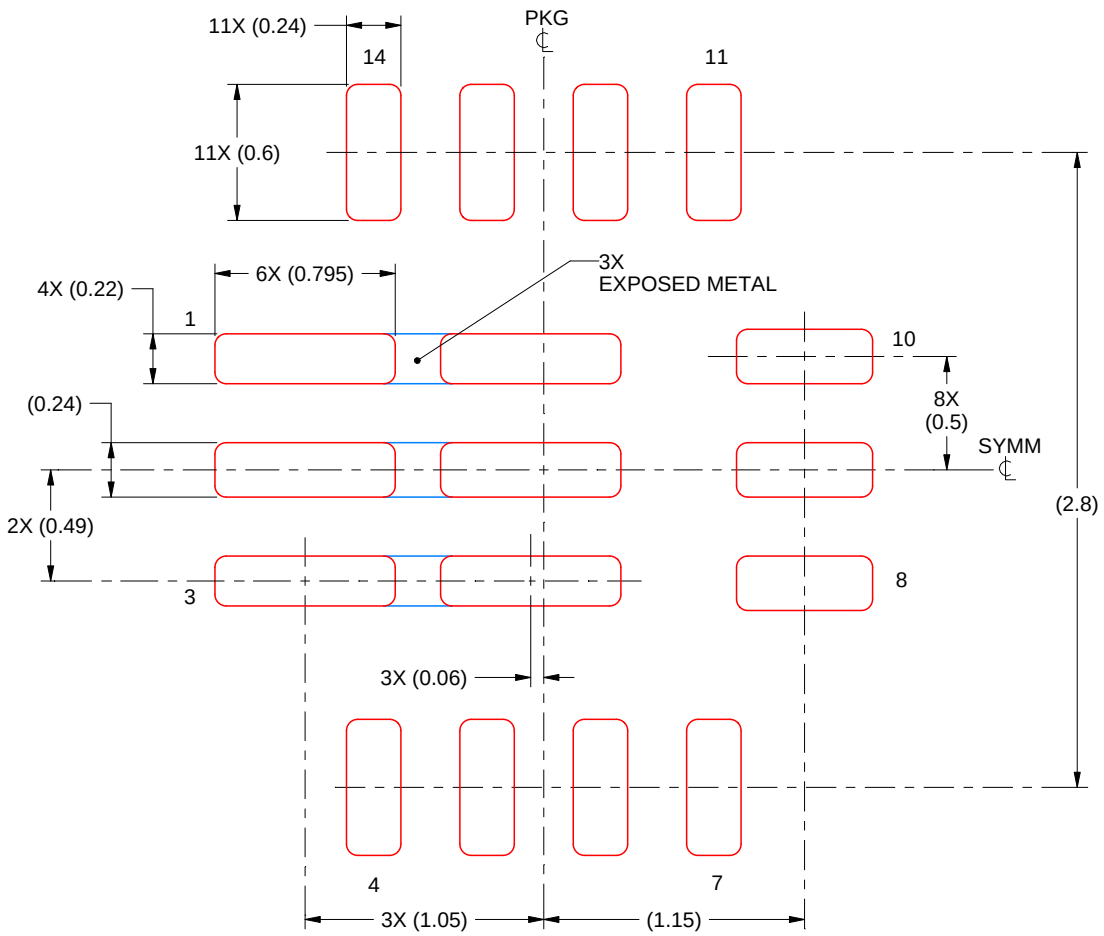
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

FOR EXPOSED PADS 1-3
89% PRINTED SOLDER COVERAGE BY AREA
SCALE:30X

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NOTES: (continued)

5. For alternate stencil design recommendations, see IPC-7525 or board assembly site preference.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265