TPS65250/1/2/3

Line Consumer Analog Product Group

TPS65250/1/2/3 LAYOUT GUIDE

The TPS65250, TPS65251, TPS65252, and TPS65253 family of power management ICs provides easy to use, flexible, 2xDCDC and 3xDCDC configurations. In order for the converters to perform optimally, certain layout rules should be followed. Passive components should be placed as close as possible to their respective pins in order to reduce trace parasitics. Input and output filters have the highest placement priority, while the placement of LDO decoupling caps is least important. A four layer board is recommended for optimal thermal management, and the power pad should be connected to the ground plane. Adherence to these guidelines will help the proper operation of your TPS65250/1/2/3 device.

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For the best performance of the chip, it is recommended that TPS6525x be used on a 4-layer board. For operation on a 2-layer board current and voltage de-rating is required, and it is application related. For further discussion, please contact the LCA Product Line.

1.1 Why a Good Layout is Important

There are different levels of activity on each PMIC pin. Pins HF AC activity are critical and the layout around them are also critical.

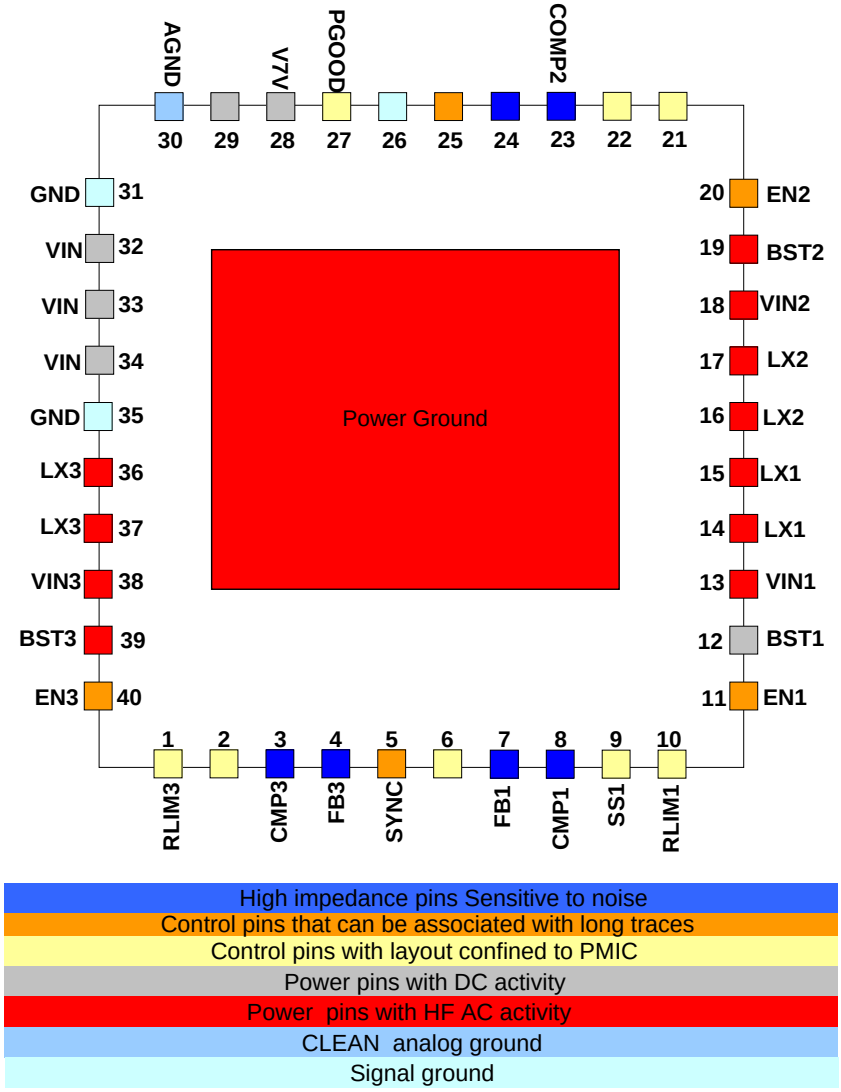

Figure 1. PMIC Layout

1.2 Component Placement Priority

In general, all external components need to be placed as close as possible to the power IC. The priorities of placement are as follows:

1. Input Vin capacitors
2. Output filter LC of switching regulators
3. COMPx pin components
4. Current limit control IRLMx,
5. OSC, SYNC pin
6. ENx pin capacitors
7. V3V and V7V output caps

1.3 PCB Stack-Up (4 Layers)

The top layer of the chip should contain DC-DC power traces and most signal lines. Any remaining area on the top layer should be filled with ground and be connected to bottom and internal grounds by strong via connection. Layer 2 is ground only and Layer 3 contains V_{IN} connections and remaining signal lines. It is critical to have a strong ground connection from all layers to each other, especially under the thermal pad. Layer 4 should be used for any additional non critical signals and ground. Use 2-oz copper for all layers if possible. See the appendix for TPS65251EVM (3 bucks) and TPS65252 (2 bucks) layout. The top side layer of the EVM is laid out in a manner typical of a multi-function DC/DC application layout.

1.4 Thermal Management

The power pad connection is used for both the thermal path and the electrical GND path in TPS6525x. Connection of power pad to ground plane helps thermal dissipation and lowers thermal resistance of the package. Moreover, the source of the low side FETs in DC-DC converters (Power ground –PGND) are connected to the power path and the thermal dissipation passes through the vias under the power pad. The EVM used 35 vias (each via: inside hole size = 0.03mm and outside hole size = 0.05mm).

1.5 Two Layer Board Usage

The TPS6525x supports both 2oz and 1oz copper trace 4 layers PCB board applications. Please contact TI before supporting the 2 layers board PCB layout.

1.6 Buck Current Flow During D Stage (Creation of AC Pulsed Current)

It is important to make sure that the GND path between input caps, output cap and the power pad GND is very short. The connection from Lx pins to inductors should be as close as possible. The current AC path includes input capacitor, HS fet, output inductor, and output capacitor. The PMIC current path includes Vin Pin, Lx pins and power PAD.

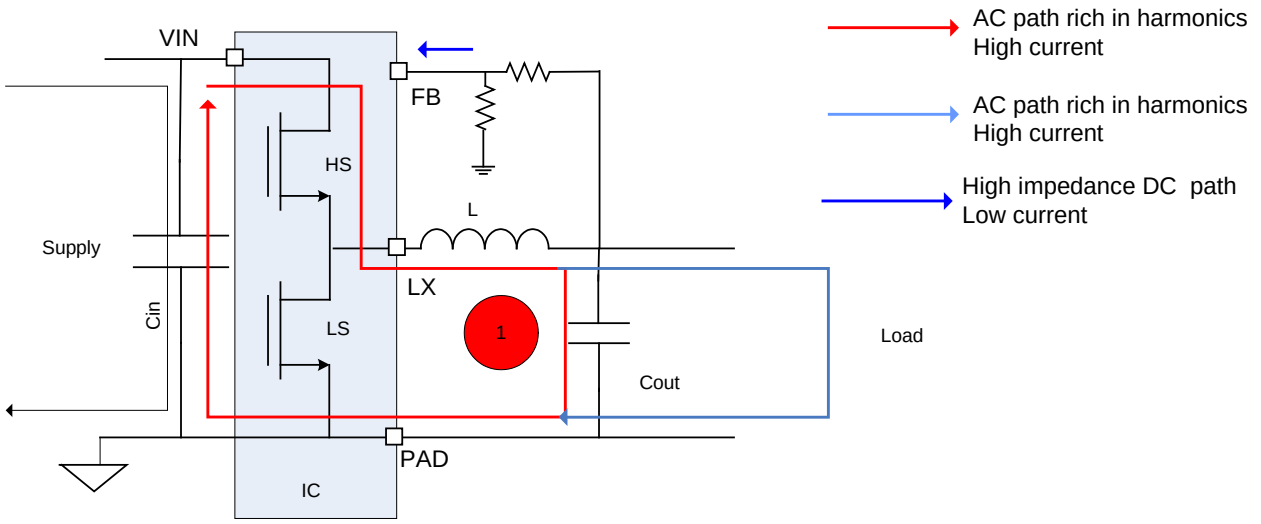

Figure 2. Current Flow through D Stage

1.7 Buck Current During (1-D) Stage (Creation of AC Pulsed Current)

The current AC path includes LS fet, output inductor and the output capacitor. The PMIC current path includes the Lx Pins and the power pad.

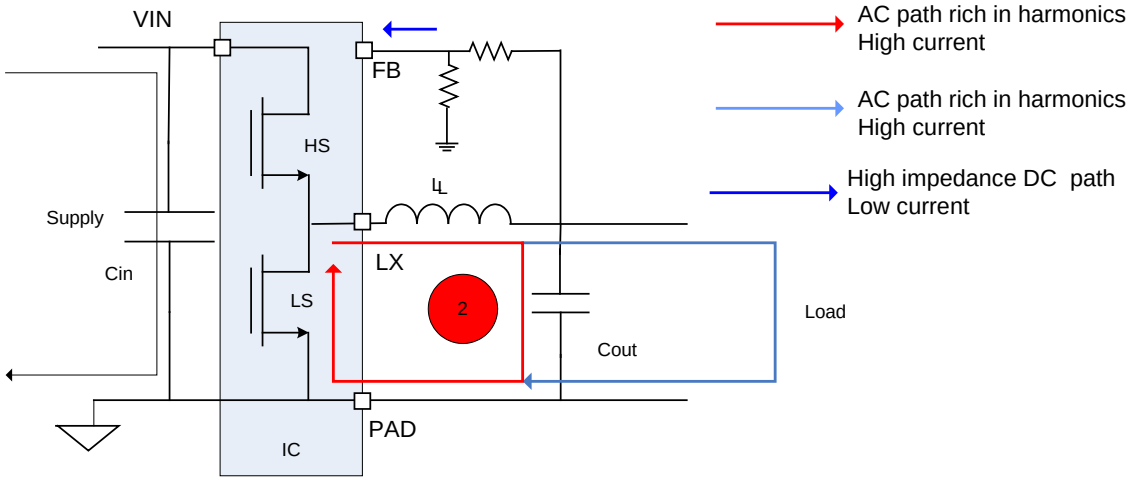

Figure 3. Buck Current During (1-D) Stage

1.8 Input Capacitor Placement

The placement and connection of input capacitor is critical. The goal is to reduce parasitic inductance between input capacitor and Vin input pins. Also, the input capacitor ground should be directly connected to power ground through multiple areas to reduce ground connection inductance. High parasitic inductances increase spike voltage on internal FETs during switching rise and fall time due to L di/dt rule. Ultimately reducing these parasitic inductances is essential to prevent EOS events. Parasitic inductance can be reduced by making the path from input capacitor to IC Vin pin as short and wide as possible. The goal is to make the connection around 0.05inches (1 to 1.5 mm). See figure 5 simple block diagram of Lpar.

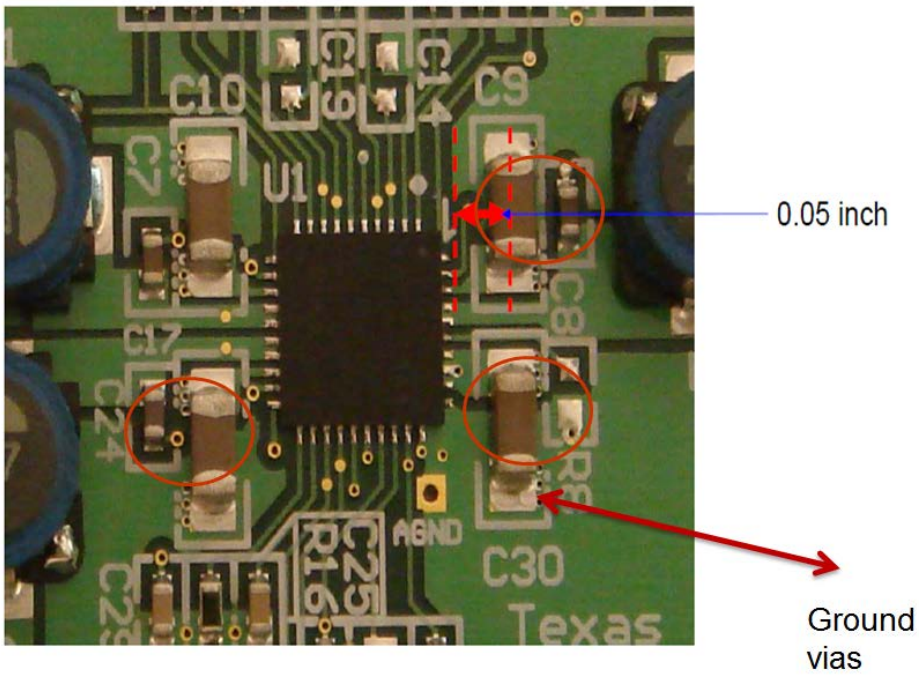

Figure 4. Input Capacitor Placement

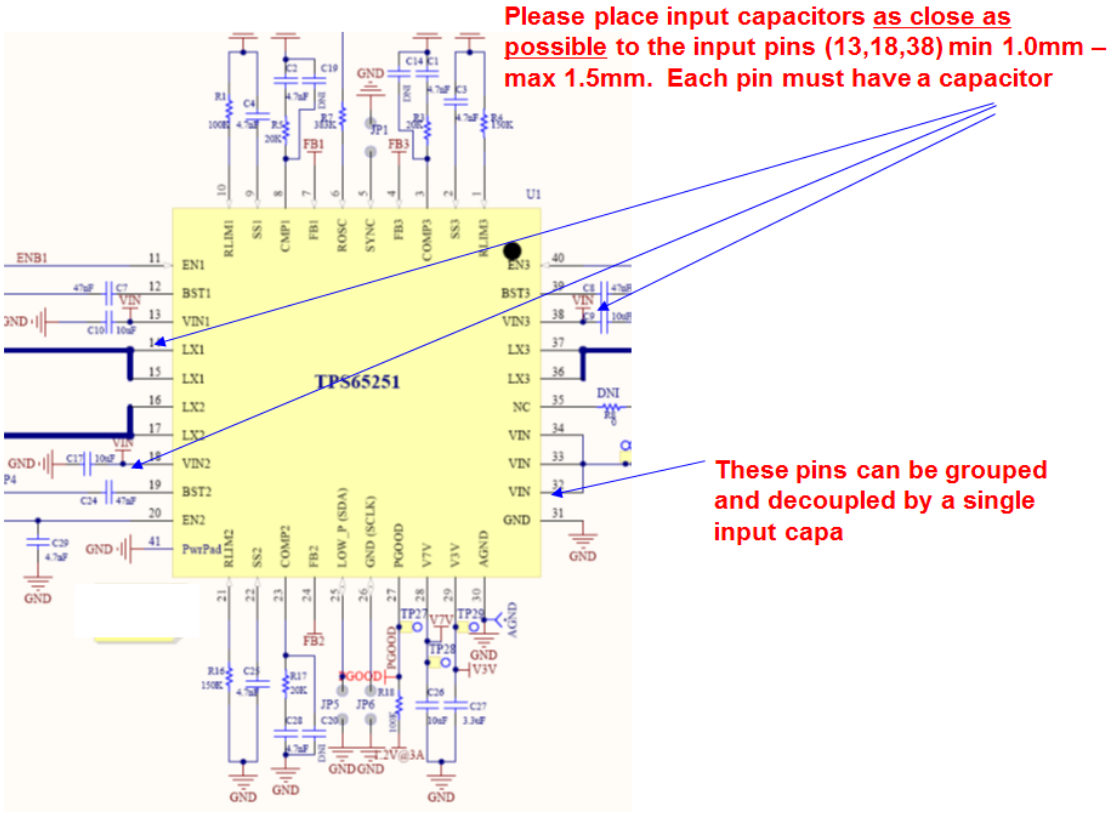

Figure 5. Capacitor Placement

1.9 Bad PCB Layout

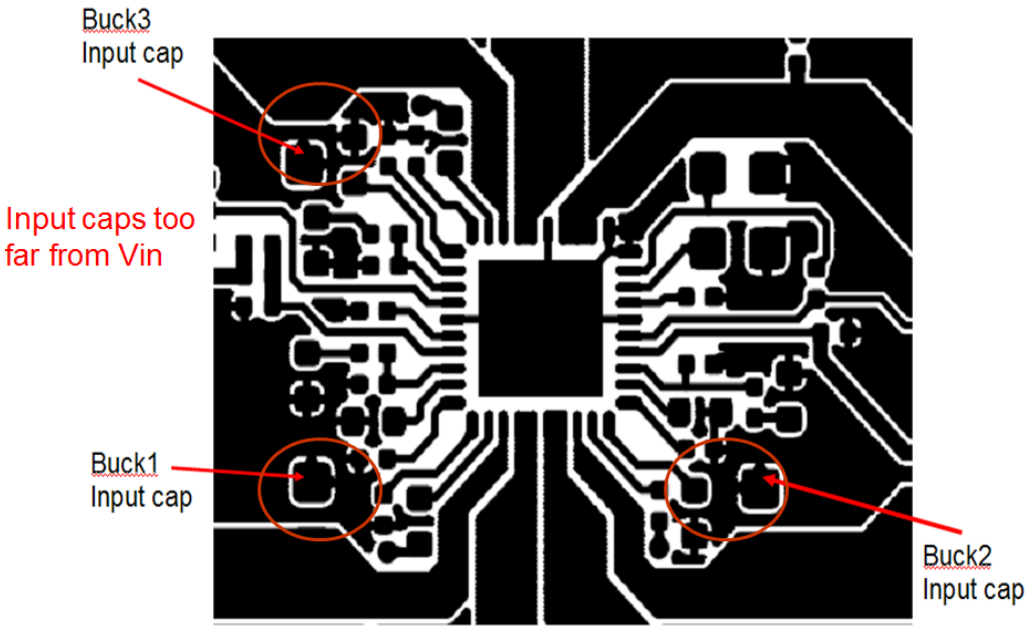

Figure 6. Bad PCB Layout 1

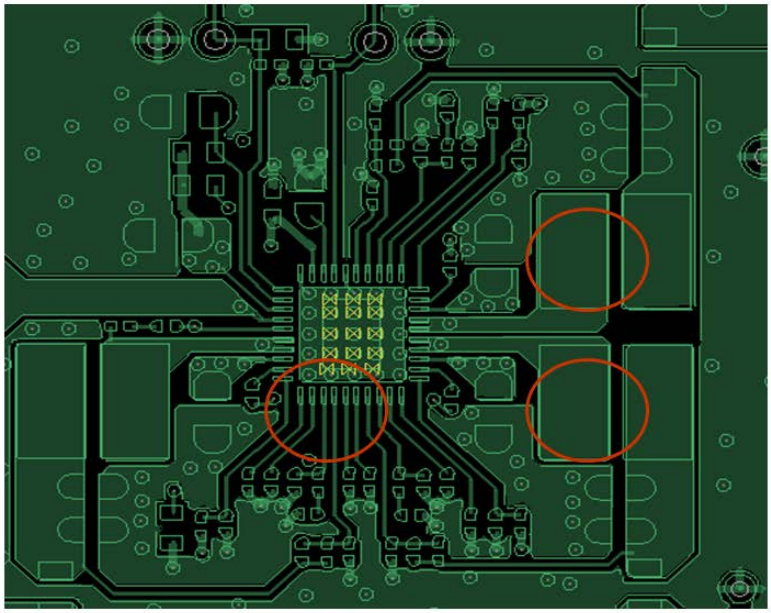

Figure 7. Bad PCB Layout 2

1.10 Output Filter Considerations 1

For the output considerations, the inductor traces should be on top of the board. Try to make inductor connection to LX width around 2.5mm. Also, make the inductor trace to LX as short as possible. The distance should be minimized from output capacitor ground to input capacitor ground and power pad. The vias should be added to the GND connection of output capacitor. If possible connect beginning of feedback divider to output capacitor. FBx trace connects to a high impedance pin. Make the trace as short as possible and avoid noisy areas (associated with AC Paths). Make sure the ground of the feedback divider connects to a clean section of the ground plane (not on the path of AC currents).

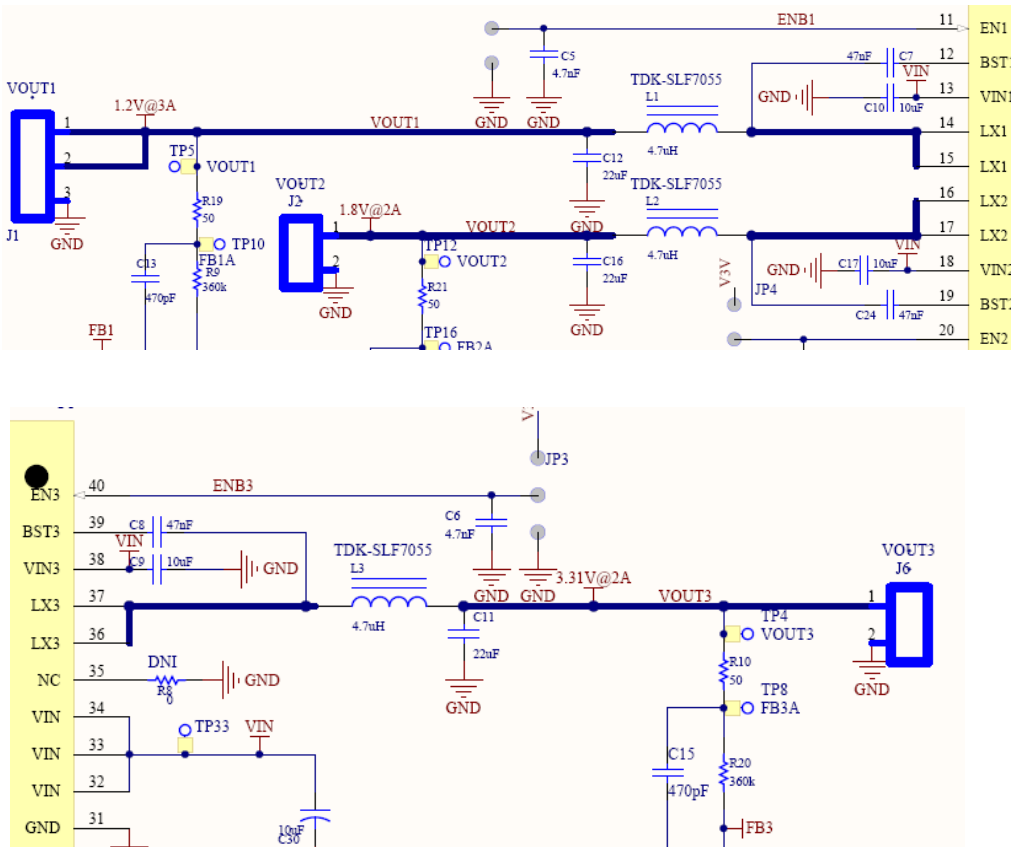

Figure 8. Output Filter Considerations 1

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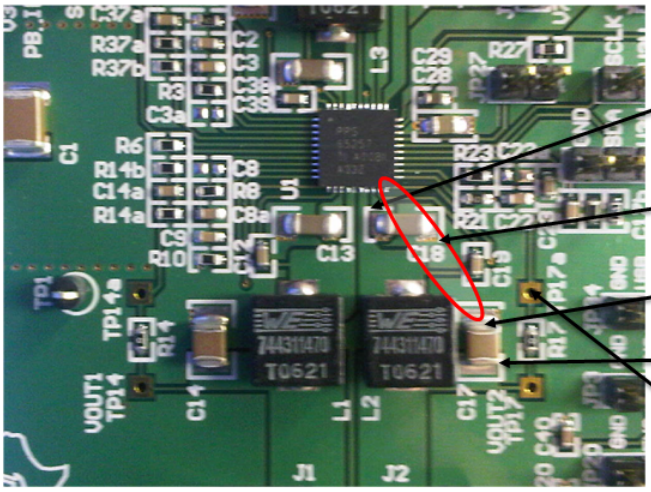
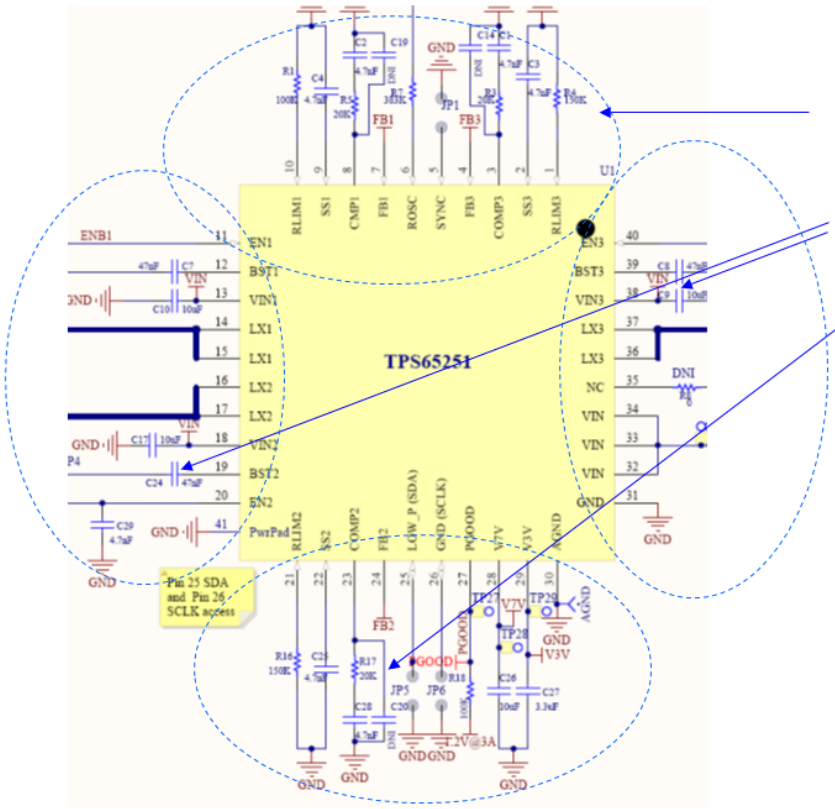
1.11 Output Filter Considerations 2



- Try to make inductor connection to LX width around 2.5mm
- Make the inductor trace to LX as short as possible
- Minimize the distance from output capacitor ground to input capacitor ground and power pad
- Add vias to GND connection of output capacitor
- If possible connect beginning of feedback divider to output capacitor
- FBx trace connects to a high impedance pin. Make the trace as short as possible and avoid noisy areas (associated with AC Paths).
- Make sure the ground of the feedback divider connects to a clean section of the ground plane (not on the path of AC currents)

Noisy and Sensitive Signals, Compensation and BST Caps.
Noisy and sensitive signals should be routed far away from each other. In switching regulators, LX switching nodes and BST (bootstrap) are among the noisiest source. Most sensitive analog signals are compensation and FB routes. Care should be taken to make sure that LX and BST signals are not coupling into FB and compensation pattern routes.

1.12 Control Components Placement



Please place the passive elements associated with the pin as possible. Applies to

- ROSC, RLIMx, SSx, ENx pins
- COMPx pins. These pins are high impedance pins, make traces as short as possible and components closer to the pin.
- Make sure connection to GND of passive components is good (add a via to GND planenext to each ground connection)
- If SYNC and Enx pins are driven by host processor, traces to the pins need to be routed away from noisy AC paths. Contemplate the possibility of guarding the traces.
- Place Boostrap capacitors close to pin and treat connection to BSTx pin as a noisy trace.

1.13 Feedback Traces

With the feedback traces, make sure point of regulation is close to the output capacitor, and the point of regulation trace to feedback resistor is a separated trace (kelvin) connected to the feedback divider. Also, make sure the trace is short, not routed close to noise paths, and the Mid-point of the divider is a high impedance point. The trace to pin should be short. Keep connections to the top layer, avoid changing layers, and make sure divider ground is connected to a clean ground section.

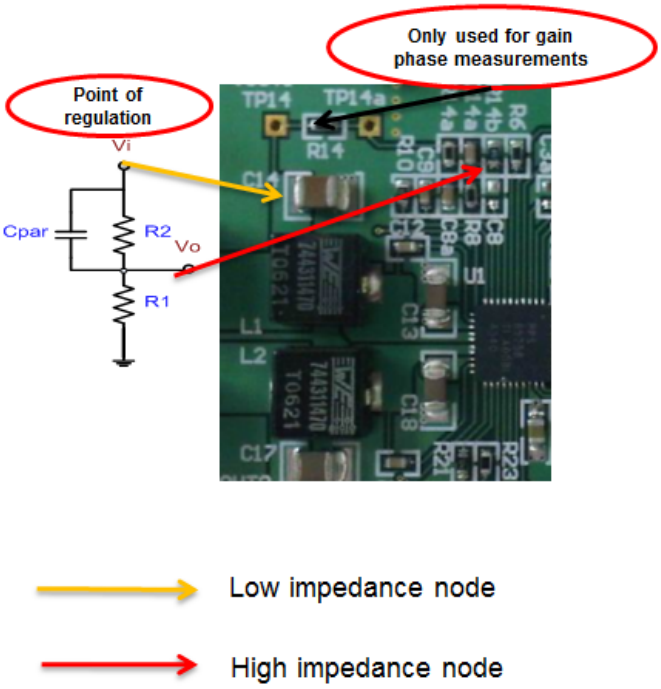
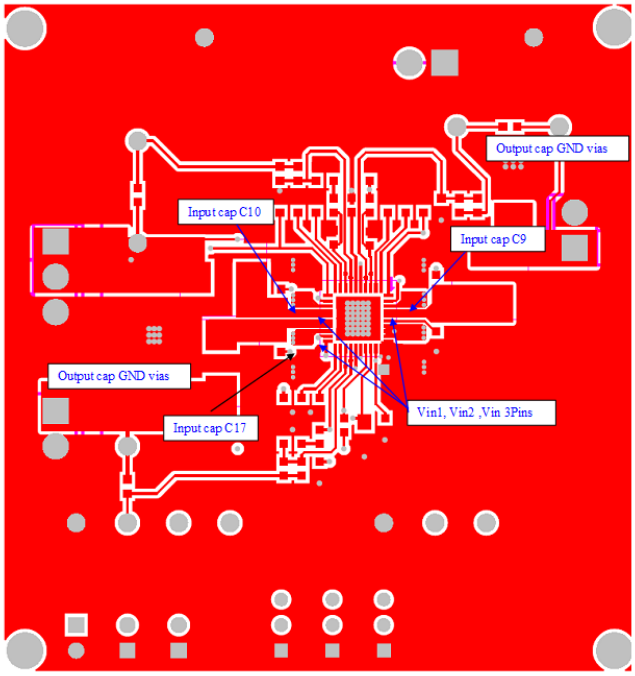


Figure 9: Feedback Traces

Appendix A. TPS6525x Layout Examples



See input cap location and output cap GND vias for high current pass support.

Figure A-1. TPS6251 Top Layer

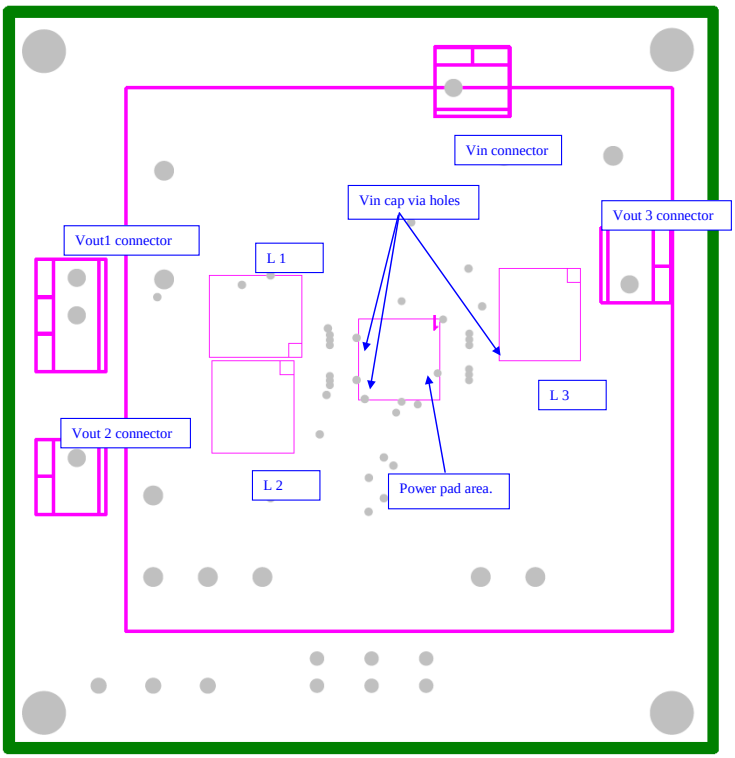


Figure A-2. TPS65251 Ground (2nd) Layer

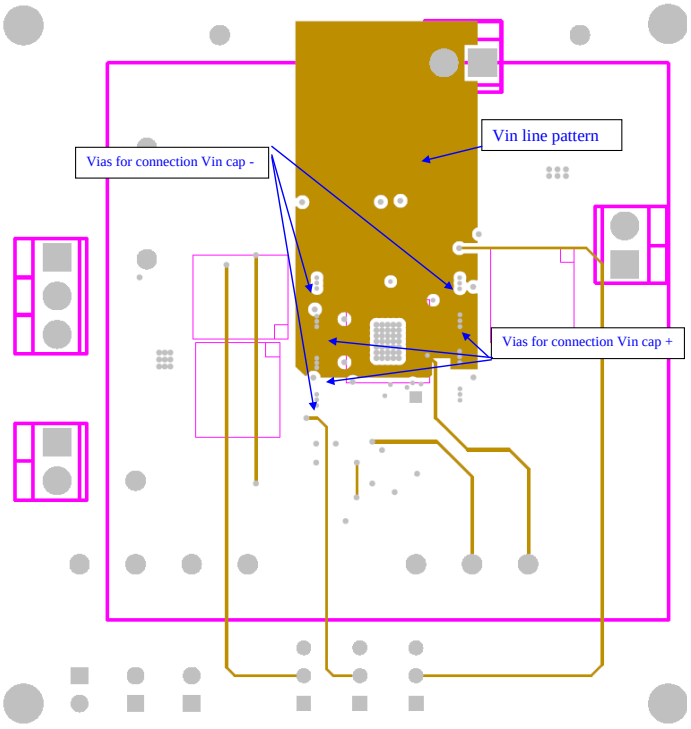
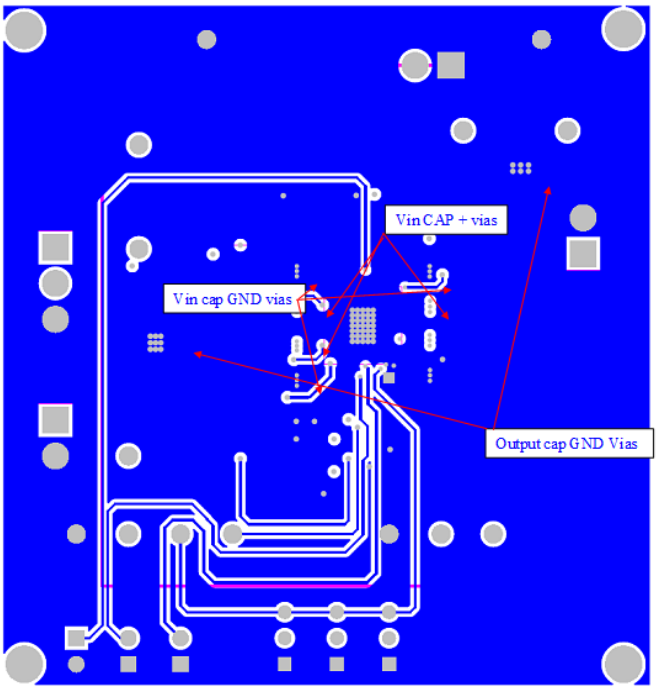


Figure A-3. TPS65251 3rd Layer



Bottom layer can be used to improve thermal dissipation by filling it with GND. Do not cut the GND plane area with traces near the TPS65251.

Figure A-4. TPS65251 Bottom Layer

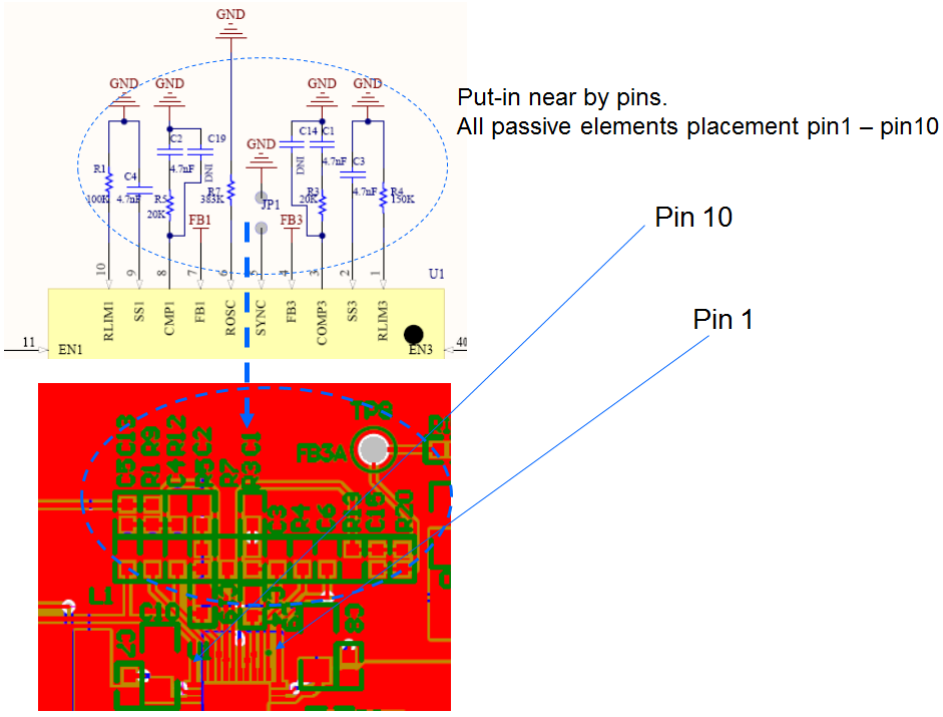


Figure A-5. TPS6251 Placement Example 1

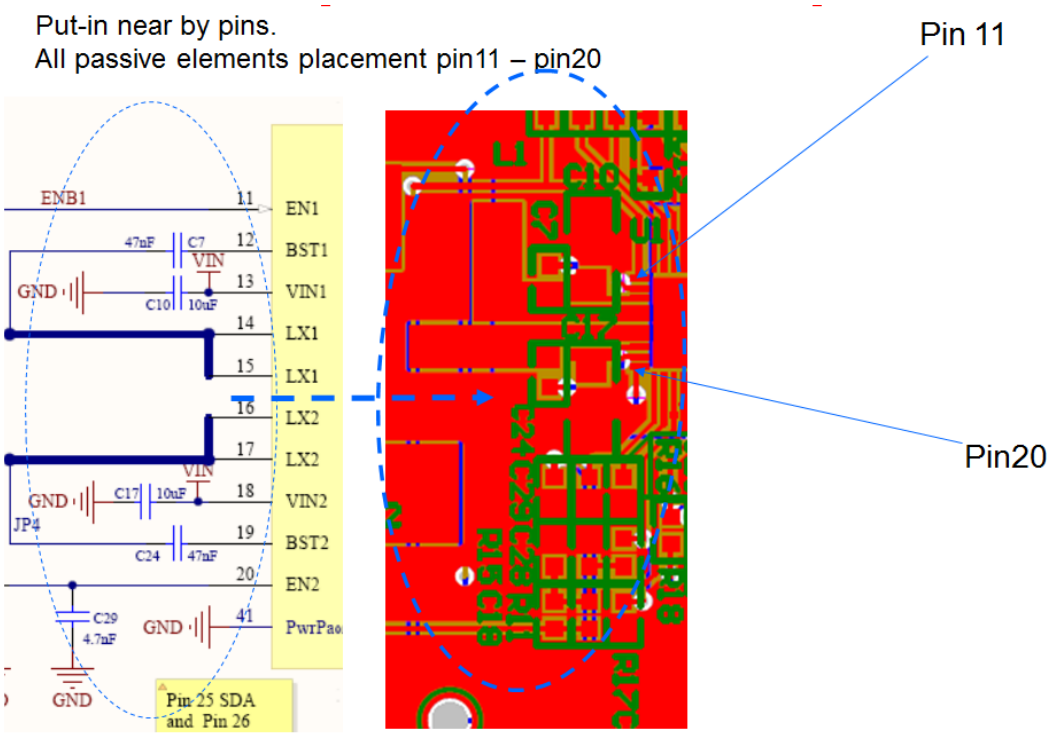


Figure A-6. TPS65251 Placement Example 2

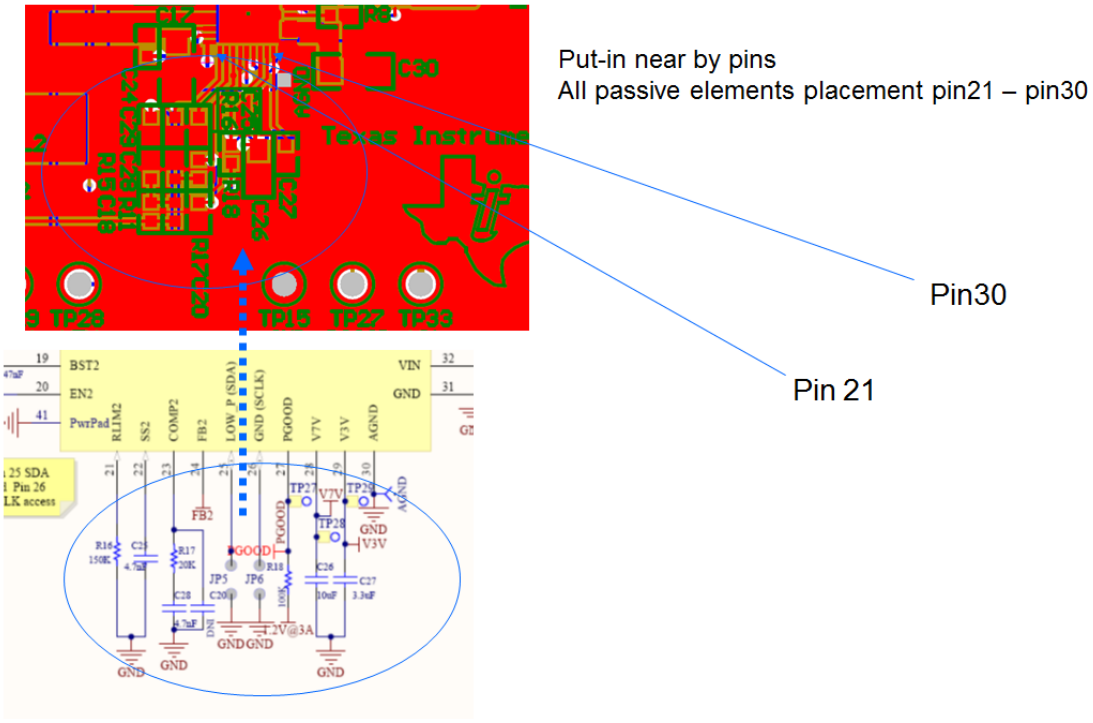


Figure A-7. TPS65251 Placement Example 3

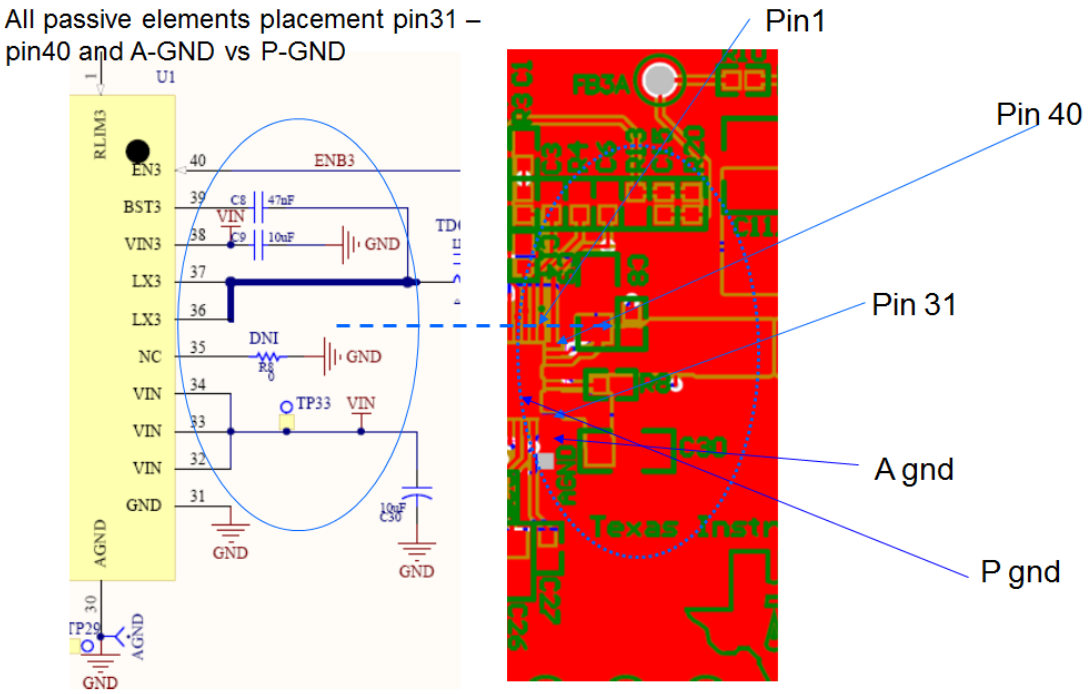


Figure A-8. TPS65251 Placement Example 4

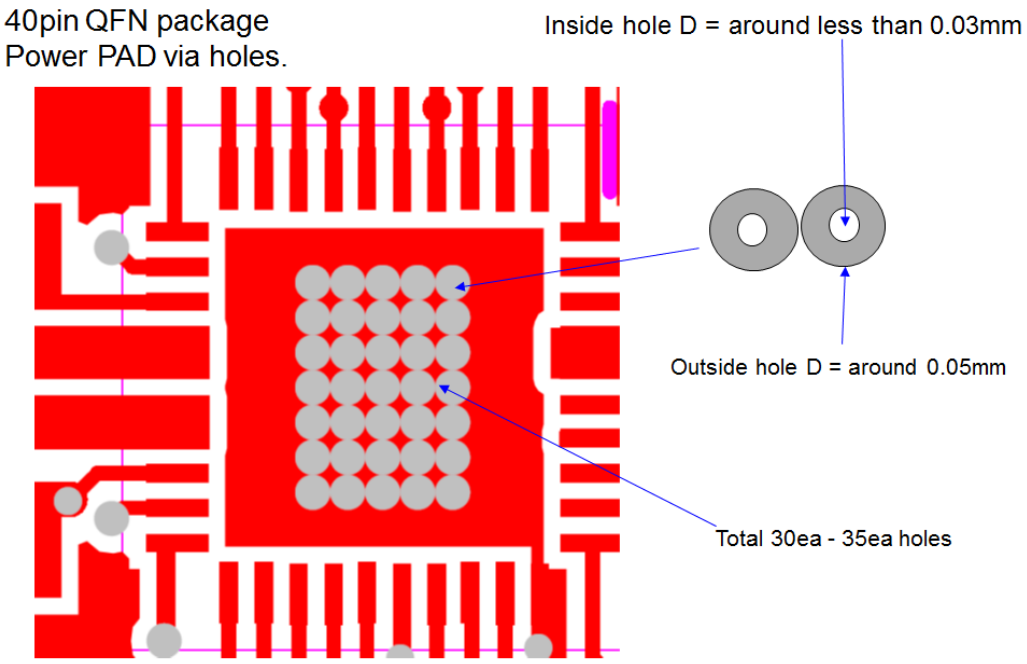


Figure A-9. TPS65251 Power Pad Example

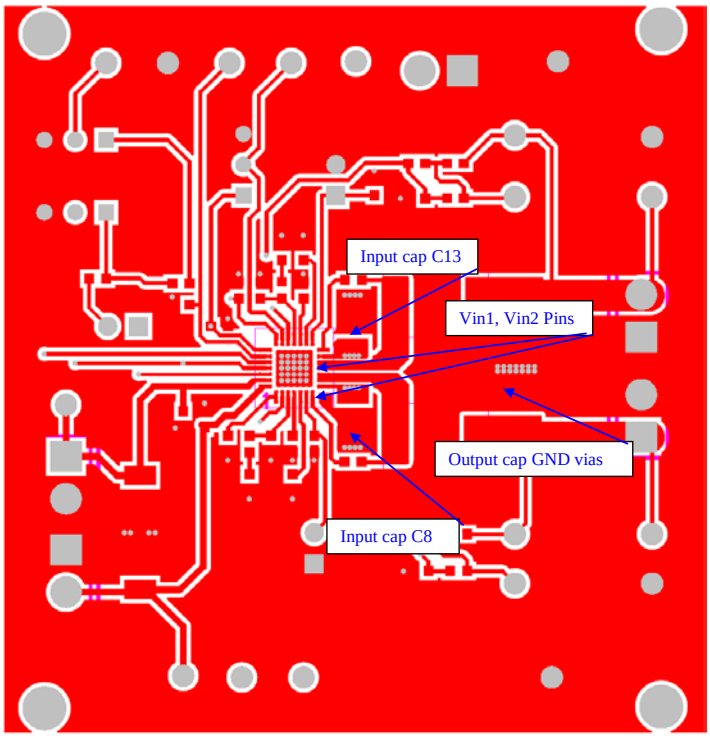


Figure A-10. TPS65252 Top Layer

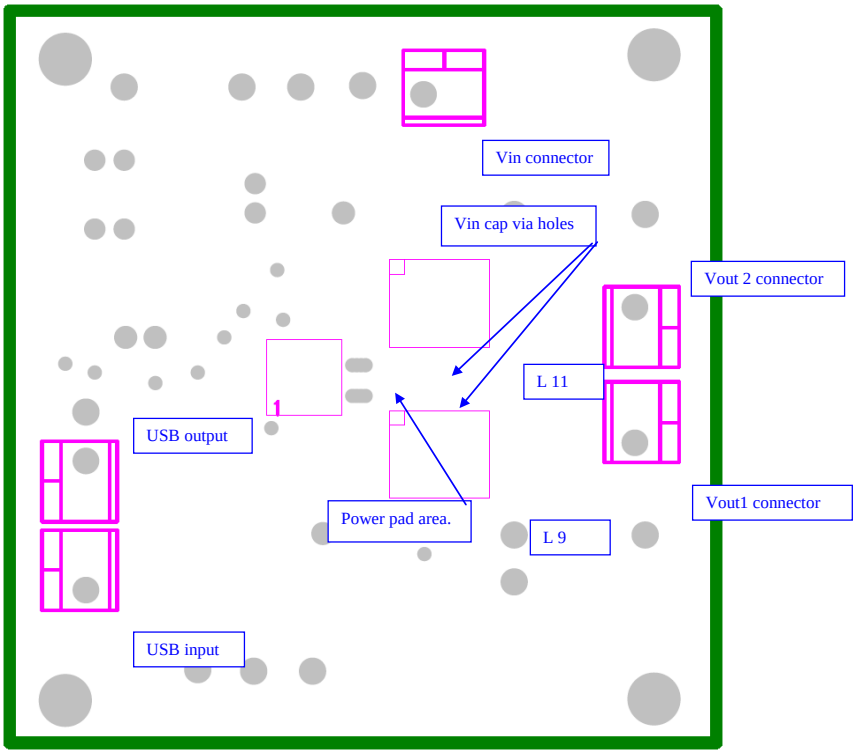


Figure A-11. TPS65252 Ground (2nd) Layer

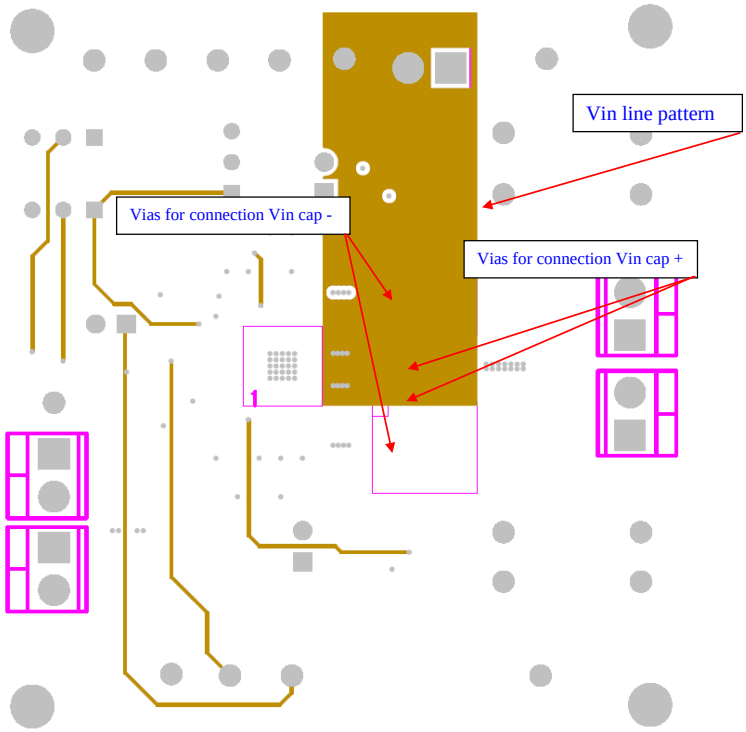


Figure A-12. TPS65252 3rd Layer

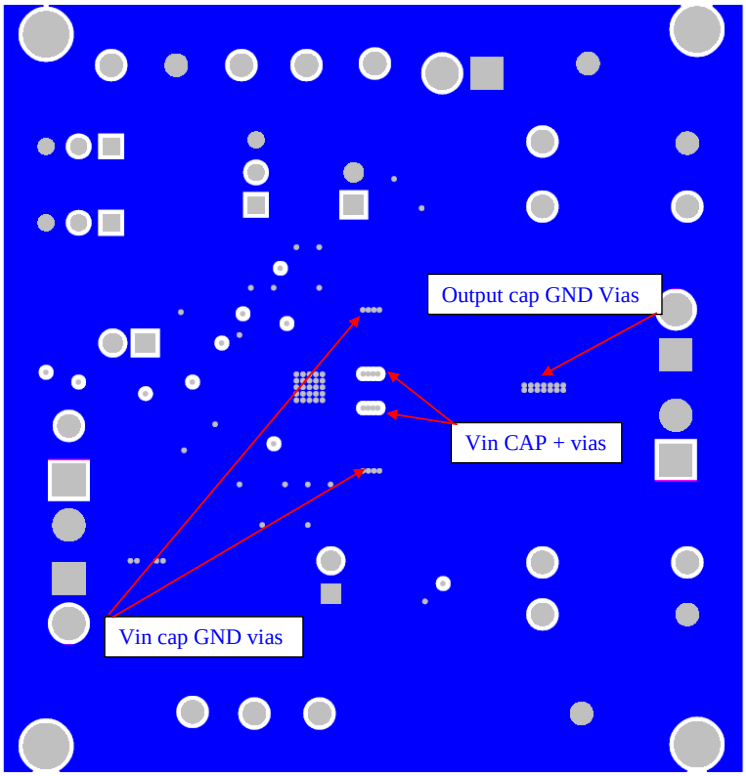


Figure A-13. TPS65252 Bottom Layer

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