

TPS65310A-Design-Checklist

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(applies to TPS65310A-Q1)

Pin Name	Pin #	Type	Signal	Description	external circuit	if not used
VSENSE	1	Analog	I	Input to monitor the battery line for under-voltage conditions. UV will be indicated by the IRQ pin.	Typical resistor to input(Battery) voltage	n/a
VIN	2	Power	PWR	Unprotected supply input for the base functionality and band gap 1. Supplied blocks are: RESET, WD, Wake, SPI, Temp Sensing, Voltage Monitoring and the Logic block.	Blocking cap to gnd min. 100nF	n/a
GPFET	3	Digital	O	Gate Driver external protection PMOS FET.	Gate of external protection Ptype-FET	open
VINPROT	4	Power	PWR	Main input supply pin (Gate Drivers & Bandgap2)	Blocking cap to gnd min. 100nF at pin + 2.2uF + 47uF closed to the HS MOS transistor of BUCK1	n/a
HSCTRL	5	Analog	O	High Side Gate driver output	Gate of an external PMOS for LED	VIN
HSENSE	6	Analog	I	Sense Input High Side / LED	shutn resistor to measure LED current	VIN
WAKE	7	Digital	I	Wake Up Input (Pull down)		leave open
EXTSUP	8	Power	PWR	Optional LV input for gate driver supply	min. 100nF blocking cap. to GND as closed as possible to pin	n/a
VREG	9	Power	PWR	Internal regulator for gate driver supply (decoupling) and VREF.	min. 2.2uF blocking cap to gnd + 100nF cap to gnd as closed as possible to pin	n/a
BOOT1	10	Power	PWR	The capacitor on these pins act as the voltage supply for the high side MOSFET gate drive circuitry.	min. 100nF cap to PH1 as closed as possible to device	n/a
GU	11	Power	PWR	Gate Driver – high side FET	Gate HS transistor(Ntype) BUCK1, short connection	n/a
PH1	12	Power	PWR	Switching Node - BUCK1 (floating ground for high side FET driver)	HS/LS Transistor(Ntype) and cap of Buck1 converter	n/a
GL	13	Power	PWR	Gate Driver – low side FET	Gate LS transistor(Ntype) BUCK1, short connection	n/a
PGND1	14	GND	GND	Ground for low side FET driver		n/a
S1	15	Analog	I	Differential current sense inputs for BUCK1, S2 pull-down only active in RAMP and ACTIVE state	Current sense resistor for BUCK1	n/a
S2	16	Analog	I		Current sense resistor for BUCK1	n/a
VMON1	17	Analog	I	Input pin for the independent voltage monitor at BUCK1	Monitoring voltage divider BUCK1	n/a
COMP1	18	Analog	O	Error Amplifier output for the switching controller. External compensation network is connected to this node	compensation network BUCK1	n/a
VSENSE1	19	Analog	I	Input for externally sensed voltage of the output using a resistor divider network from their respective output line to ground.	Control voltage divider BUCK1	n/a
COMP5	20	Analog	O	Error Amplifier output for the Boost switching controller. External compensation network is connected to this node	compensation network BOOST	GND
VSENSE5	21	Analog	I	Input for externally sensed voltage of the Boost output using a resistor divider network from their respective output line to ground.	Control voltage divider BOOST	VSENSE1
PGND5	22	GND	GND	Power Ground Boost Converter		GND
PH5	23	Power	PWR	Switching Node Boost	Coil and diode of BOOST converter	open
VBOOST	24	Power	I	Booster Output Voltage	min 50uF cap. to GND	open
VT_REF	25	Analog	O	Shutdown comparator reference output. Internally connected to DVDD, current-limited. When not in use can be connected to DVDD or left open.		DVDD or leave open
PRESN	26	Digital	O	Peripherals Reset (Open Drain)		n/a
RESN	27	Digital	O	System Reset (Open Drain)		n/a
IRQ	28	Digital	O	Low Battery Interrupt Output in Operating Mode (Open Drain)		n/a
BOOT2	29	Power	PWR	The capacitor on these pins act as the voltage supply for the High-Side MOSFET gate drive circuitry.	min. 100nF cap. to PH2 as closed as possible to device	leave open

VSUP2	30	Power	PWR	Input Voltage Supply for Switch mode Regulator BUCK2	min. 10uF + 1uF blocking cap. to GND	leave open
PH2	31	Power	PWR	Switching Node BUCK2	Coil and cap of Buck2 converter	leave open
PGND2	32	GND	GND	Power ground of synchronous converter BUCK2.		leave open
VMON2	33	Analog	I	Input pin for the independent voltage monitor at BUCK2	Monitoring voltage divider BUCK2	VMON1
COMP2	34	Digital	I	Compensation selection for the BUCK2 switching converter.	low, open or high digital signal to define internal compenmsation of buck2	GND
VSENSE2	35	Analog	I	Input for externally sensed voltage of the output using a resistor divider network from their respective output line to ground.	Control voltage divider BUCK2	leave open
VSENSE3	36	Analog	I	Input for externally sensed voltage of the output using a resistor divider network from their respective output line to ground.	Control voltage divider BUCK3	leave open
COMP3	37	Digital	I	Compensation selection for the BUCK3 switching converter.	low, open or high digital signal to define internal compenmsation of buck3	GND
VMON3	38	Analog	I	Input pin for the independent voltage monitor at BUCK3	Monitoring voltage divider BUCK3	VMON1
PGND3	39	GND	GND	Power ground of synchronous converter BUCK3		n/a
PH3	40	Power	PWR	Switching Node BUCK3	Coil and cap of Buck3 converter	leave open
VSUP3	41	Power	PWR	Input Voltage Supply for Switch mode Regulator BUCK3	min. 10uF + 1uF blocking cap. to GND	leave open
BOOT3	42	Power	PWR	The capacitor on these pins act as the voltage supply for the BUCK3 High-Side MOSFET gate drive circuitry.	min. 100nF cap. to PH3 as closed as possible to device	leave open
WD	43	Digital	I	Watchdog input pin. WD is the trigger input coming from the MCU. (Pull down)		n/a
CSN	44	Digital	I	SPI – Chip select (Pull up)		leave open
SDI	45	Digital	I	SPI – Master Out Slave In (Pull down)		leave open
SCK	46	Digital	I	SPI – Clock (Pull down)		leave open
SDO	47	Digital	O	SPI – Master In Slave Out - Push Pull Output supplied by VIO		n/a
VIO	48	Power	PWR	Supply Input for the Digital Interface to the MCU. Voltage on this input will be monitored. If VIO falls below UV threshold a reset will be generated and the part enters Error Mode.	min. 100nF cap. as closed as possible to GND	n/a
HSPWM	49	Digital	I	High side / LED PWM Input (Pull down)		leave open
VSUP4	50	Power	PWR	Input Voltage Supply for Linear Regulator LDO	min. 1uF cap. as closed as possible to GND	leave open
LDO	51	Power	PWR	Linear regulated output (connect a low ESR ceramic output capacitor to this terminal)	10uF cap. as closed as possible to GND	leave open
VSENSE4	52	Analog	I	Input for externally sensed voltage of the output using a resistor divider network from their respective output line to ground.	Control voltage divider LDO	VMON1
VREF	53	Analog	O	Accurate reference voltage output for peripherals on the system (e.g. ADC)	1uF cap. as closed as possible to GND	n/a
VT	54	Analog	I	Input pin for the comparator with shutdown functionality. This input can be used to sense an external NTC resistor to shut down the IC in case of TA too high / TA too low. Tie to GND if not in use.		GND
DVDD	55	Power	PWR	Internal DVDD output for decoupling	100nF + 1uF cap. as closed as possible to GND	n/a
GND	56	GND	GND	Analog GND, digital GND and substrate connection		n/a

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