Application Report
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# TPS65310A-Q1 and TPS65311-Q1 BUCK1 Compensation Resistor Limitation

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**ABSTRACT**

This application report provides guidelines and recommendations for designing an optimum compensation circuit for the TPS65310A-Q1 and TPS65311-Q1 BUCK1 controller to achieve smooth soft-start during the regulator start-up. This application report also provides insight on the effects of different external components for the regulator on regulator start-up behavior.

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## 1 Introduction

Figure 1 shows the detailed block diagram of the BUCK1 regulator with external components. The device has a *break before make* gate driver to avoid any dead time violations. The high-side (HS) gate-drive buffer is a floating driver switching between the BOOT1 and PH1 pins. The BOOT1 voltage is boosted using the external bootstrap capacitor, and the voltage is approximately equal to PH1 + VREG. The low-side (LS) gate-drive buffer is switched between the VREG and PGND1 pins. The device has a built-in soft-start which limits the output voltage slope during the start-up. The transconductance amplifier ($g_m$) has a traditional, folded-cascode architecture which has a high output impedance.

The BUCK1 controller requires external type-2 compensation network on the COMP1 pin for normal-mode operation. During the BUCK1 start-up, the internal $g_m$ amplifier goes through a large-signal transient behavior. With a large compensation resistor, the gm amplifier output (COMP1) voltage may overshoot during start-up. This overshoot on the COMP1 pin could affect the soft-start behavior of the regulator.

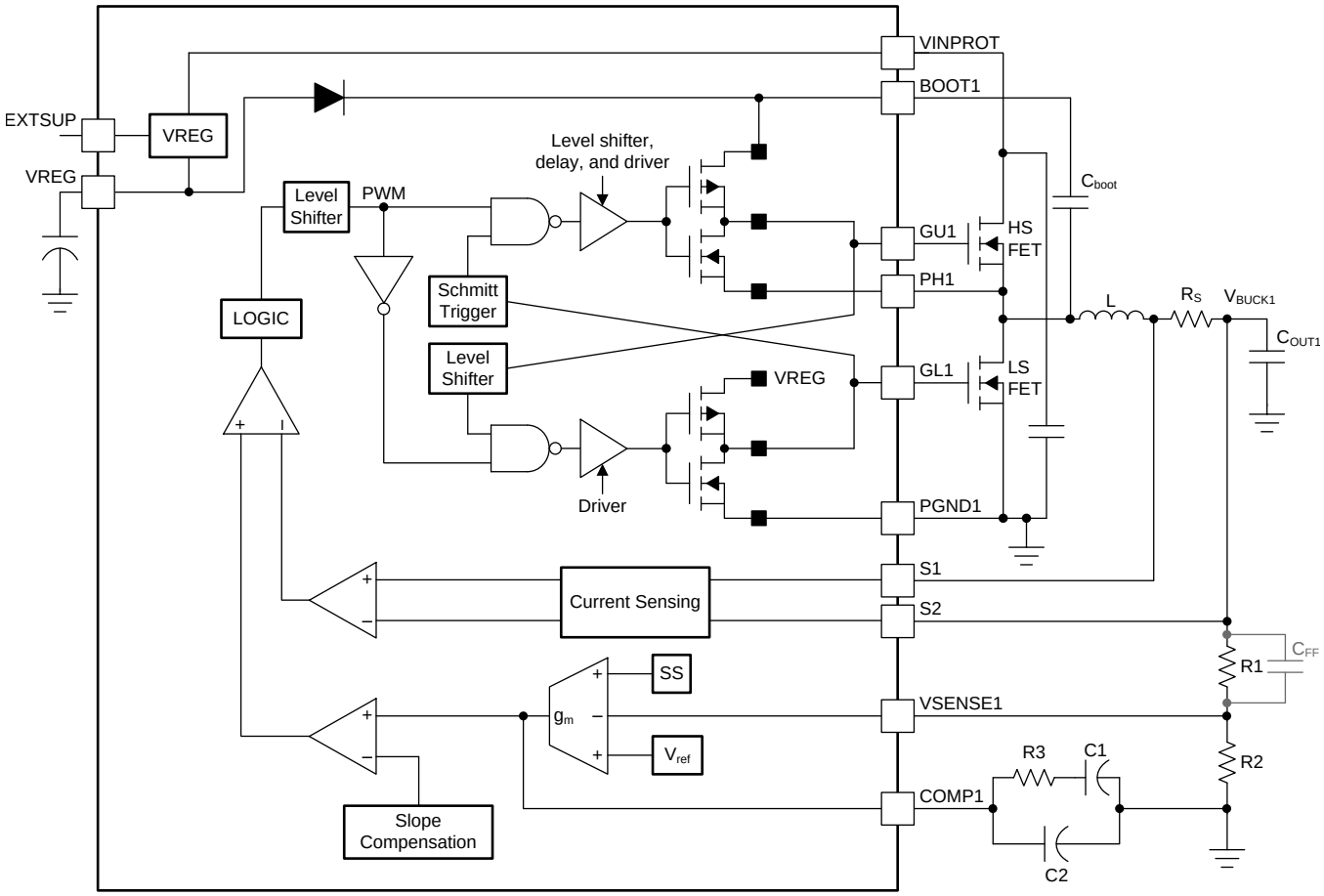





**Figure 1. TPS65310A-Q1 and TPS65311-Q1 BUCK1 Regulator With External Components**

## 2 Compensation Component Calculations

Use Equation 1, Equation 2, and Equation 3 to calculate the BUCK1 compensation components. The value of the R3 resistor is directly proportional to the value of the output capacitor for a given shunt resistor, output voltage, and bandwidth setting.

1. Select a value for the bandwidth, $f_{BW}$, that is between the switching frequency ($f_{SWBUCK1}$) / 6 (faster response) and $f_{SWBUCK1}$ / 10 (more conservative).

$$R3 = \frac{2\pi \times f_{BW} \times V_{OUT1} \times C_{OUT1}}{g_m \times K_{CFB} \times V_{refBUCK}}$$

where

- $C_{OUT1}$ is the load capacitance of BUCK1.
- $g_m$ is the transconductance of the error amplifier (0.9 ms typical).

$K_{CFB}$ = 0.125 / $R_S$ (defined by design)

where

- $R_S$ is the current-sense resistor.
- $V_{refBUCK}$ is the internal reference voltage (0.8 V).

2. Use Equation 2 to select a value for C1 (in series with R3, see Figure 1) to set the zero frequency close to $f_{BW}$ / 10.

$$C1 = \frac{10}{2\pi \times R3 \times f_{BW}} \quad (2)$$

3. Use Equation 3 to select a value for C2 (parallel with R3 and C1, see Figure 1) to set the second pole below $f_{SWBUCK1}$ / 2.

$$C2 = \frac{1}{2\pi \times R3 \times f_{BW} \times 3} \quad (3)$$

For example, $f_{SWBUCK1}$ is 490 kHz, $V_{OUT1}$ is 3.3 V, $V_{refBUCK}$ is 0.8 V, and $f_{BW}$ is 60 kHz. Table 1 lists the calculated compensation component values for different $C_{OUT1}$ and $R_S$ values assuming 25% derating of the output capacitor.

**Table 1. Calculated Compensation-Component Values**

| COMP_CONFIG Number | $C_{OUT1}$ (µF) | $R_S$ (mΩ) | R3 (kΩ) | C1 (nF) | C2 (pF) |
|---|---|---|---|---|---|
| 1 | 50 | 10 | 5.6 | 4.7 | 150 |
| 2 | 100 | 10 | 12 | 2.2 | 82 |
| 3 | 150 | 10 | 16 | 1.5 | 56 |
| 4 | 50 | 20 | 12 | 2.2 | 68 |
| 5 | 100 | 20 | 24 | 1.2 | 39 |
| 6 | 150 | 20 | 36 | 0.68 | 22 |

The exact estimate of the output capacitor derating values and predicting the stability is difficult and therefore these calculations are guidelines only. Stability and load-step response must be verified with measurements on the user's board to optimize the values of the compensation components. Slightly different values could be more optimum for the given application conditions.

## 3 Measurement Setup and Test Conditions

The TPS65310AEVM was used for all the measurements performed in this application report. The TPS65310A-Q1 BUCK1 controller is configured with these conditions:

- Input supply ($V_{IN}$) = 12.5 V, bench-top supply with 4-A DC current limit
- Venable phase analyzer used for measuring the regulator loop response
- $V_{OUT}$ (VBUCK1) = 3.3 V
- R1 = 50 kΩ
- R2 = 16 kΩ

- Inductor (L) = 4.7 µH
- Output capacitor ($C_{OUT1}$) = 50 µF, 100 µF, and 150-µF ceramic
- Current-sense resistor ($R_S$) = 10 mΩ and 20 mΩ
- GPFET is bypassed by shorting the VIN and VINPROT pins with the input LC filter shorted.
- To test the effect of the external FETs (FET2) on the PH1 overshoot at start-up, different FETs (2 single FETs in two different packages) were soldered on the existing footprint without any additional blue wiring to minimize the parasitic effects. FET1 is the default FET (dual FETs in one package) on the TI EVM.

## 4 Stability and Load Transient Measurements

To provide a quick overview of the stability performance of the regulator, measurements were taken for different output capacitors and compensation components combinations listed in Table 1. Table 2 lists the measurement results which show that regulator is stable across different compensation options calculated based on the equations in the data sheet.

**Table 2. Summary of Stability and Load transient Measurements for Calculated Compensation Components**

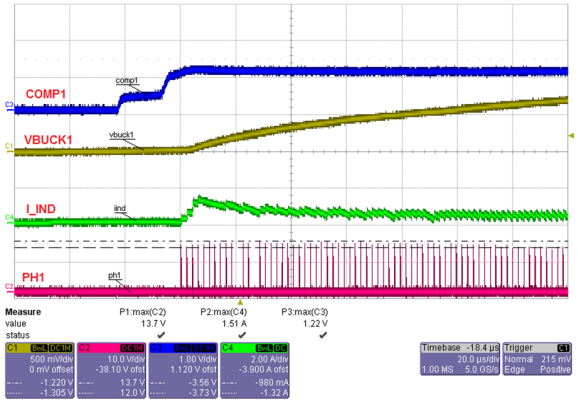
| Compensation Option R3, C1, C2 | $R_S$ (mΩ) | $C_{OUT1}$ (µF) | Bandwidth (kHz) | Phase Margin (Degree) | Gain Margin (dB) | Undershoot (mV) Load Transient 0 A to 2 A in 2 µS |
|---|---|---|---|---|---|---|
| 5.6 kΩ, 4.7 nF, 150 pF | 10 | 50 | 35 | 55 | 15 | 125 |
| 12 kΩ, 2.2 nF, 82 pF | 10 | 100 | 40 | 55 | 10 | 85 |
| 16 kΩ, 1.5 nF, 56 pF | 10 | 150 | 40 | 50 | 10 | 64 |
| 12 kΩ, 2.2 nF, 68 pF | 20 | 50 | 35 | 65 | 15 | 120 |
| 24 kΩ, 1.2 nF, 39 pF | 20 | 100 | 40 | 60 | 15 | 80 |
| 36 kΩ, 680 pF, 22 pF | 20 | 150 | 40 | 55 | 15 | 62 |

## 5 BUCK1 Soft-Start Limitation for Compensation Resistor Greater Than 16 kΩ

The $g_m$ amplifier is a folded-cascode transconductance amplifier with high output impedance. The amplifier acts as a current source with an output current proportional to the input differential voltage. With a limited voltage swing, the output of the $g_m$ amplifier can become saturated if the compensation resistor, R3, is too large. If the value of R3 is too large, the $g_m$ amplifier quickly becomes nonlinear causing an overshoot on the COMP1 pin at start-up. The swing of the $g_m$ amplifier can be forced to be linear by limiting the value of R3 to a maximum of 16 kΩ.

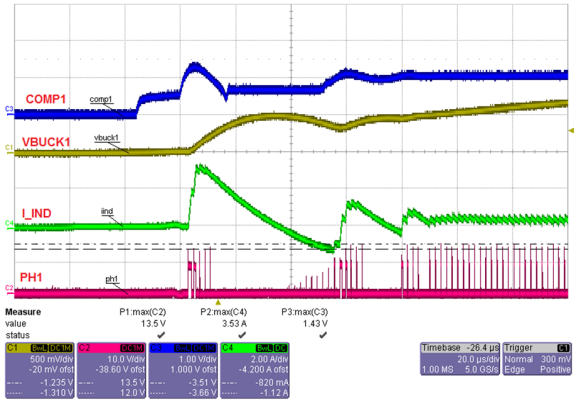
Figure 2 and Figure 3 show the regulator start-up behavior for 16-kΩ R3 and 24-kΩ R3. When the value of R3 is less than or equal to 16 kΩ, the start-up of the VBUCK1 output voltage is smooth and no significant inductor current occurs during the start-up. When the value of R3 is 24 kΩ, the VBUCK1 output voltage shoots up because the overshoot that occurs on the COMP1 pin, and the inductor current is significantly larger compared to the normal start-up.

The BUCK2, BUCK3, BOOST and LDO regulators of this device are not affected by this limitation on BUCK1.




$C_{OUT1}$ = 100 µF $R_S$ = 10 mΩ C1 = 1.5 nF
C2 = 56 pF

**Figure 2. Regulator Startup Behavior With 16-kΩ R3**

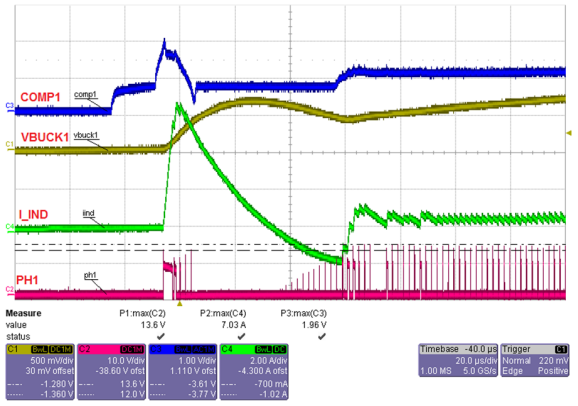



$C_{OUT1}$ = 100 µF $R_S$ = 10 mΩ C1 = 1.5 nF
C2 = 56 pF

**Figure 3. Regulator Startup Behavior With 24-kΩ R3**

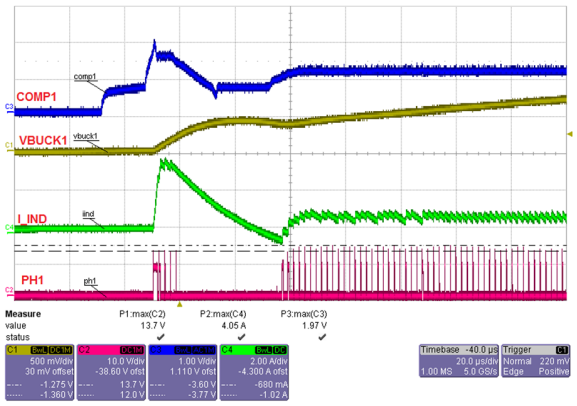
Figure 3 shows a slight oscillation behavior occurring on the COMP1 pin as this compensation case had poor stability margins.

The amount of COMP1 pin overshoot and inductor inrush current depends on many application conditions such as the value of the shunt resistor, compensation resistor, output capacitor, and other components. Figure 4 and Figure 5 shows the behavior for different compensation components, $C_{OUT1}$, and $R_S$.




$C_{OUT1}$ = 150 µF C1 = 680 pF C2 = 22 pF

**Figure 4. Regulator Start-Up Behavior With 36-kΩ R3 and 10-mΩ $R_S$**




$C_{OUT1}$ = 150 µF C1 = 680 pF C2 = 22 pF

**Figure 5. Regulator Startup Behavior With 36-kΩ R3 and 22-mΩ $R_S$**

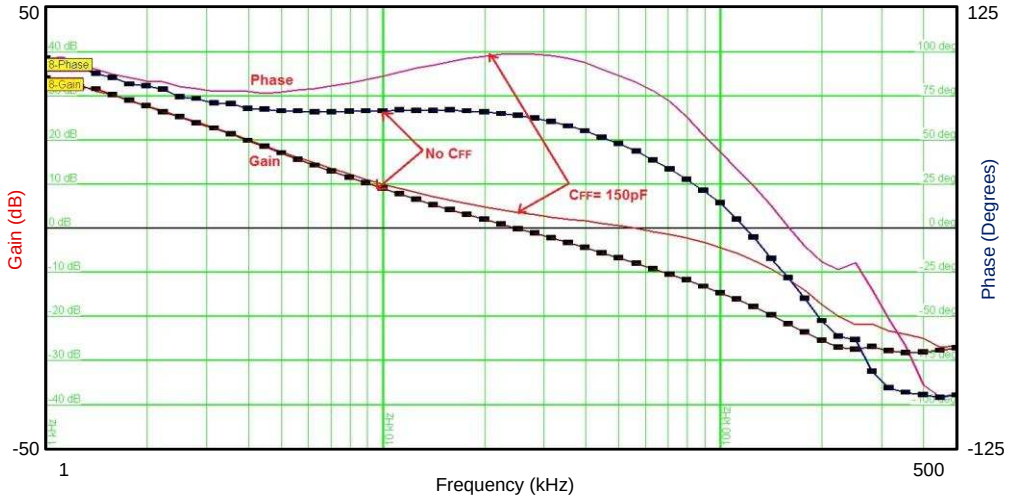
## 6 Effect of Feedforward Capacitor on Bandwidth and Phase Margin

To slightly improve the regulator bandwidth, add a small feedforward capacitor ($C_{FF}$) across the top feedback divider resistor (R1). This feedforward capacitor is selected to provide a zero around the desired crossover frequency with R1. Use Equation 4 to calculate the value of of $C_{FF}$.

$$C_{FF} = \frac{1}{2 \times 3.14 \times R1 \times f_{BW}} \quad (4)$$

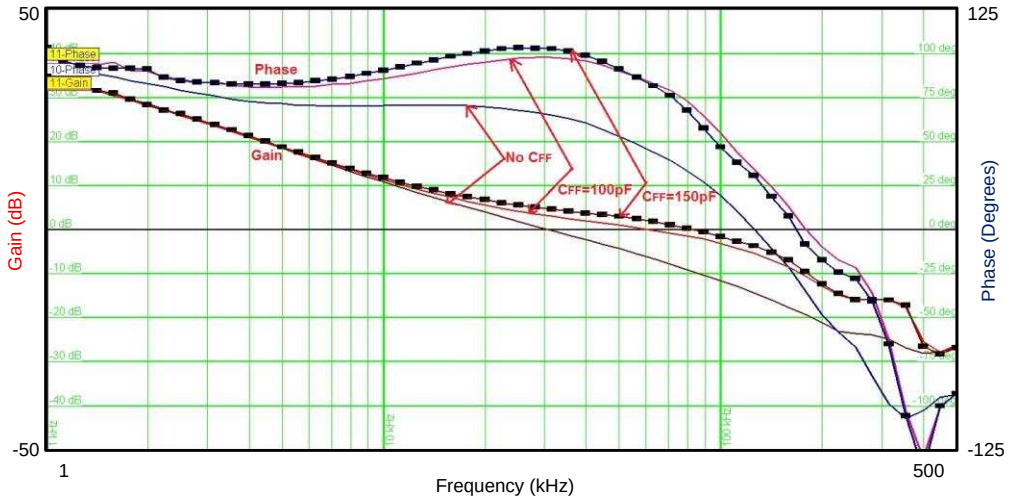
Figure 6, Figure 7, and Figure 8 show that the feedforward capacitor improves the bandwidth and the phase margin. Figure 9 and Figure 10 show that the optimum feedforward capacitor reduces the undershoot and overshoot during load transients by increasing the regulator bandwidth.

Keep the value of this capacitor as small as possible as a large feedforward capacitor will affect the phase margin and gain margin, and create stability issues. The feedforward capacitor must always be optimized based on the actual measurements. Figure 7 ($C_{FF}$ = 150 pF), Figure 8 ($C_{FF}$ = 100 pF), and Figure 11 show the effect of a large feedforward capacitor. In Figure 11, considerable ringing can be observed at the falling edge of load transient indicating lower phase margin and stability issues.



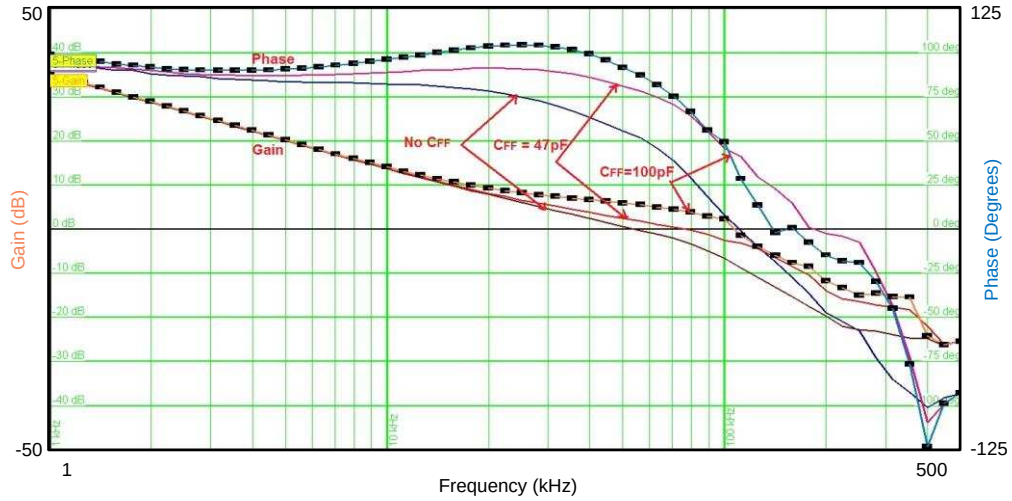

$C_{OUT1}$ = 150 µF $R_S$ = 20 mΩ R3 = 16 kΩ
C1 = 1.5 nF C2 = 56 pF

**Figure 6. Stability Plot With and Without Feedforward Capacitor for 150-µF $C_{OUT1}$ and 20-mΩ $R_S$**



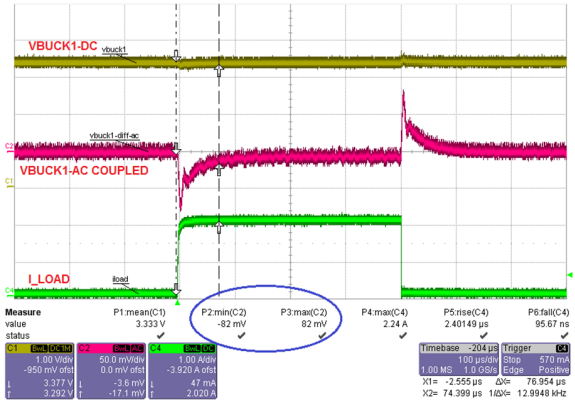

$C_{OUT1}$ = 100 µF $R_S$ = 20 mΩ R3 = 16 kΩ
C1 = 1.5 nF C2 = 56 pF

**Figure 7. Stability Plot With and Without Feedforward Capacitor for 100-µF $C_{OUT1}$ and 20-mΩ $R_S$**



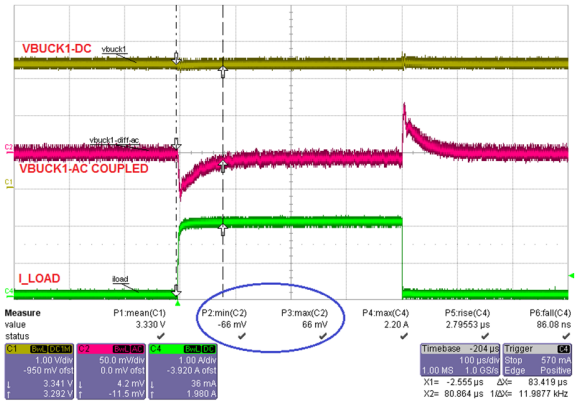

$C_{OUT1}$ = 100 µF $R_S$ = 10 mΩ R3 = 16 kΩ
C1 = 1.5 nF C2 = 56 pF

**Figure 8. Stability Plot With and Without Feedforward Capacitor for 100-µF $C_{OUT1}$ and 10-mΩ $R_S$**



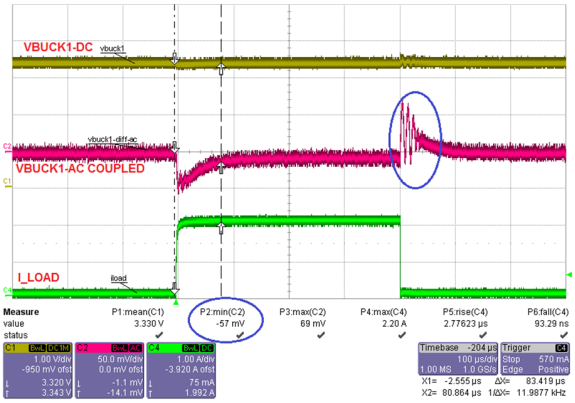

$C_{OUT}$ = 100 µF $R_S$ = 10 mΩ R3 = 16 kΩ
C1 = 1.5 nF C2 = 56 pF

**Figure 9. Load Transient Plot Without $C_{FF}$ for 100-µF $C_{OUT1}$ and 10-mΩ $R_S$**




$C_{OUT}$ = 100 µF $R_S$ = 10 mΩ R3 = 16 kΩ
C1 = 1.5 nF C2 = 56 pF $C_{FF}$ = 47 pF

**Figure 10. Load Transient Plot With 47-pF $C_{FF}$ for 100-µF $C_{OUT1}$ and 10-mΩ $R_S$**




$C_{OUT}$ = 100 µF $R_S$ = 10 mΩ R3 = 16 kΩ
C1 = 1.5 nF C2 = 56 pF

**Figure 11. Load Transient Plot With 100-pF $C_{FF}$ for 100-µF $C_{OUT1}$ and 10-mΩ $R_S$**

Because the value of R3 must be 16 kΩ or less to achieve smooth start-up, the value of R3 was set to 16 kΩ and regulator performance was optimized by adjusting the feedforward capacitor. Table 3 lists the stability and load transient results for the optimized regulator. In Table 3, the S. No. 1, 4, and 7 are results based on the calculated compensation circuit. The S. No. 3, 6, and 9 are results with the compensation resistor set to 16 kΩ with an optimized feedforward capacitor and these results show improved regulator performance compared to the calculated compensation circuit. However, tests were performed based only on limited application conditions and users must verify the behavior on their board.

**Table 3. Stability and Load Transient Results for the Optimized Regulator With R3 = 16 kΩ**

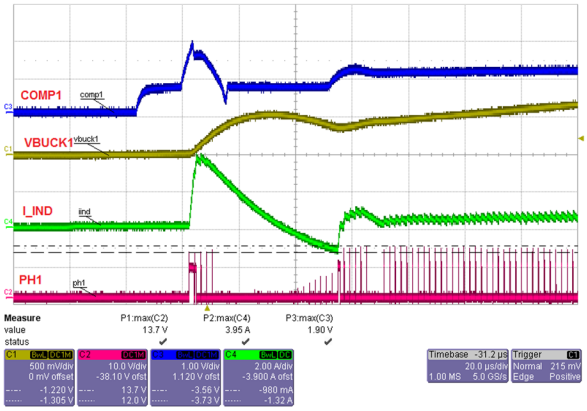
| S. No. | COMP1 Component Values R3, C1, C2, $C_{FF}$ | $R_S$ (mΩ) | $C_{OUT1}$ (µF) | Bandwidth (KHz) | Phase Margin (Degree) | Gain Margin (dB) | Undershoot (mV) Load Transient 0 A to 2 A in 2 µS |
|---|---|---|---|---|---|---|---|
| 1 | 12 kΩ, 2.2 nF, 82 pF, no $C_{FF}$ | 10 | 100 | 40 | 55 | 10 | 85 |
| 2 | 16 kΩ, 1.5 nF, 56 pF, no $C_{FF}$ | 10 | 100 | 52 | 50 | 10 | 82 |
| 3 | 16 kΩ, 1.5 nF, 56 pF, $C_{FF}$ = 47 pF | 10 | 100 | 75 | 65 | 10 | 66 |
| 4 | 24 kΩ, 1.2 nF, 39 pF, no $C_{FF}$ | 20 | 100 | 40 | 60 | 15 | 80 |
| 5 | 16 kΩ, 1.5 nF, 56 pF, no $C_{FF}$ | 20 | 100 | 30 | 100 | 15 | 85 |
| 6 | 16 kΩ, 1.5 nF, 56 pF, $C_{FF}$ = 100 pF | 20 | 100 | 60 | 80 | 10 | 65 |
| 7 | 36 kΩ, 680 pF, 22 pF, no $C_{FF}$ | 20 | 150 | 40 | 55 | 15 | 62 |
| 8 | 16 kΩ, 1.5 nF, 56 pF, no $C_{FF}$ | 20 | 150 | 25 | 65 | 18 | 78 |
| 9 | 16 kΩ, 1.5 nF, 56 pF, $C_{FF}$ = 150 pF | 20 | 150 | 55 | 80 | 10 | 54 |

## 7 Guidelines for Selecting Compensation Capacitors (C1 and C2)

The value of the compensation resistor, R3, is calculated first. Then, based on the value of R3, the values of the compensation capacitors (C1 in series with R3 and C2 connected between COMP1 and GND) are calculated. The C1 capacitor adds a pole to compensate for the $g_m$ amplifier zero. The value of the C1 capacitor can be adjusted in a small range to optimize regulator performance. A smaller value provides slightly higher gain and bandwidth at the expense of phase margin. For the stability plots across three different values of C1, see Figure 13.

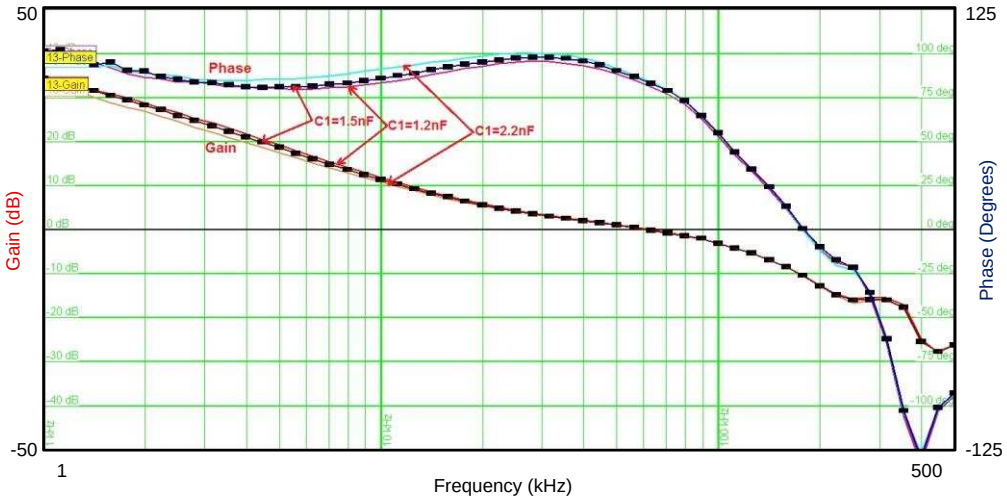
Too small value, such as 680 pF, could affect the performance of the $g_m$ amplifier and, therefore, TI recommends keeping the value of this capacitor between 1.2 nF and 6.8 nF.

Figure 12 shows the effect of 16-kΩ R3 and 680-pF C1. In this case, COMP1 overshoot occurs during start-up.




$C_{OUT1}$ = 100 µF $R_S$ = 10 mΩ R3 = 16 kΩ
C1 = 680 pF C2 = 56 pF

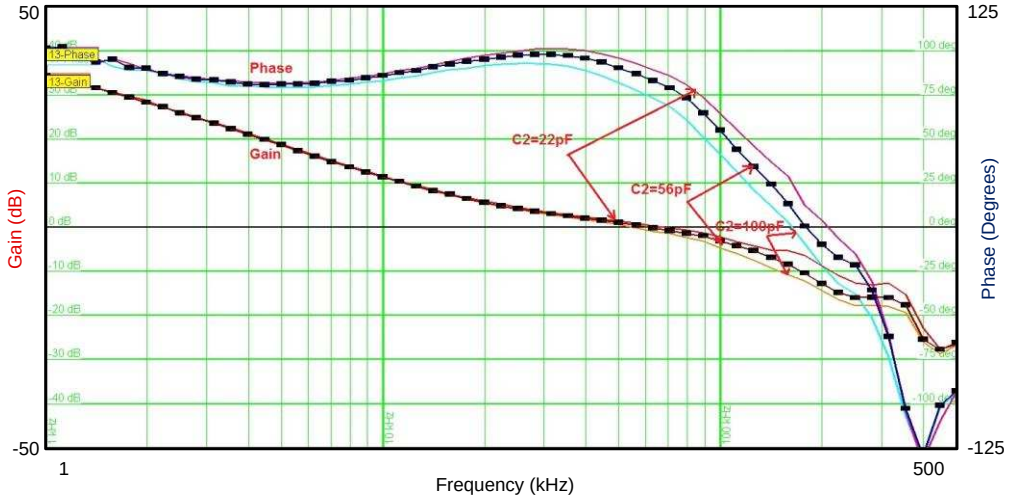
**Figure 12. Effect of Too Small Compensation Capacitor**




$C_{OUT1}$ = 100 µF $R_S$ = 20 mΩ R3 = 16 kΩ
C2 = 56 pF $C_{FF}$ = 100 pF

**Figure 13. Stability Plots Across Three Different C1 Values**

The value of the C2 capacitor can be adjusted in a small range to optimize regulator performance. A smaller value provides slightly higher gain and bandwidth at the expense of phase margin. Keep the values close to the calculated value. For the stability plots across three different values of C2, see Figure 14.

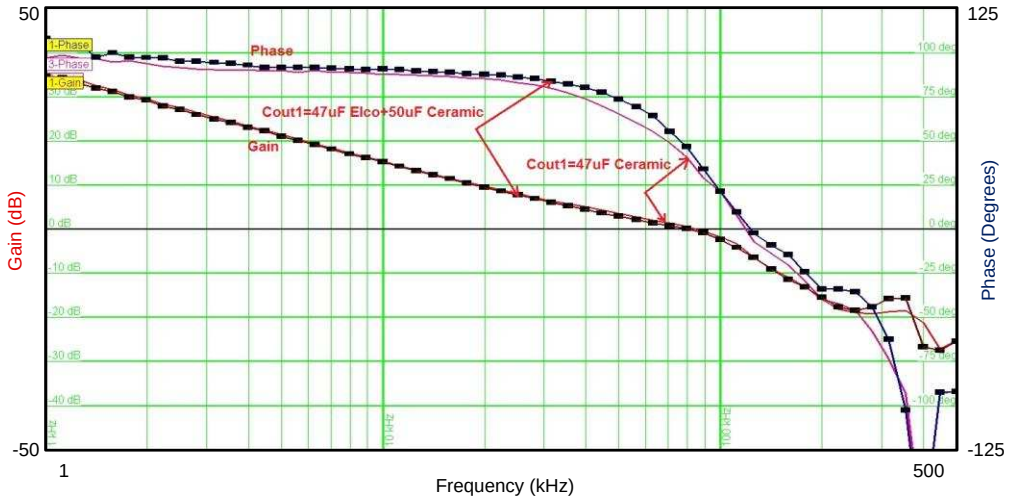



$C_{OUT1}$ = 100 µF $R_S$ = 20 mΩ R3 = 16 kΩ
C1 = 1.5 nF $C_{FF}$ = 100 pF

**Figure 14. Stability Plots Across Three Different C2 Values**

## 8 Effect of Different Types of Output Capacitors on Stability

Ceramic output capacitors have very small ESR (3 mΩ to 5 mΩ typical) and electrolytic capacitors typically have much larger ESR. The capacitor ESR has certain influence on the regulator stability and must be considered during the calculation and validation of the compensation components. For example, shows the stability plot with a 50-µF ceramic output capacitor and a combination of a ceramic capacitor and electrolytic capacitor which had a dissipation factor of approximately 0.25. The addition of the electrolytic capacitor did not affect the stability plot. In this case, the compensation circuit calculated, considering the total capacitance (100 µF) would result in unstable regulator.



## 9 Effect of Different Switching FETs on SW Node Overshoot

During start-up with compensation resistors larger than 16 kΩ, the PH1 pin has wide pulses followed by narrow pulses for a short period of time because of the COMP1 overshoot. This pulsing results in large inrush current on the inductor. This transient behavior along with the external switching-FET characteristics could result in significant shoot-through current. Along with the parasitic inductance of the board, this large shoot-through current could cause significant overshoot on the PH1 pin. For higher input voltages, these large overshoots are significant enough to exceed the absolute maximum rating of the PH1 and BOOT1 pins. This behavior should be verified during the design validation phase to make sure that no significant overshoot occurs on the PH1 and BOOT1 pins. At cold temperature conditions, semiconductor devices switch faster and parasitic inductance effect is worse. Therefore, cold temperature conditions are typically worse for such effects.

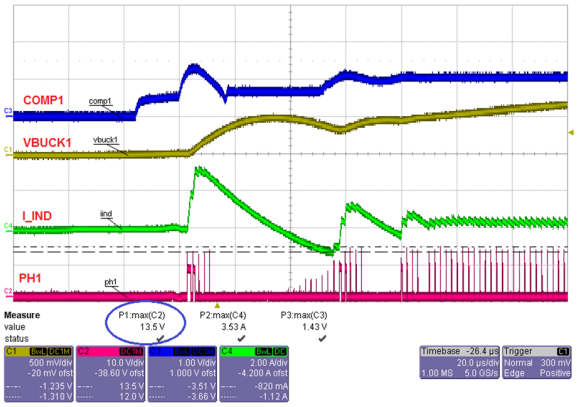
Follow these guidelines to improve the PH1 overshoot during start-up:

- TI recommends minimizing the parasitic inductance of the board in the switching path, and place the ceramic decoupling capacitors of different values very close to the drain of the high-side switching FET. Keep the ground connection (PGND1 pin) of these decoupling capacitors very short to reduce the parasitic inductance in the ground path.
- Placing an RC snubber at the PH1 pin helps reduce the ringing which helps to reduce the PH1 overshoot.
- Verify that the switching FETs do not have shoot-through issues caused by reverse recovery effects or the turnon and turnoff delay effects of the switching FETs.
- A small gate resistor can help reduce the shoot-through effects by slowing down the edges. However these gate resistors affect the efficiency and turnon and turnoff delays. Therefore these resistors must be carefully selected with detailed validation.

In the case shown in Figure 16, one 2.2-µF HS FET, drain-decoupling capacitor was soldered directly across drain of the HS FET and source of the LS FET. One 2.2-µF drain capacitor was also placed on the underside of the printed circuit board (PCB), just below the drain of the HS FET with a short connection to the PGND1 pin.

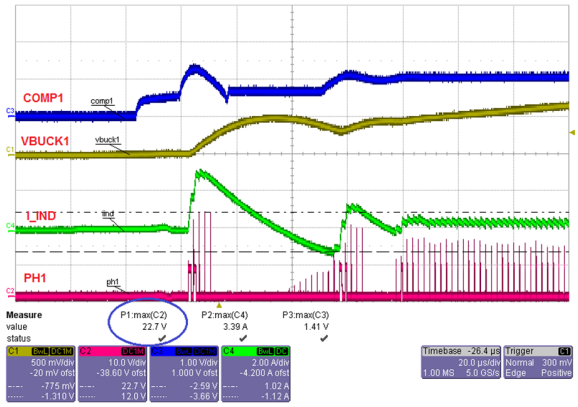
Figure 17 has the same decoupling capacitors as Figure 16, but different switching FETs (FET2) were soldered.

The two different FETs had a difference in the PH1 pin overshoot of approximately 9 V.




$C_{OUT1}$ = 100 µF $R_S$ = 10 mΩ R3 = 24 kΩ
C1 = 1.2 nF C2 = 56 pF

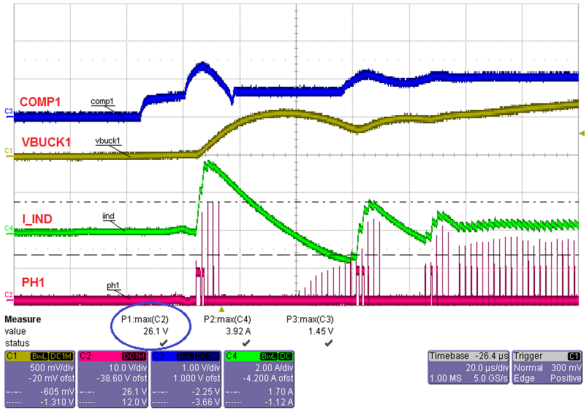
**Figure 16. Startup Waveform With FET1 and Two 2.2-µF Drain Capacitors**




$C_{OUT1}$ = 100 µF $R_S$ = 10 mΩ R3 = 24 kΩ
C1 = 1.2 nF C2 = 56 pF

**Figure 17. Startup Waveform With FET2 and Two 2.2-µF Drain Capacitors**

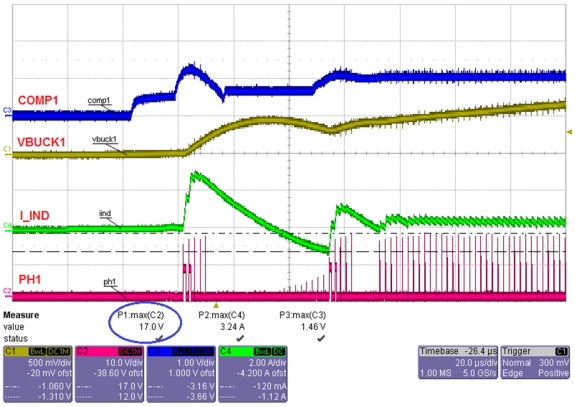
Figure 18 was also taken with the same setup used in Figure 17. In this case, cold spray was applied and the temperature was approximately –20°C to 0°C. With this PH1 overshoot, the voltage increased by approximately 3.5 V.




$C_{OUT1}$ = 100 µF $R_S$ = 10 mΩ R3 = 24 kΩ
C1 = 1.2 nF C2 = 56 pF

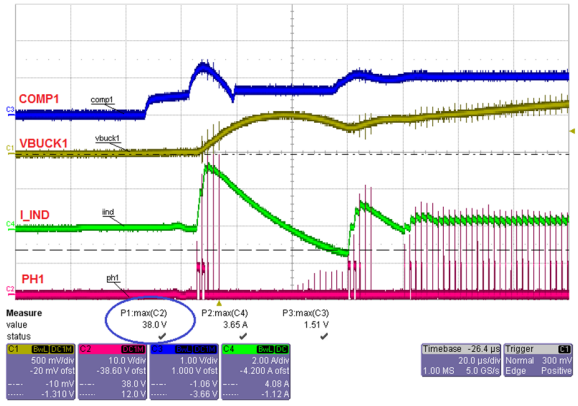
**Figure 18. Startup Waveform With FET2 and Two 2.2-µF Drain Capacitors at Cold Temperature**

In the case shown in Figure 19 and Figure 20, only one 2.2-µF drain capacitor was placed on the underside of the PCB, just below the drain of the high-side FET with a short connection to the PGND1 pin. The PH1 overshoot with FET2 increased significantly (17 V with FET1 and 38 V with FET2), indicating large shoot-through current through FET2. In this case, even a small parasitic inductance caused large overshoot. Adding a 10-Ω gate resistor completely eliminated overshoots. Figure 21 was taken with the same test conditions as Figure 20, but with 10-Ω gate resistors.



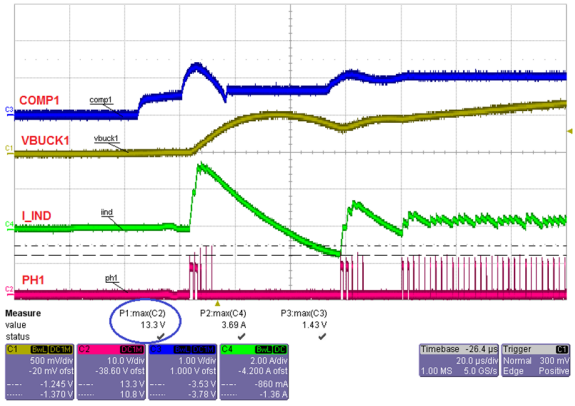

$C_{OUT1}$ = 100 µF $R_S$ = 10 mΩ R3 = 24 kΩ
C1 = 1.2 nF C2 = 56 pF

**Figure 19. Startup Waveform With FET1 and One 2.2-µF Drain Capacitor**




$C_{OUT1}$ = 100 µF $R_S$ = 10 mΩ R3 = 24 kΩ
C1 = 1.2 nF C2 = 56 pF

**Figure 20. Startup Waveform With FET2 and One 2.2-µF Drain Capacitor**




$C_{OUT1}$ = 100 µF $R_S$ = 10 mΩ R3 = 24 kΩ
C1 = 1.2 nF C2 = 56 pF

**Figure 21. Startup Waveform With FET2, One 2.2-µF Drain Capacitor, and 10-Ω Gate Resistors**

## 10 Conclusion

The following conclusions can be made:

- The BUCK1 regulator of the TPS65310A-Q1 and TPS65311-Q1 devices shows a start-up overshoot on the COMP1 pin for a short time when the compensation resistor is more than 16 kΩ because of the limited current through the $g_m$ amplifier output. This overshoot affects the soft-start behavior of the regulator during start-up.
- When the COMP1 overshoot occurs during start-up, the inductor current could reach the current limit level. However, this overshoot occurs only for a short period of time (less than 20 µs). With this short overshoot period, BUCK1 regulator shutdown is not a risk because of overcurrent detection. The typical filter time for BUCK1 current-limit detection to the error state is 1 ms and if the current limit duration is less than this time, the device will not reset.
- With compensation resistors larger than 16 kΩ, during normal operation, COMP1 overshoot behavior was not observed because during the normal operation, the COMP1 pin does not make a large step from 0 V to 1 V. However, for optimum soft-start behavior, TI recommends limiting this resistor value to less than or equal to 16 kΩ.
- A suitable feed-forward capacitor can be used to improve the bandwidth.
- Users must verify the stability and load transient behavior on their board across temperature as regulator performance can vary across temperature.
- Careful selection of external switching FETs, careful PCB layout design, and placement of external components to minimize the parasitic effects are necessary to reduce the overshoot on the PH1 pin.
- An RC snubber on the PH1 pin and gate resistors can be used to further minimize the ringing and overshoot. However, these methods affect the efficiency. Gate resistors affect the turnon and turnoff delay of the external FETs and also a voltage drop occurs across these resistors because of transient switching currents. Therefore detailed measurements are necessary to optimize the snubber and gate resistor values.

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