

TPS659037 Design Guide

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ABSTRACT

This application note provides guidance on schematic design and can be used as a design review of applications using the TPS659037 power management IC (PMIC). This document describes recommended external components, recommended connections of select signals, and contains a design checklist. Prior to using this guide, TI recommends reading the user's guide, *TPS659037 User's Guide to Power AM572x and AM571x* ([SLIU011](#)) and select an OTP version, because the schematic design is dependent on the OTP configuration of the device.

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1 Introduction

The TPS659037 PMIC is an integrated device used to power a system-on-chip (SoC). The device contains 9 DC-DC switching converters combined in 7 output rails and 7 low-dropout (LDO) regulators. The device also includes control signals for operation in various modes. This guide includes information on the recommended external connections for each ball of the IC to assist in the schematic design of a system using the TPS659037 device.

The TPS659037 device utilizes one-time-programmable (OTP) memory to store configuration information for the device, including configuration of GPIO pins, polarity of inputs, boot voltages, power sequence, and some other functions. The TPS659037 user's guide describes this information for both configurations of TPS659037. The OTP version that will be used in the system must be known before completing the schematic design.

A link to the design checklist in Excel® format is provided in [Section 3](#) which provides a different view of this information.

2 Design Guide

2.1 Supply Voltages

2.1.1 VCC1

The supply voltage to the PMIC should be a regulated voltage between 3.3 V and 5 V (nominal). During operation, the supply voltage should not be higher than 5.25 V or lower than 3.135 V, which allows for 5% tolerance from 5 V and 3.3 V (nominal) respectively.

Using a 10- μ F decoupling capacitor at the VCC1 pin is recommended.

2.1.2 VIO_IN

The VIO_IN regulated supply voltage to the PMIC input should be 1.8 V or 3.3 V. The VIO_IN supply should be the same supply to the SoC I/O and other I/O voltages on the system. If the VIO_IN supply is 3.3 V, it should be supplied by a switched 3.3-V supply external to the PMIC, or a 3.3-V SMPS output from the PMIC, depending on the OTP. If the VIO_IN supply is 1.8 V, then it should be connected to the first sequenced 1.8-V rail, which is typically SMPS8 or LDO2 depending on the OTP.

The VIO_IN pin should not have the same supply as the VCC1 pin. If the VIO_IN and VCC1 pins are supplied by the same voltage, then the output buffers on VIO_IN signals (for example, INT, GPIO_4, or GPIO_6) can be activated for a short period when the supply ramps, before the OTP is loaded.

Using a 100-nF decoupling capacitor at the VIO_IN pin is recommended.

2.1.3 Ground Connections (GND_ANA, GND_DIG, VIO_GND, PBKG)

Each group of ground pins should be connected to each other. For example, the GND_ANA pins should be connected, the GND_DIG pins should be connected, and so on. Each ground connection should then be connected to a common ground plane at one point.

2.2 SMPS Regulators

2.2.1 SMPS Input Pins (SMPSx_IN)

All SMPS input pins must be supplied by the same supply as the VCC1 pin. Each input should have a 4.7- μ F decoupling capacitor very close to the SMPS input pin. If the regulator is unused, the input supply should still be present, but the decoupling capacitor is not required.

2.2.2 SMPS Switch Nodes (SMPSx_SW)

Each SMPS output should be connected to a 1- μ H inductor, and the output of the inductor connected to a 47- μ F capacitor.

NOTE: The total capacitive load per phase should not exceed 57 μ F, including decoupling capacitors at the load. Reduce the output capacitance to a minimum of 20 μ F if required.

The saturation current of the inductor should exceed the current limit of the SMPS, including that of the ripple current. If the regulator is unused, the switch node should be left floating.

Each SMPS is configured to supply a specific SoC domain based on the boot voltage and power sequence slot. To determine which SoC domain the SMPS should supply, refer to the TPS659037 user's guide.

2.2.3 SMPS Feedback Pins (SMPSx_FDBK, SMPSx_FDBK_GND)

To compensate for the voltage drop due to the resistance of the PCB trace, each SMPSx_FDBK pin should be connected to the output voltage at the load. The SMPS12 and SMPS45 pins offer differential remote feedback, therefore the SMPSx_FDBK_GND lines for the SMPS12 and SMPS45 pins should be routed to the GND pin at the SoC.

2.2.4 SMPS Ground Pins (SMPSx_GND)

Each SMPSx_GND pin should be connected together, and this ground should be connected to a common ground plane at one point.

2.3 LDO Regulators

2.3.1 LDO Input Pins (LDOx_IN)

Each LDO input pin should be connected to a preregulated supply. The LDOUSB regulator has two input supplies, and both should be supplied with a valid voltage. Refer to the data sheet, *TPS659037 Power Management Unit (PMU) for Processor (SLIS165)*, for the supply voltage range for each LDO. The input voltage should also be higher than the output voltage plus maximum dropout.

NOTE: Some inputs are shared (for example, LDO12_IN powers both LDO1 and LDO2), and therefore the input voltage must be able to power both regulators.

Each LDO input pin should have a 2.2- μ F capacitor connected to the input supply that is ideally placed close to the IC pin. If any LDO is unused, the input pin should still be supplied, but the 2.2- μ F capacitor is not required.

The supply for each LDO must be available before the LDO is turned on in the sequence, otherwise the LDO will detect a short circuit and remain off.

2.3.2 LDO Output Pins (LDOx_OUT)

Each LDO output should have a 2.2- μ F capacitor at the output. Each LDO output is configured to supply a specific SoC domain based on the boot voltage and power sequence slot. To determine which SoC domain the LDO output should supply, refer to the TPS659037 user's guide.

LDOVANA and LDOVRTC are internal regulators, and require a 2.2- μ F output capacitor. If either LDO regulator is not connected to anything externally, the output pin only requires the 2.2- μ F capacitor.

2.3.3 LDO Supply (LDO_SUPPLY)

The TPS659037 device has three LDO_SUPPLY pins. These pins are used for ESD cell supplies, and should be connected to the VCC1 supply.

2.4 ADC Pins

2.4.1 GPADC Inputs (GPADC_INx)

The GPADC has three input channels which can be used to measure an analog voltage. Refer to the TPS659037 data sheet for the input voltage range for each channel. If the channel is unused, it should be connected to GND.

2.4.2 GPADC Reference (GPADC_VREF)

The GPADC voltage reference can be used when using the GPADC_IN1 pin and a NTC thermistor to measure system temperature. In this case, the GPADC voltage reference can be connected to GPADC_IN1 through a resistor. If the GPADC voltage reference is not used, the GPADC_VREF pin should be left floating.

2.5 Clocking Pins

2.5.1 OSC16MIN, OSC16MOUT, OSC16MCAP

The connection of the oscillator pins depends on the setting of the OTP bit, OSC16M_CFG. When the OSC16M_CFG bit is set to 0, the oscillator is enabled and the OSC16MIN and OSC16MOUT pins should have a 16.384-MHz crystal connected between them. The load capacitors of both OSC16MIN and OSC16MOUT pins depend on crystal specifications, typically 10 pF to 12 pF. The OSC16MCAP pin should be connected to a 2.2- μ F capacitor. If the OSC16M_CFG bit is set to 0, a crystal must be populated, otherwise the device will not operate correctly.

When the OSC16M_CFG bit is set to 1, the oscillator is bypassed, therefore no crystal should be populated. In this case, the OSC16MIN pin should be connected to GND, and the OSC16MOUT and OSC16MCAP pins should both be floating.

2.5.2 CLK32KGO

The CLK32KGO signal can only be controlled through OTP. Refer to the TPS659037 user's guide to see if the CLK32KGO signal is enabled in the specific configuration that is used. If the CLK32KGO signal is used, it should be connected based on the recommendation in the TPS659037 user's guide. If the CLK32KGO signal is unused, it should be left floating.

2.5.3 SYNCDCDC

If the TPS659037 device is synchronized to an external clock, this clock signal should be connected to the SYNCDCDC pin. If the internal 2.2-MHz clock is used, the SYNCDCDC pin should be connected to GND.

2.6 System Control Signals

2.6.1 Power-on Signals (PWRON, RPWRON, GPIO_7)

The PMIC can be turned on using three different methods: PWRON, RPWRON, and GPIO_7 (if configured to POWERHOLD in OTP). One of these signals must be used to turn on the PMIC. PWRON and RPWRON are active-low signals. When the PMIC is on, the DEV_ON bit must be set to 1 by I²C within 8 seconds or else the PMIC will shut off. If this method is used to turn on the PMIC, then PWRON, RPWRON, or both should be connected to a push-button which shorts the pin to GND when pressed. If either or both are unused, they can remain floating.

If GPIO_7 is configured as POWERHOLD, it can be used as a level-sensitive ON-OFF signal. When GPIO_7 is set to 1.8 V, the PMIC will turn on, and when GPIO_7 is set to GND, it will turn off. If GPIO_7 is used to turn the PMIC on, then GPIO_7 should be connected to a 1.8-V enable or disable signal that is active when the PMIC is off. If the PMIC should always remain on, GPIO_7 can be connected directly to LDOVRTC_OUT. If GPIO_7 is unused, it should be connected to GND.

PWRON and RPWRON are both in the VSYS domain, therefore if they are externally pulled up, they should be pulled up to VCC1 voltage. GPIO_7 is in the VRTC domain but is tolerant up to 5.25 V, which means a high-level logic on GPIO_7 should be between 1.8 V and 5.25 V.

2.6.2 PMIC Reset Signals (RESET_IN, PWRDOWN)

The RESET_IN and PWRDOWN pins can both be used to reset the PMIC. Typically RESET_IN is active low, meaning the device is reset when RESET_IN is low, while PWRDOWN is active high, meaning the device is reset when PWRDOWN is high. Refer to the TPS659037 user's guide for OTP programming of polarity and pull-down configuration for the RESET_IN and PWRDOWN pins. If either RESET_IN or PWRDOWN pin is used, it should be connected to a reset signal on the system that can disable and enable the PMIC, and therefore not come from the SoC itself. If either pin is unused, it should be set to the inactive state, typically high for RESET_IN and floating or GND for PWRDOWN.

Both RESET_IN and PWRDOWN are in the VRTC domain but are tolerant up to 5.25 V, which means the high-level logic for the RESET_IN and PWRDOWN pins should be between 1.8 V and 5.25 V.

2.6.3 BOOT0, BOOT1

The function of each BOOT pin is described in the TPS659037 user's guide. Each BOOT pin should be connected to LDOVRTC_OUT or GND depending on the desired functionality. TI recommends placing a pad for a 0-Ω resistor from each BOOT pin to both GND and LDOVRTC_OUT. In addition, each BOOT pin should only populate the desired resistor. Placing the 0-Ω resistor pads allows flexibility in case the BOOT options require changing.

2.6.4 ENABLE1

If ENABLE1 is used to control regulator states within the PMIC, it should be connected to a digital signal in the VIO domain that is the same voltage as VIO_IN. If ENABLE1 is unused, it can remain floating or be connected to the same supply as VIO_IN.

2.6.5 General Purpose I/Os (GPIOx)

The TPS659037 device has eight GPIO pins which have multiple functions multiplexed into each pin. Refer to the TPS659037 user's guide for the default configuration of each GPIO pin. Refer to the TPS659037 data sheet for the recommended connection for each GPIO pin in the default state if it is unused, as well as the voltage domain. This information is also shown in [Table 1](#).

Table 1. GPIO Functions

Functionality	Voltage Domain	Connection if Unused
GPIO_0	VRTC (5.25-V tolerant)	Ground
GPIO_1	VSYS (VCC1)	Ground
VBUSDET (GPIO_1)		Floating
GPIO_2	VSYS (VCC1)	Floating (or Ground)
REGEN2 (GPIO_2)		Floating
GPIO_3	VRTC (5.25-V tolerant)	Ground
GPIO_4	VIO	Ground
SYSEN1 (GPIO_4)		Floating
GPIO_5	VRTC	Ground
CLK32KGO1V8 or SYNCCLKOUT (GPIO_5)		Floating
GPIO_6	VIO	Ground
SYSEN2 (GPIO_6)		Floating
GPIO_7	VRTC (5.25-V tolerant)	Ground
POWERHOLD (GPIO_7)		Ground

2.6.6 I²C and SPI pins (I2C1_SCL_SCK, I2C1_SDA_SDI, I2C2_SDA_SDO, I2C2_SCL_SCE)

The TPS659037 device is configured in I²C mode or SPI mode based on the I2C_SPI OTP bit as described in the TPS659037 user's guide. For example, when configured in I²C mode, the following must occur:

- I2C1_SCL_SCK should be connected to the master I²C clock line.
- I2C1_SDA_SDI should be connected to the master I²C data line.

Both I2C1_SCL_SCK and I2C1_SDA_SDI pins should be pulled up to the VIO voltage. I2C2 can optionally be used for a dedicated I²C bus to control AVS voltages.

If I2C2 is used, the following must occur:

- I2C_SCL_SCE should be connected to the master I²C clock line.
- I2C2_SDA_SDO should be connected to the master I²C data line.

If I2C2 is unused, both I2C_SCL_SCE and I2C2_SDA_SDO lines should be either pulled up to VIO, or connected to the I2C1 lines.

If the TPS659037 device is configured in SPI mode, the following must occur:

- I2C1_SCL_SCK should be connected to the master SPI clock line.
- I2C1_SDA_SDI should be connected to the master SPI data-out or slave data-in line.
- I2C2_SDA_SDO should be connected to the master SPI data-in or slave data-out line.
- I2C2_SCL_SCE should be connected to the master SPI chip enable signal.

2.6.7 INT

The INT pin should be connected to the interrupt input of the SoC. If unused, the INT pin can remain floating, although it is recommended to use this pin so the SoC can be notified of any faults, including short circuit output and overtemperature, among others. The default selection of unmasked interrupts is defined by OTP, and can be found in the TPS659037 user's guide.

2.6.8 NRESWARM

The NRESWARM pin should be connected to the warm reset output of the SoC. The NRESWARM pin is in the VRTC domain, therefore a high-level logic should be between 1.3 V and 1.85 V. If the NRESWARM pin is unused, it can be left floating due to the internal pull-up to VRTC.

2.6.9 NSLEEP

The NSLEEP pin should be connected to the sleep output pin of the SoC. However with the AM572x processor, sleep mode is not supported, therefore the NSLEEP pin should not be used. If the NSLEEP pin is not used, it can be left floating due to the internal pull-up to VRTC.

2.6.10 REGEN1

Refer to the TPS659037 user's guide to see if REGEN1 is part of the power-up sequence. If REGEN1 is part of the power-up sequence and is used on the system, it should be connected as shown in the TPS659037 user's guide. If REGEN1 is not in the power-up sequence and it is used on the system, it can be enabled through I²C and therefore should be connected to the external device. If REGEN1 is not used, it can be left floating.

REGEN1 is in the VSYS domain, therefore the output voltage will be the same voltage as VCC1.

2.6.11 RESET_OUT

RESET_OUT is the last rail to come up in the sequence, and should release the SoC from reset. RESET_OUT should be connected to the reset input of the processor. RESET_OUT is in the VIO domain, therefore the output voltage will be the same as VIO.

2.7 Power Detection Signals

2.7.1 POWERGOOD

POWERGOOD is an open-drain output which indicates that each SMPS is within a certain tolerance of the programmed output voltage. It should be connected to a pull-up resistor to 1.8 V, for example LDOVRTC_OUT. If POWERGOOD is unused, it can be left floating.

2.7.2 VBUS

The VBUS pin can be used to detect the presence of a USB VBUS line. If the VBUS pin function is used, VBUS rising and falling edges can be detected through the VBUS interrupt, and the status of the VBUS pin can be read through the VBUSDET output multiplexed with GPIO_1. The VBUS should then be connected to the VBUS line of a USB port. If the VBUS pin function is unused, it should be connected to GND.

2.8 VCC_SENSE, VCC_SENSE2

The VCC_SENSE and VCC_SENSE2 pins should both be connected together to the VCC1 supply. VCC_SENSE must be higher than the programmed VSYS_HI level before the PMIC will turn on. Refer to the TPS659037 user's guide for the programmed VSYS_HI level. The VCC_SENSE and VCC_SENSE2 pins must always be used, and should never be left floating.

2.9 Test Pins

2.9.1 VPROG

VPROG is only used for factory testing, and should be left floating.

3 Design Checklist

The *TPS659037 Design Checklist* ([SLIA089](#)) in Excel format lists the recommended external components, connections if unused, as well as other helpful information.

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