Application Report
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How to Power Up the TPS659038-Q1 and TPS659039-Q1

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ABSTRACT

The TPS659038-Q1 and TPS659039-Q1 (TPS65903x-Q1) are highly integrated power-management integrated circuits (PMICs) used to power application processors such as OMAP5 and Jacinto 6. This application note discusses the various methods that can be used to enable and disable the TPS65903x-Q1 device and includes timing diagrams for each enable and disable method. In case of a discrepancy between this document and the data sheet, please refer to the data sheet for the most accurate information.

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1 Introduction

The TPS65903x-Q1 PMIC contains an embedded power controller (EPC) that executes one-time-programmable (OTP) power sequences. This feature allows the device to offer all of the needed power sequencing that the supported processor needs with minimal external components. As a result of this integration, the PMIC offers multiple ways to enable and disable the device.

2 Key Terms

Before discussing the different methods of powering up the TPS65903x-Q1 device, a few key terms must be defined and explained. These terms include: ON request (see Section 2.1), OFF request (see Section 2.2), gating condition (see Section 2.3), and power acknowledge (see Section 2.4).

2.1 ON Request

ON requests are used to switch on the device. These requests cause the device to transition from the OFF state to the ACTIVE state. Table 1 lists the complete list of ON requests for the TPS65903x-Q1 device along with additional information about each request.

Table 1. ON Requests

EVENT	MASKABLE	POLARITY	COMMENT	DEBOUNCE
RPWRON (pin)	No	Low	Level Sensitive	16 ms ± 1 ms
PWRON (pin)	No	Low	Level Sensitive	N/A
Part of Interrupts (event)	Yes (INTx_MASK register, default state is masked)	Event	Edge Sensitive	N/A
POWERHOLD (pin)	No	High	Level Sensitive	N/A

2.2 OFF Request

OFF requests are used to switch off the device. They cause the device to transition from the ACTIVE state to the OFF state or from the SLEEP state to the OFF state. OFF requests have the highest priority with no gating conditions for an OFF request. Any OFF request is executed even if a valid SLEEP or ON request is present, with the exception of DEV_ON and POWERHOLD, which both have lower priority. In that case, the device goes to the OFF state, and, when the OFF request is cleared, the device reacts to the ON or SLEEP request if the respective request is still present. Table 2 lists a complete list of OFF requests along with additional information about each OFF request.

Table 2. OFF Requests

EVENT	MASKABLE	POLARITY	DEBOUNCE	SWITCH OFF DELAY	RESET LEVEL	RESET SEQUENCE
PWRON (pin) (long press key)	No	Low	N/A	SWOFF_DLY	HWRST	Shutdown
PWRDOWN (pin)	No	High	N/A	SWOFF_DLY	SWORST	Cold reset
WATCHDOG TIMEOUT (internal event)	N/A. WDT is disabled by default but software can enable it	N/A	N/A	SWOFF_DLY	HWRST	Cold reset
THERMAL SHUTDOWN (internal event)	No	N/A	N/A	0	HWRST	Shutdown
RESET_IN (pin)	No	Low	N/A	SWOFF_DLY	HWRST	Cold reset
SW_RST (register bit)	No	N/A	N/A	0	HWRST	Cold reset
DEV_ON (register bit)	No	N/A	N/A	0	SWORST	Shutdown
VSYS_LO (internal event)	No	N/A	N/A	0	HWRST	Shutdown
POWERHOLD (pin)	No	Low	N/A	0	SWORST	Shutdown
GPADC_SHUTDOWN	Yes	N/A	N/A	SWOFF_DLY	SWORST	Shutdown

Notes:

- SWOFF_DLY is the same for all requests. Once configured through I2C to a specific value (0, 1, 2, or 4 s) it is applied to all OFF requests.
- RESET_LEVEL is selectable as HWRST (wide set of registers is reset to default values) or SWORST (more limited set of registers is reset).
- OFF requests are configured to force the EPC to either execute a shutdown (SD) or a cold restart (CR).
  - When configured to generate an SD, the EPC executes a transition to the OFF state (SLP2OFF or ACT2OFF power sequence) and remains in the OFF state.
  - When configured to generate a CR, the EPC executes a transition to the OFF state (SLP2OFF or ACT2OFF power sequence) and restarts, transitioning to the ACTIVE state (OFF2ACT power sequence) if none of the ON request gating conditions are present.
- Watchdog is disabled by default. Software (SW) can enable watchdog and lock (write protect) watchdog register (WATCHDOG).
- The DEV_ON event has a lower priority over other ON events; it forces the device to go to the OFF state only if no other ON conditions are keeping the device active (POWERHOLD).
- The POWERHOLD event has a lower priority over other ON events; it forces the device to go to the OFF state only if no other ON conditions are keeping the device active (DEV_ON).

2.3 Gating Condition

A gating condition is a device condition that prevents an ON request from successfully enabling the PMIC. Table 3 lists a complete list of all gating conditions along with additional information about each condition.

Table 3. ON Request Gating Conditions

EVENT	MASKABLE	POLARITY	COMMENT
VSYS_HI (event)	No	Low	VCC_SENSE < VSYS_HI
HOTDIE (event)	No	High	Device temperature exceeds HOTDIE level
PWRDOWN (pin)	No	High	
RESET_IN (pin)	No	Low	

2.4 Power Acknowledge

When the PMIC is turned on, the PMIC remains on for 8 s and then shuts off automatically if the PMIC does not receive a power acknowledge in this time. The power acknowledge can be communicated in two ways. The first way is by driving the POWERHOLD pin high to 1.8 V. When the POWERHOLD pin is used as an ON request, it also provides the power on acknowledge at the same time.

The second way to communicate power acknowledge is by setting the register bit, DEV_CTRL.DEV_ON, to 1. When using this method, the OTP bit, AUTODEVON, must be considered. Because the AUTODEVON bit is set to 0 by default, the DEV_CTRL.DEV_ON bit must be set to 1 through I^2C within 8 s of a power on.

Power acknowledge must be considered when PWRON, RPWRON, and interrupts are used as a power-on request. When these ON requests are used to enable the PMIC, either DEV_CTRL.DEV_ON bit should be set by the AUTODEVON bit or I^2C, or else the POWERHOLD bit must be driven at 1.8 V to keep the PMIC active.

3 Enabling the PMIC

3.1 First Supply Detection (FSD, VSYS_HI)

As listed in the previous tables, the PMIC can be enabled in several ways. Perhaps the simplest method is first supply detection. This method consists of removing all gating conditions, tying the POWERHOLD signal to a permanent logic HIGH, and applying a voltage above VSYS_HI (OTP configurable, programmed to 3.1 V) to the VCC1 pin. This method enables the PMIC as soon as the VSYS_HI threshold is crossed without having to control any external signals. Figure 1 below shows the turn-on sequence of the PMIC being triggered by the 5-V DC supply on VCC1.

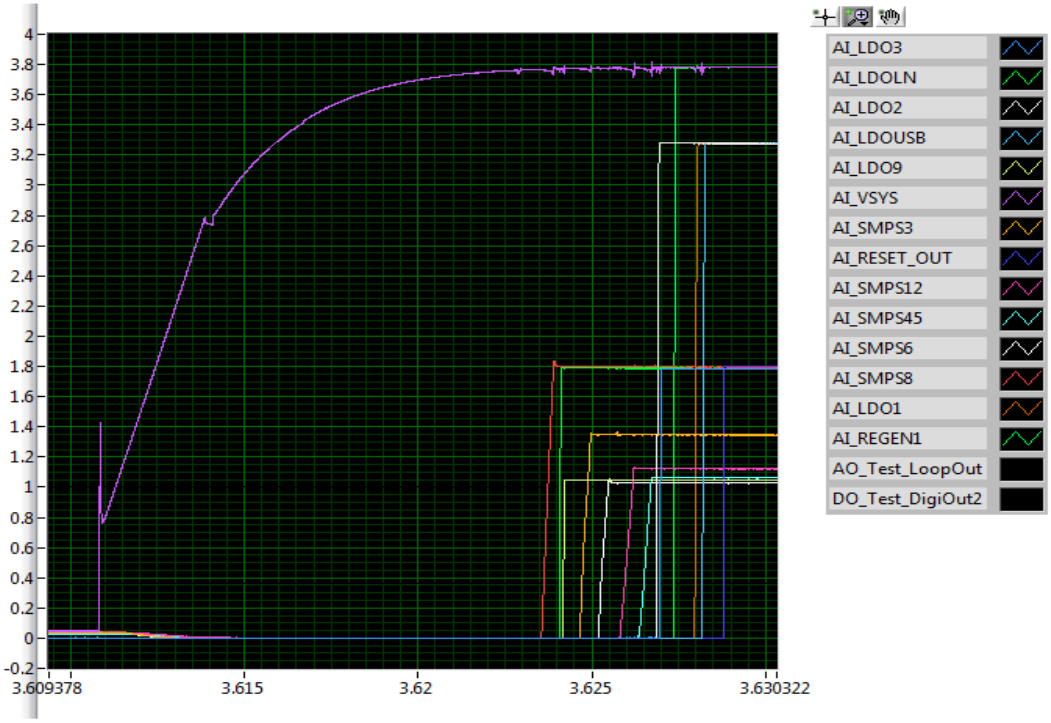

Figure 1. ON Request using First Supply Detection (VSYS_HI)

3.2 PWRON

Another method of enabling the PMIC is using the PWRON signal. Typically, the PWRON signal is used in a pushbutton application where one pin of the pushbutton is connected to GND and the other pin is connected to the PWRON pin. When the pushbutton is pressed, the active-low PWRON pin is shorted to GND initiating the ON request. Because of the active-low nature, the PWRON pin has an internal pullup resistor to the VSYS voltage domain. Figure 2 shows a circuit diagram of this configuration. Figure 3 shows the PMIC power sequence using the PWRON signal.

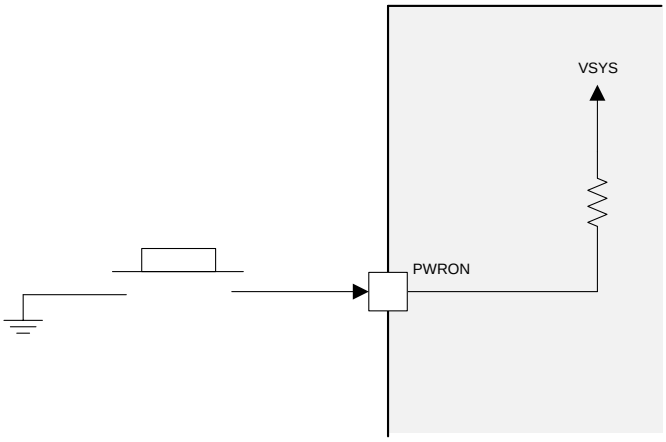

Figure 2. Typical PWRON Configuration

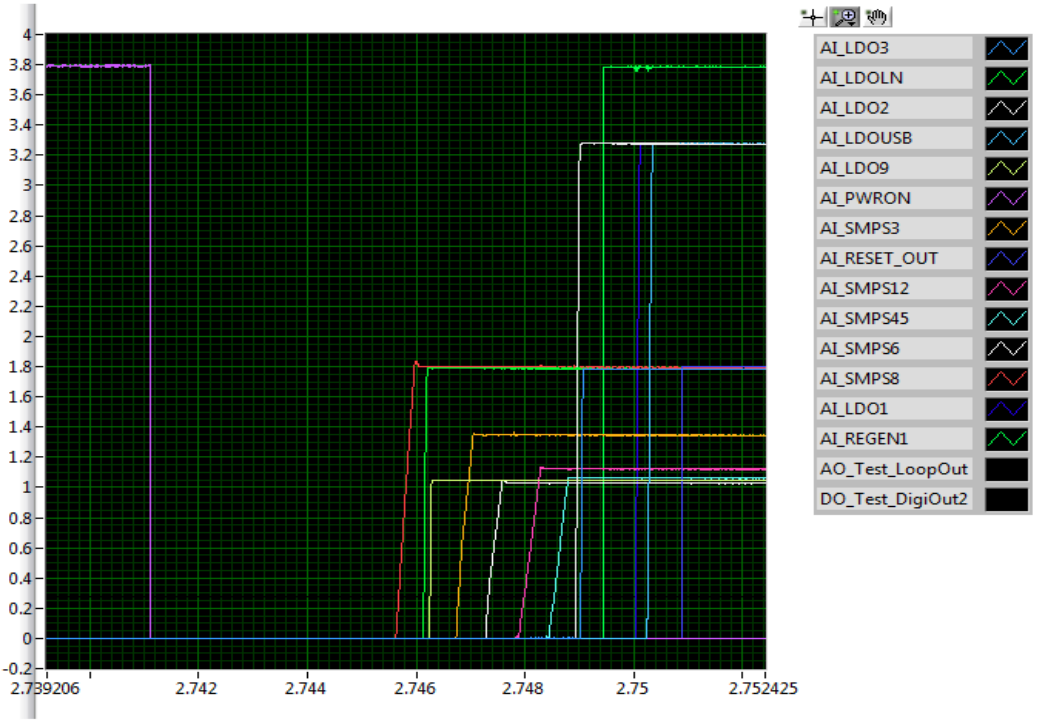

Figure 3. ON Request Using PWRON

The PMIC has a long key-press function that disables the PMIC if the PWRON pin is connected to GND for a certain configurable length of time. This duration is configured through the LONG_PRESS_KEY register and can be set through I^2C to a duration of 6 s, 8 s, 10 s, or 12 s (default). Because of this function, the PWRON signal must be released before the timer expires otherwise the PMIC turns off which is why the pushbutton is often used with the PWRON signal. A simple push and release initiates the ON request. This function is discussed further when discussing OFF requests in Section 4.

3.3 RPWRON

Similarly to the PWRON signal, remote PWRON (RPWRON) can be used to enable the PMIC. The difference between these two methods is that RPWRON does not normally use a pushbutton and it relies on software or logic instead. RPWRON is an active-low signal, so it must be driven low to initiate the ON request. Figure 4 shows the PMIC power sequence using RPWRON as the ON request. RPWRON does not offer the LONG_PRES_KEY-functionality.

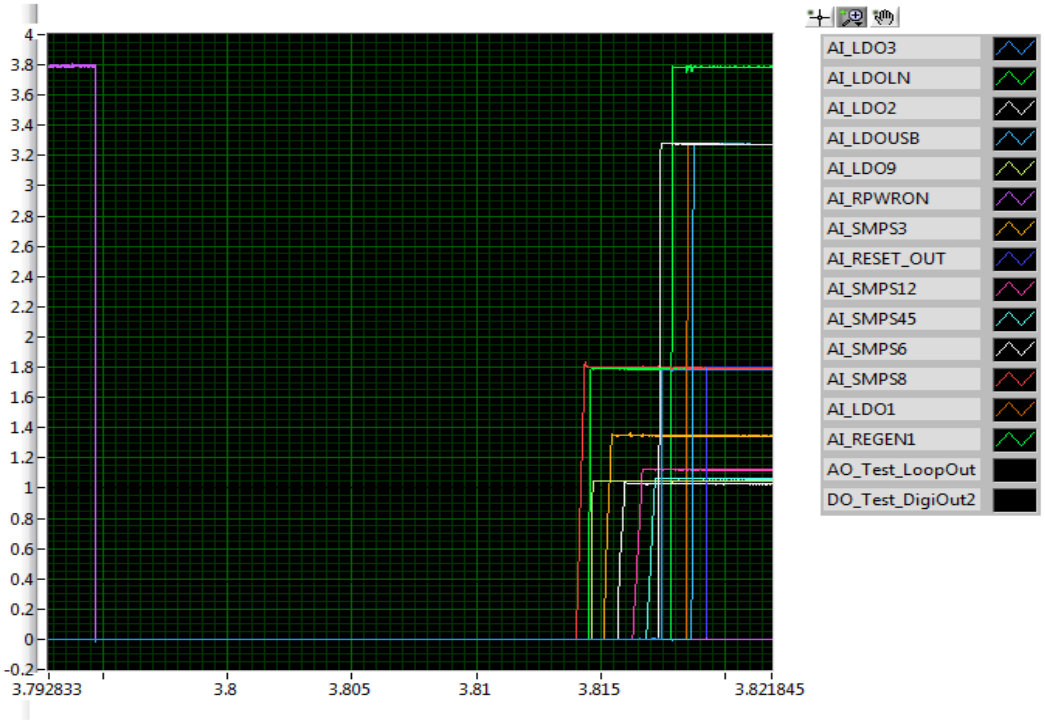

Figure 4. ON Request Using RPWRON

3.4 Interrupts

Interrupts can also be used to enable the PMIC. By default, these interrupts are masked as ON requests, but these interrupts can be unmasked through register manipulation. The *Interrupt Sources* table in the TPS65903x-Q1 data sheet lists a full list of PMIC interrupts. Figure 5 shows the PMIC power sequence using the GPIO_5 interrupt as the ON request.

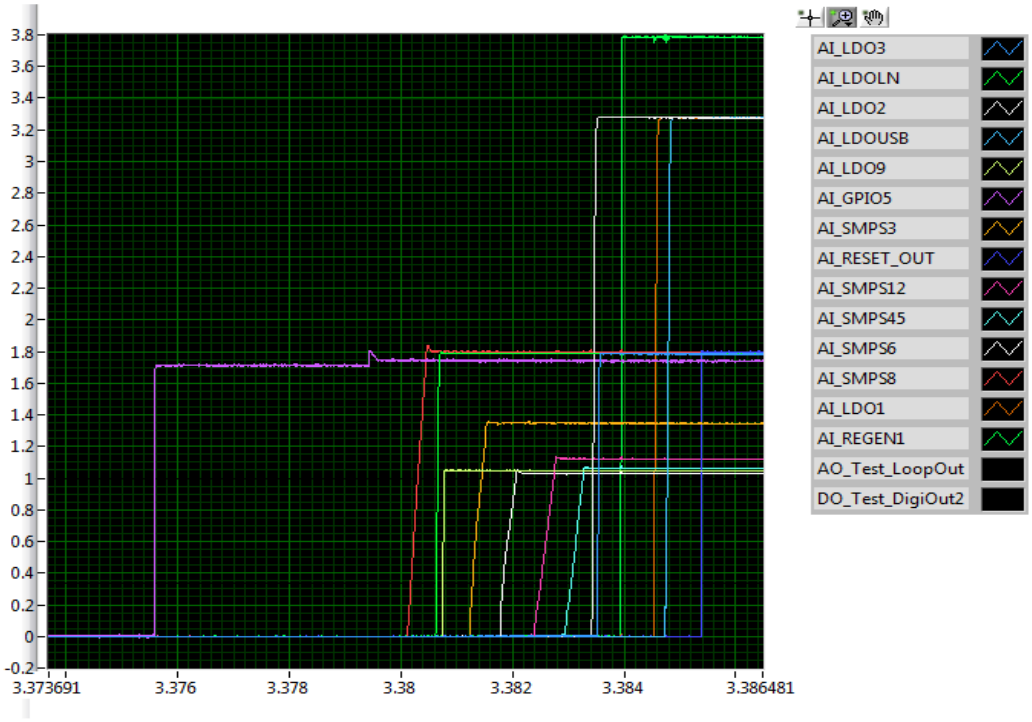

Figure 5. ON Request Using GPIO_5 Interrupt

3.5 POWERHOLD

The last event that can be used as an ON request is the POWERHOLD signal. A logic high on the POWERHOLD pin enables the PMIC, while a logic low disables it. This pin can be used in combination with another ON request as shown in Figure 6 to keep the PMIC on when the reset signal of the processor is released (RESET_OUT). When the POWERHOLD pin goes LOW, it is interpreted as an OFF request by the PMIC.

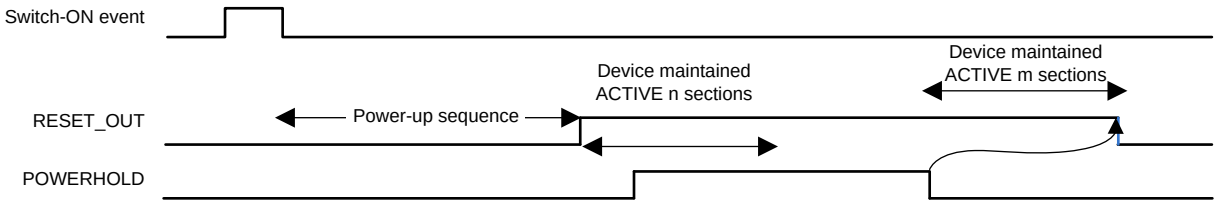

Figure 6. Typical POWERHOLD Use Case

Figure 7 shows the PMIC power-up sequence when the POWERHOLD signal is used as the ON request.

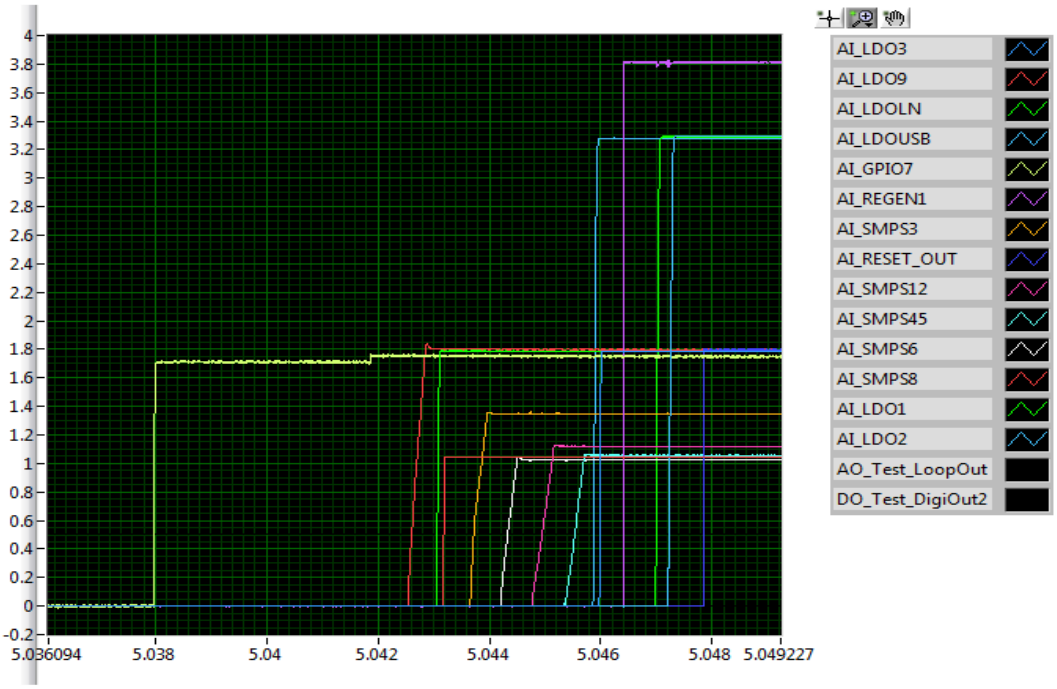

Figure 7. ON Request Using POWERHOLD

4 Disabling the PMIC

4.1 Long Key Press

As mentioned in the PWRON section (Section 3.2), the PMIC has a long key-press function that disables the PMIC if the PWRON pin is connected to GND for a certain configurable length of time. This duration is configured through the LONG_KEY_PRESS register and can be set through I^2C to a duration of 6 s, 8 s, 10 s, or 12 s (default). When a long key press event is detected, the PMIC initiates a transition from the ACTIVE to the OFF state and all HWRST registers are reset to the default value. Figure 8 shows the PMIC power-down sequence when the long key press is used as the OFF request

NOTE: The PWRON signal (yellow trace) is low when all rails sequence off.

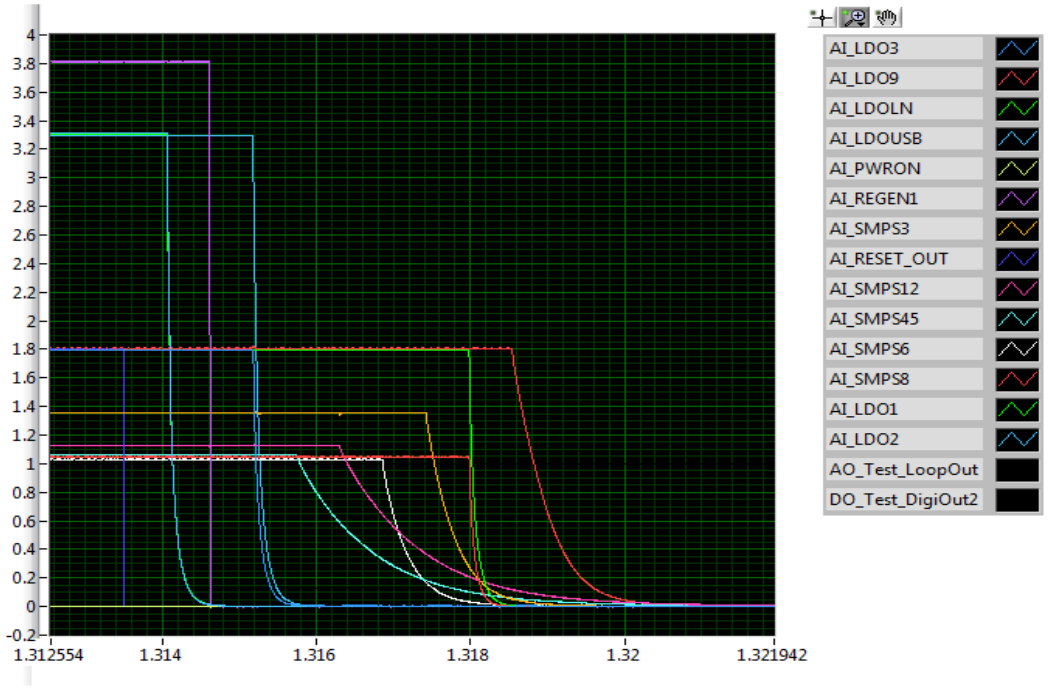

Figure 8. OFF Request Using Long Key Press (PWRON)

4.2 PWRDOWN

The PWRDOWN pin can be used to disable the PMIC or as a gating condition for power-on. This pin is active high, which means that when PWRDOWN pin is high then the device shuts off. Figure 9 shows the PMIC power down sequence when the PWRDOWN signal is used as the OFF request and executes a shutdown event rather than a cold restart. Figure 10 shows the PWRDOWN pin used as a gating condition for power-on.

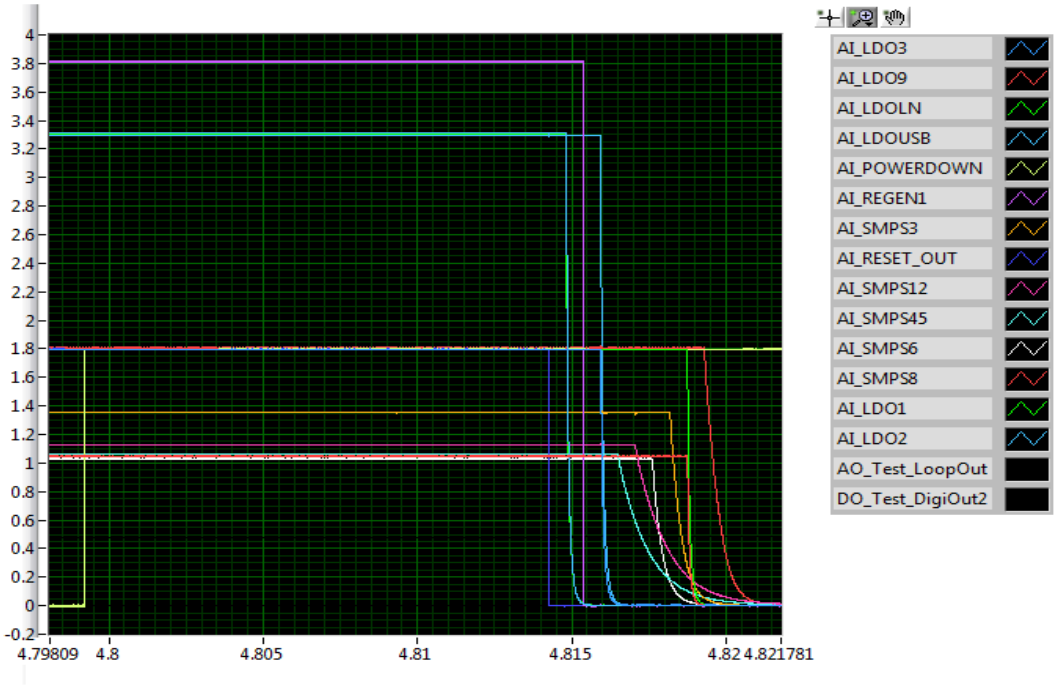

Figure 9. OFF Request Using POWERDOWN

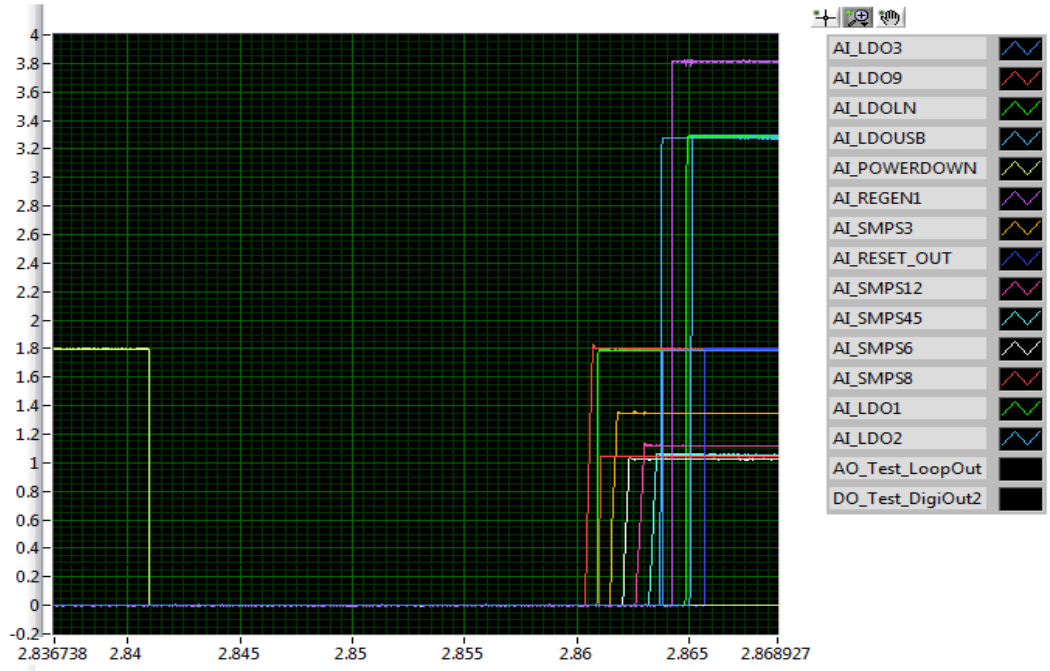

Figure 10. POWERDOWN as a Gating Condition

4.3 RESET_IN

The RESET_IN pin can be used to disable the PMIC or as a gating condition for power-on. This pin is active low, which means that when RESET_IN is low, then the device shuts off. Figure 11 shows the PMIC power-down sequence when the RESET_IN signal is used as the OFF request, and executes a shutdown event rather than a cold restart.

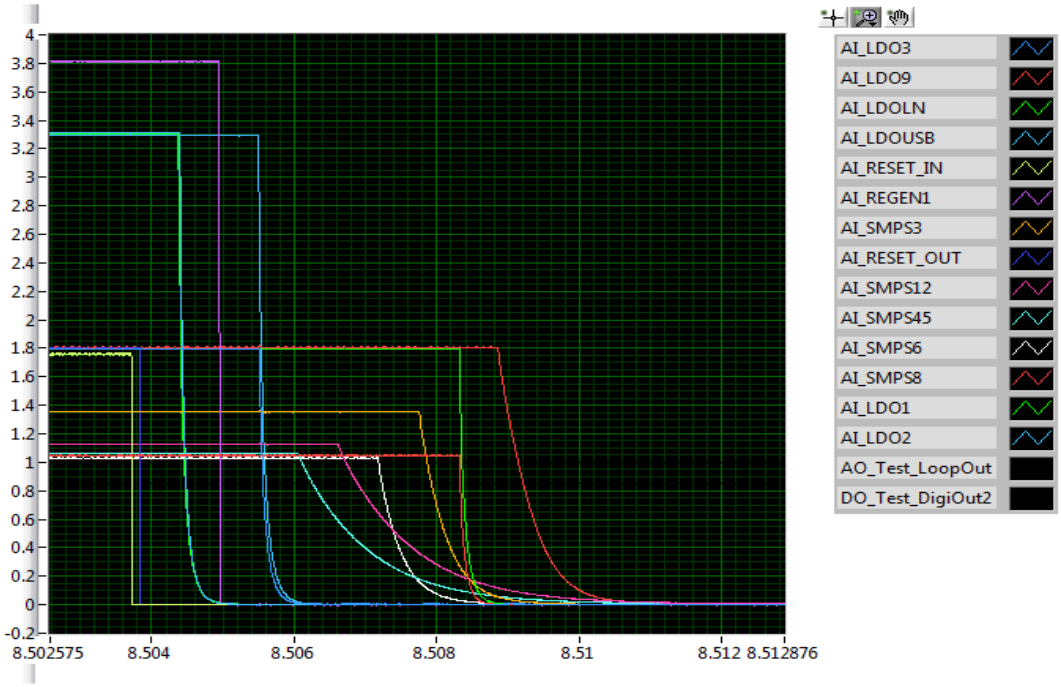

Figure 11. OFF Request Using RESET_IN

4.4 DEV_ON

The DEV_ON bit can be used to disable the PMIC. As mentioned in the section on OFF requests, the DEV_ON bit has a lower priority over other events. This bit forces the device to go to the OFF state only if no other ON conditions are keeping the device active (POWERHOLD). When used as the OFF request, the DEV_ON bit executes the shutdown sequence and all SWORST registers are reset to the default value. This method of disabling the PMIC is controlled by software only.

4.5 VSYS_LO

Another method that can be used to disable the PMIC is by removing the input supply voltage. When the voltage on the VCC1 pin drops below the VSYS_LO value (configured to 2.75 V), all power rails are disabled immediately. This disabling is a failsafe mechanism and should not be consistently used as the power-down method because the sequencing requirements fo the processor may not be met. Figure 12 shows the power-off sequence of the PMIC being triggered by removal of the input supply voltage.

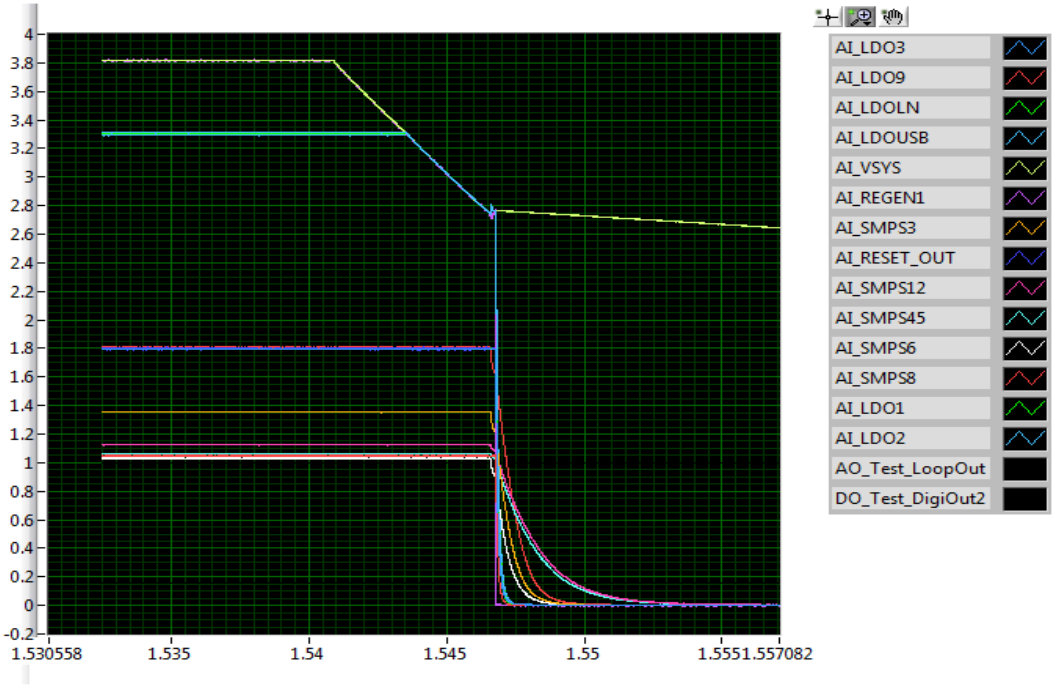

Figure 12. OFF Request by Removal of Supply Voltage (VSYS_LO)

4.6 POWERHOLD

The POWERHOLD pin can also be used as an OFF request. This is a level-sensitive signal and, therefore, as soon as the signal is driven LOW, the shutdown sequence is initiated. Using the POWERHOLD pin as the OFF request resets all of the SWORST registers to the default value and executes a shutdown event. Figure 13 shows the power-off sequence of the PMIC as triggered by a POWERHOLD event.

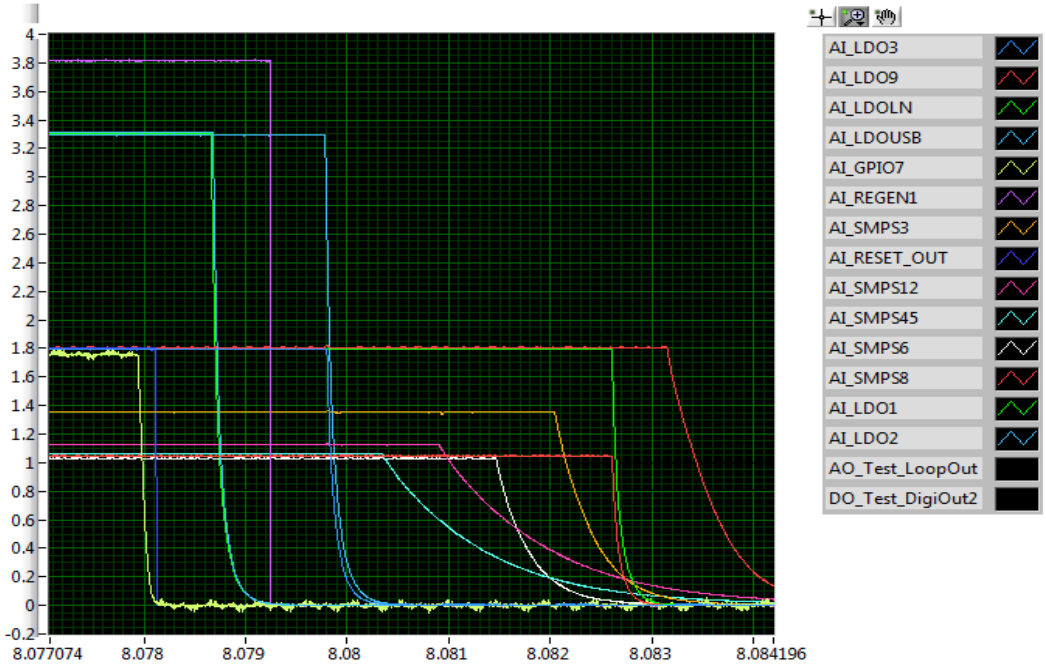

Figure 13. OFF Request Using POWERHOLD

5 Conclusion

While various options are available to power up and power down the PMIC, two approaches are used frequently depending on the application.

For stand-alone products like tablets that have a dedicated power-button, the PWRON approach is usually used. For automotive applications the RESET_IN with POWERHOLD tied high approach is usually used.

In stand-alone applications, the startup time is not critical and pressing the power-button for a long time to reset the device is common. The same functionality is achieved with the PWRON approach.

In automotive application where having fast startup times (such as for a rear-view camera) is paramount and with no power-button being available (mostly always on when ignition is on), no long-press-key is possible. Because no software is required for both power up (no need to service the POWERHOLD pin) and shutdown (no need to set the DEV_ON bit), this approach is fast and robust.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2014) to A Revision	Page
• First public release of document	3

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