TPS65910 User Guide For OMAP3 Family of Processor

This document can be used as a reference for connectivity between the TPS65910 power-management integrated circuit (PMIC) and the OMAP3 family (OMAP35xx/OMAP36xx/DM37xx/AM37xx/AM35xx, except AM3517 and AM3505).

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1 Introduction

This document can be used as a reference for connectivity between the TPS65910 PMIC and OMAP3 family (OMAP35xx/OMAP36xx/DM37xx/AM37xx/AM35xx, except AM3517 and AM3505). For information about the power resources or the functionality of the device, see the device data sheet.

2 Platform Connection

Figure 1 shows the power supply connections between the TPS65910 and OMAP3.

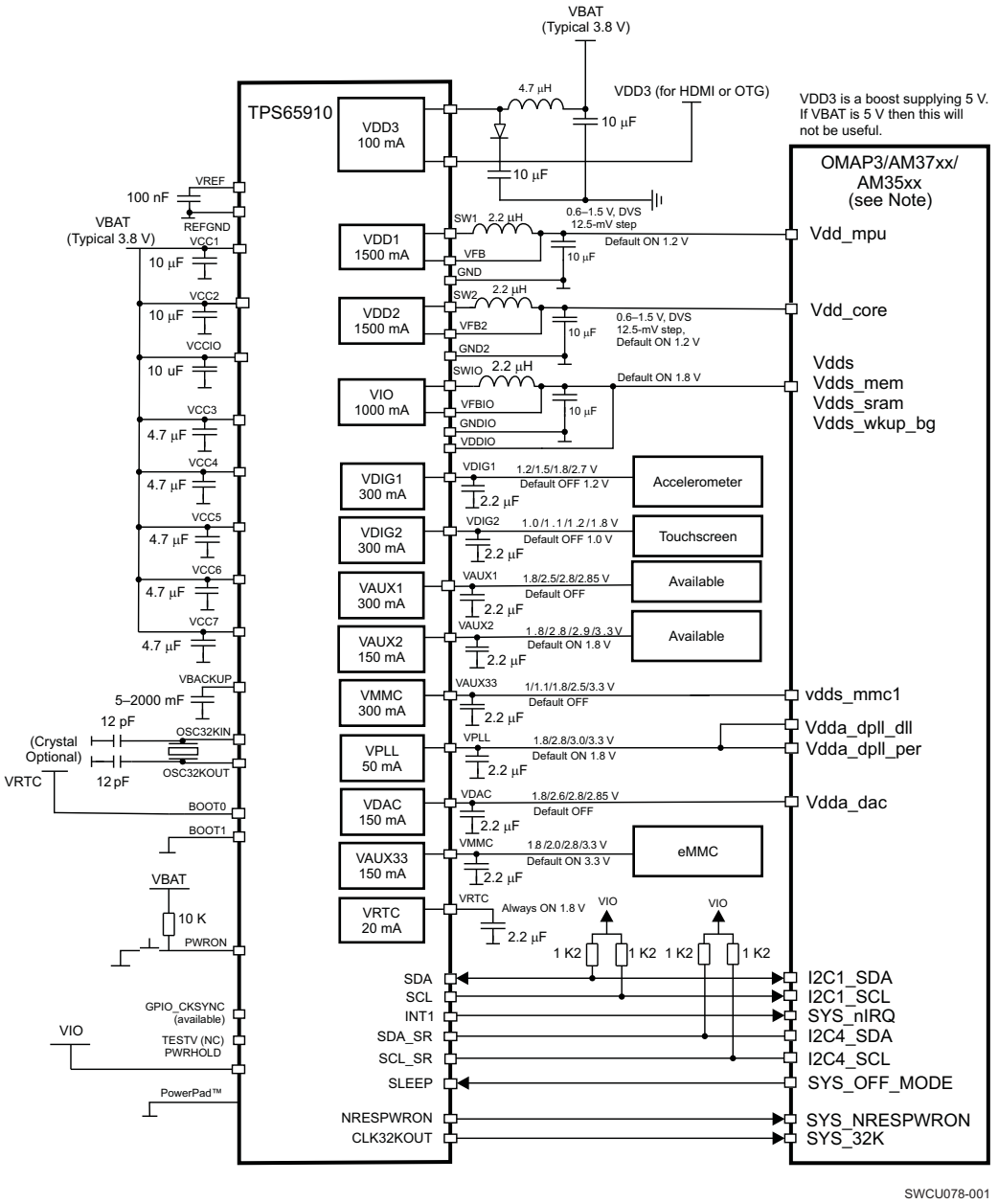

Figure 1. OMAP3 Power Supply Connections With TPS65910

NOTE:

- This diagram does not apply to the AM3517 and AM3505 processors.
- The power-up sequence for OMAP core power rails (for VDD_CORE and VDD_MPU) is swapped. However, this does not affect OMAP power up. OMAP powers up without any issues.
- The reason for swapping the supply domains is that, based on experimentation, VDD1 is less board sensitive than VDD2 under heavy load (> 1200 mA) conditions, so it is recommended to use VDD1 for handling the heaviest load condition of the application, thus easing the board routing.

At power up, the maximum current capability (default setting) of the DCDC converters is as follows:

- VIO(max) = 500 mA
- VDD1(max) = 1000 mA
- VDD2(max) = 1000 mA

To have the maximum current capability, the user must program the following register bits:

- VIO_REG[ILMAX] = b01 for 1 A
- VDD1_REG[ILMAX] = b1 for 1.5 A
- VDD2_REG[ILMAX] = b1 for 1.5 A

3 Power-Up Sequencing

3.1 Power-Up Sequence for OMAP3 Family

This section describes the power-up sequence for the TPS65910 power rails that matches the power-up sequence for the processors named in Section 1, *Introduction*. To power up the system, the user should press and release the PWRON switch (generating a negative pulse) on the platform (see Figure 2.)

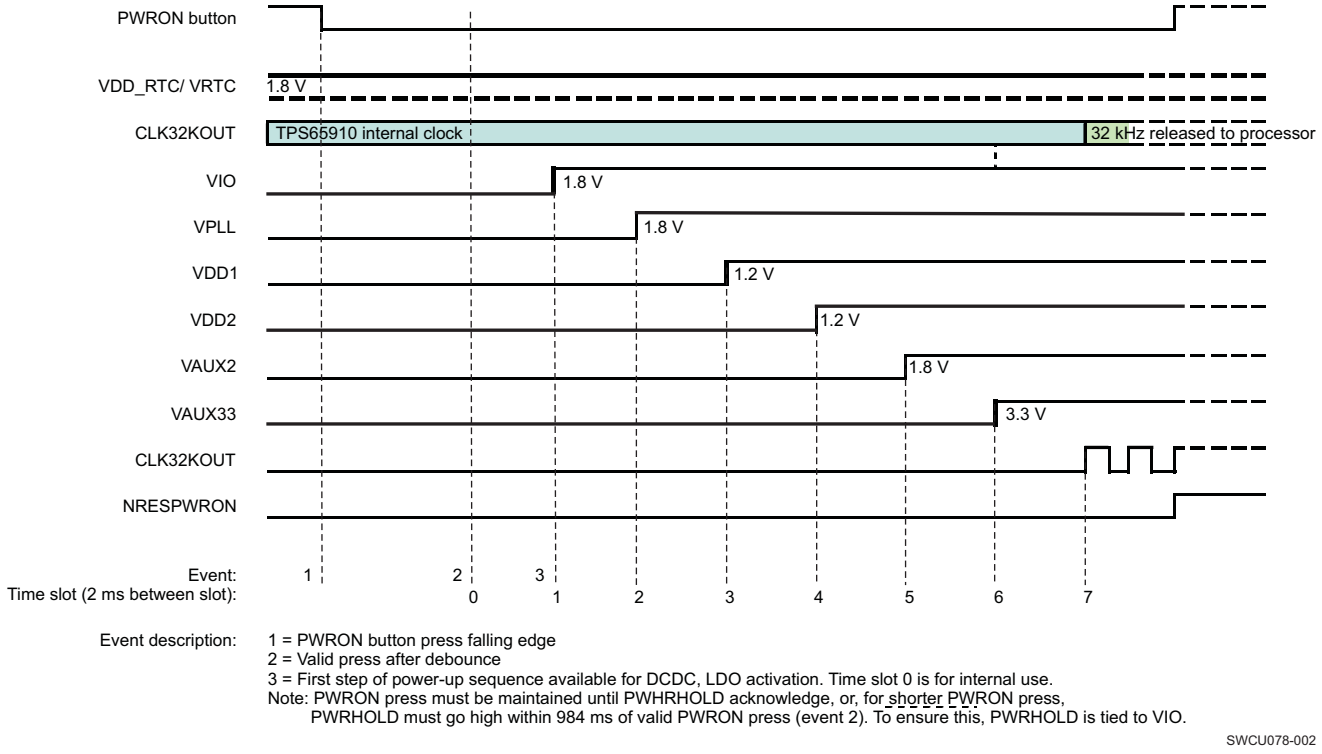

Figure 2. Power-Up Sequence for TPS65910

Table 1 describes the power-up sequence for TPS65910 where BOOT0 = 1 and BOOT1 = 0. This sequence is aligned for the family of processors named in Section 1, *Introduction*.

Table 1. Power-Up Sequence for TPS65910 (BOOT0 = 1 and BOOT1 = 0)

Power Domain	Pin Name	Voltage (V)	Sequence
IO CORE	VDDS_WKUP_BGVDDS_SRAMVDDS_MEMVDDS	1.8	1
PLL	VDDS_DPLL_DLLVDDS_DPLL_PER	1.8	2
Core	VDD_CORE	1.2	3
Core	VDD_MPU	1.2	4

NOTE: For correct power on of the device, the PWRHOLD signal should be high after PWRON is pressed. For an OMAP3 configuration, the PWRHOLD signal on TPS65910 is connected to VIO. PWRHOLD transitions to high when VIO powers up.

Table 2 describes the power domain mapping for the TPS65910 and OMAP35xx/AM35xx processors.

Table 2. Power Domain Mapping

TPS65910 Power Resource	Imax (mA)	OMAP35xx/AM35xx Power Domain	Imax (mA)
VIO	1000	Vdds_io	60
		vdds_mem	35
		vdds_sram	41
		Vdda_wkup_bg_bb	5
VPLL	50	Vdda_dplls_dll	30
		Vdda_dpll_per	10
VDD1	1500	Vdd_mpu	1200
VDD2	1500	Vdd_core	300
VDAC	150	Vdda_dac	60
VAUX2	150	Vdds_mmc1	20

Table 3 lists the EEPROM configuration of the TPS65910.

Table 3. EEPROM Configuration of TPS65910

Register	Bit	Description	TPS65910 BOOT0/1
VDD1_OP_REG	SEL	VDD1 voltage level selection for boot	1.2 V
VDD1_REG	VGAIN_SEL	VDD1 gain selection (x1 or x2)	x1
EEPROM		VDD1 time slot selection	3
DCDCCTRL_REG	VDD1_PSKIP	VDD1 pulse skip mode enable	Skip enabled
VDD2_OP_REG/VDD2_SR_REG	SEL	VDD2 voltage level selection for boot	1.2 V
VDD2_REG	VGAIN_SEL	VDD2 gain selection (x1 or x3)	x1
EEPROM		VDD2 time slot selection	4
DCDCCTRL_REG	VDD2_PSKIP	VDD2 pulse skip mode enable	Skip enabled
VIO_REG	SEL	VIO voltage selection	1.8 V
EEPROM		VIO time slot selection	1
DCDCCTRL_REG	VIO_PSKIP	VIO pulse skip mode enable	Skip enabled
EEPROM		VDD3 time slot	OFF
VDIG1_REG	SEL	LDO voltage selection	1.2 V
EEPROM		LDO time slot	OFF
VDIG2_REG	SEL	LDO voltage selection	1.0 V
EEPROM		LDO time slot	OFF
VDAC_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	OFF
VPLL_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	2
VAUX1_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	OFF
VMMC_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	OFF
VAUX33_REG	SEL	LDO voltage selection	3.3 V

Table 3. EEPROM Configuration of TPS65910 (continued)

Register	Bit	Description	TPS65910 BOOT0/1
EEPROM		LDO time slot	6
VAUX2_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	5
CLK32KOUT pin		CLK32KOUT time slot	7
NRESPWRON pin		NRESPWRON time slot	7 + 1
VRTC_REG	VRTC_OFFMASK	0 = VRTC LDO is in low-power mode during OFF state. 1 = VRC LDO is in full-power mode during OFF state.	Low-power mode
DEVCTRL_REG	RTC_PWDN	0 = RTC in normal power mode 1 = Clock gating of RTC register and logic, low-power mode	1
DEVCTRL_REG	CK32K_CTRL	0 = Clock source is crystal/external clock. 1 = Clock source is internal RC oscillator.	Crystal
DEVCTRL2_REG	TSLOT_LENGTH	Boot sequence time slot duration: 0 = 0.5 ms 1 = 2 ms	2 ms
DEVCTRL2_REG	IT_POL	0 = INT1 signal will be active low 1 = INT1 signal is active high.	Active low
INT_MSK_REG	VMBHI_IT_MSK	0 = Device automatically switches on at NOSUPPLY-to-OFF or BACKUP-to-OFF transition. 1 = Start-up reason is required before switch on.	0 = Automatic switch-on from supply insertion
VMBCH_REG	VMBCH_SEL[1:0]	Select threshold for main battery comparator threshold VMBCH.	3 V

4 Getting Started With TPS65910 and Associated Processor

4.1 First Initialization

4.1.1 I/O Polarity/Muxing Configuration

Program DEVCTRL2_REG.SLEEPSIG_POL = 0 to set the polarity of the SLEEP signal for active low. The software configuration allows specific power resources to enter low consumption state when the SLEEP signal goes low.

Set DEVCTRL_REG.DEV_SLP = 1 to allow sleep transition when requested.

Update the GPIO0 configuration (GPIO0_REG) as desired.

4.1.2 Define Wakeup/Interrupt Event (SLEEP or OFF)

Select the appropriate bits in the INT_MSK_REG and INT_MSK2_REG registers to activate an interrupt to the processor on the INT1 line.

4.1.3 Backup Battery Configuration

If a backup battery is used, set BBCH_REG[BBCHEN] to 1 to enable backup battery charging. Maximum voltage can be set based on backup battery specifications (BBSEL).

4.1.4 DCDC and Voltage Scaling Resource Configuration

NOTE: If the SmartReflex™ interface is not used for voltage scaling (power saving), then these pins can be used to control the power resources.

Configure two operating voltages for DCDC1 and DCDC2:

- VDDx_OP_REG.SEL = roof voltage (Enx ball High)
- VDDx_SR_REG.SEL = floor voltage (Enx ball Low)

Assign control of DCDC1 to SCLSR_EN1 and DCDC2 to SCLSR_EN2:

- Set EN1_SMPS_ASS_REG.VDD1_EN1 = 1.
- Set EN2_SMPS_ASS_REG.VDD2_EN2 = 1.
- Set SLEEP_KEEP_RES_ON_REG.VDD2_KEEPON = 1 (allow low-power mode).
- Set SLEEP_KEEP_RES_ON_REG.VDD1_KEEPON = 1 (allow low-power mode).

4.1.5 Sleep Platform Configuration

Configure the state of the LDOs when the SLEEP signal is used. By default, all resources go to SLEEP state. In SLEEP state the LDO voltage is maintained but transient and load capability is reduced.

Resources that provide full load capability must be set in the SLEEP_KEEP_LDO_ON_REG register.

Resources that can be set off in SLEEP state to optimize power consumption must be set in the SLEEP_SET_LDO_OFF_REG register.

4.2 Event Management Through Interrupt

4.2.1 INT_STS_REG.VMBHI_IT

INT_STS_REG.VMBHI_IT indicates that the supply (VBAT) is connected. Leaving BACKUP or NO SUPPLY state, the system must be initialized (see Section 4.1, *First Initialization*).

4.2.2 INT_STS_REG.PWRON_IT

INT_STS_REG.PWRON_IT is triggered by pressing the PWRON button. If the device is in OFF or SLEEP state, then this interrupt acts as a wake-up event and resources are reinitialized.

4.2.3 INT_STS_REG.PWRON_LP_IT

INT_STS_REG.PWRON_LP_IT is the PWRON long-press interrupt and is generated when the PWRON switch is pressed for 6 seconds. The application processor can decide to acknowledge the interrupt. If this interrupt is not acknowledged in the following 2 seconds, the device interprets this as a power-down event.

4.2.4 INT_STS_REG.HOTDIE_IT

INT_STS_REG.HOTDIE_IT indicates that the temperature of the die is reaching the limit. Software must decrease power consumption before automatic shutdown.

4.2.5 INT_STS_REG.VMBDCH_IT

INT_STS_REG.VMBDCH_IT indicates that the input supply is low and the processor must prepare a shutdown to avoid losing data.

This interrupt is linked to VBAT but does not apply in a system where PMIC is connected to 5-V rails and not connected directly to VBAT.

4.2.6 INT_STS2_REG.GPIO_R/F_IT

INT_STS2_REG.GPIO_R/F_IT is the GPIO interrupt event and can be used to wake up the device from SLEEP state. This can be an interrupt coming from any peripheral or similar device. This wake-up event is not valid for a transition from OFF state.

4.2.7 INT_STS_REG.RTC_ALARM_IT

INT_STS_REG.RTC_ALARM_IT is triggered when the RTC alarm set time is reached.

5 Revision History

Table 4. Revision History

Version	Literature Number	Date	Notes
*	SWCU078	December 2010	See (1).
A	SWCU078A	July 2011	See (2).

(1) *TPS65910 User Guide For OMAP3 Family of Processor*, SWCU071 - Initial release.

(2) *TPS65910 User Guide For OMAP3 Family of Processor, and TMS320C674x*, SWCU071A:

- Update Figure 1: Fix inductors on DCDC1 and DCDC2, change from 2.2 nH to 2.2 uH.

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