Application Report
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TPS65950 Schematic Checklist

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ABSTRACT

This application note for TPS65950 , a power companion device for OMAP processors, lists the connection details for each pin. The ball details include a brief explanation of the function of each pin or signal and whether the signal is analog or digital. Use this information to check the connectivity for each ball on a system schematic.

Table 1. TPS65950 Schematic Checklist

Ball Name	TPS65950 Pinlist	Default Configuration	SW Pin Muxing (Reg Name/Bit Name/Value)	Description	Type	A/D	Output Default Value	Recommended Connectivity	Connectivity When Function is not Used
H4	ADC	ADCIN0		Battery type	IO	A		Internal current source. Limited input voltage 1.5 V. No prescaler. Grounded if not used.	GND
J3		ADCIN1		Battery temperature	IO	A		BCI battery presence check. Internal current source. Limited input voltage 1.5 V. No prescaler. Cannot be used as general-purpose. Grounded if not used.	GND
G3		ADCIN2		General-purpose ADC input	I	A		Prescaler integrated. Limited input voltage 2.5 V. Grounded if not used.	GND
P5	Charger	VCCS		Charge current sensing	I	A		Precharge battery voltage sensing. 0.22 Rs sense resistor close to device. Routing matched with VBATS. Resistance max 3Ω. Connected to VRPRECH if not used.	Connected to VRPRECH if not used
N5		VAC		Charge device input voltage	POWER	A		Charger presence detection and connection. Add RC and transistor for in-rush current limitation. Grounded if BCI not used. 7-V maximum.	Connected to ground
P4		VBATS		Charge current sensing	I	A		Precharge battery voltage sensing. 0.22 Rs sense resistor close to device. Routing matched with VCCS. Resistance max 3Ω. Connected to VRPRECH if not used.	Connected to VRPRECH if not used
N4		PCHGAC		Ac precharge sense signal. Also used for EEPROM.	I	A		Ac path, power FET power dissipation limitation, check TRM for calculation. Common value are in the 700K range.	GND
N6		PCHGUSB		USB precharge sense signal	I	A		USB path, power FET power dissipation limitation, check TRM for calculation. Common values are in the 500K range.	GND
N2		VPRECH		Precharge regulator output	O	A		Capacitor of 1uF to ground. Cap to ground if BCI not used.	1uF cap to GND
N1		BCIAUTO		Linear charge specific boot mode	I	A		Resistor connected between BCIAUTO pin and GND: 22K for CVENACA = 0 or 140K for CVENACA = 1. Grounded if BCI not used.	GND
P6		ICTLUSB1		USB power device control	O	A		Don't forget stability external component. Floating if BCI not used.	Floating
P1		ICTLUSB2		USB power device control	O	A		Don't forget stability external component. Floating if BCI not used.	Floating
N7		ICTLAC1		Ac power device control	O	A		Don't forget stability external component. Floating if BCI not used.	Floating
P2		ICTLAC2		Ac power device control	O	A		Don't forget stability external component. Floating if BCI not used.	Floating

Table 1. TPS65950 Schematic Checklist (continued)

Ball Name	TPS65950 Pinlist	Default Configuration	SW Pin Muxing (Reg Name/Bit Name/Value)	Description	Type	A/D	Output Default Value	Recommended Connectivity	Connectivity When Function is not Used
R5		VBAT		Battery voltage sensing	POWER	A		Add 10 µF Filtering capacitor. VBAT level sense.	VBAT
P12	GPIOs/JTAG	GPIO0/CD 1		GPIO0/card detection 1	IO	D		Can be left floating as internal PD	Floating
		JTAG.TDO		JTAG test data output	IO	D		Connected to TDI next chip if used	
N12		GPIO1/CD 2		GPIO1/card detection 2	IO	D		Can be left floating as internal PD	Floating
		JTAG.TMS		JTAG test mode state	I	D		Connected to general TMS if used.	
L4		GPIO2		GPIO2	IO	D		Can be left floating as internal PD	Floating
		TEST1		TEST1 pin used in test mode only	IO	D		Can be left floating as internal PD. TP.	
P13		GPIO15		GPIO15	IO	D		Can be left floating as internal PD	Floating
		TEST2		TEST2 pin used in test mode only	IO	D		Can be left floating as internal PD. TP.	
M4		GPIO6	PMBR1/GPIO6_CLKOK_PWM0_MUTE/b00	GPIO6	IO	D		Can be left floating as internal PD	Floating
		--	PMBR1/GPIO6_CLKOK_PWM0_MUTE/b11	Clock OK	O	D			
		PWM0	PMBR1/GPIO6_CLKOK_PWM0_MUTE/b01	Pulse width driver 0	O	D		Can be left floating as internal PD	
		TEST3		TEST3 pin used in test mode only (controlled by JTAG)	IO	D		Can be left floating as internal PD. TP	
N14		GPIO7	PMBR1/GPIO7_VIBRASYNC_PWM1/b00	GPIO7	IO	D		Can be left floating as internal PD	Floating
		VIBRA.SYNC	PMBR1/GPIO7_VIBRASYNC_PWM2/b01	Vibrator ON-OFF synchronization	I	D		Can be left floating as internal PD or PU.	

Table 1. TPS65950 Schematic Checklist (continued)

Ball Name	TPS65950 Pinlist	Default Configuration	SW Pin Muxing (Reg Name/Bit Name/Value)	Description	Type	A/D	Output Default Value	Recommended Connectivity	Connectivity When Function is not Used
		PWM1	PMBR1/GPIO7_VIBRASYNC_PWM3/b11	Pulse width driver 1	O	D	0	Can be left floating as output.	
		TEST4		TEST4 pin used in test mode only (controlled by JTAG)	IO	D		Can be left floating as internal PD or PU. TP.	
J9	START.ADC	START.ADC		ADC conversion request	I	D		Grounded if not used	GND
C13	CONTROL	SYSEN		System enable output	Open drain/I	D	0	Control slave power IC in master mode or force T2 in Wai-on if low in slave mode. TP required.	Floating
C6		CLKEN		Clock e3nable	O	D	0	Clock enable, TP	Floating
D7		CLKEN2		Clock enable 2	O	D	0	Clock enable 2, TP	Floating
G10		CLKREQ		Clock request	I	D		NSLEEP3. Associated with processor3.TP. Grounded if not used.	GND
F10		INT1		output interrupt line 1	O	D	0	output interrupt for processor 1. TP.	Floating
F9		INT2		output interrupt line 2	O	D	0	output interrupt for processor 2. TP.	Floating
A13		NRESPWRON		output control the NRESPWRON of the application processor	O	D	0	Control of host processor reset. TP.	Floating
B13		NRESWARM		input, detect user action on the reset button.	I	D		User reset. TP. PU required if connected to button. GND if not used.	GND
A11		PWRON		input. Detect a control command to start or stop the system.	I	D		Switch on control. TP (secondary general reset after 8 slow state and battery removal). Need external PU of 5KΩ.	VBAT
B14		NC		Not connected					
P7		NSLEEP1		Sleep request from device 1	I	D		Sleep request from processor 1. TP.	GND
G9		NSLEEP2		SLEEP request from device 2	I	D		Sleep request from processor 2. TP. Grounded if not used.	GND
D13		CLK256FS			O	D	0	Audio clock 256 FS. TP.	Floating

Table 1. TPS65950 Schematic Checklist (continued)

Ball Name	TPS65950 Pinlist	Default Configuration	SW Pin Muxing (Reg Name/Bit Name/Value)	Description	Type	A/D	Output Default Value	Recommended Connectivity	Connectivity When Function is not Used
F8		VMODE1		Digital voltage scaling linked with VDD1	I	D		Digital voltage scaling. Ground if not used.	GND
K11		BOOT0		Boot pin 0 (1)	IO	A/D		Boot selection. TP. 4 possibilities.	
J11		BOOT1		Boot pin 1 (1)	IO	A/D		Boot selection. TP. 4 possibilities.	
A10		REGEN		Enable signal for external LDO	Open drain	D	0	External LDO control. TP.	Floating
H8		MSECURE		Security and digital rights management	I	D		Secure mode: 1 to be active (RW of secure registers possible). Unsecure mode: 0. Only read is possible.	
N16	VREF	VREF		Reference voltage	POWER	A		Bandgap voltage. 1 uF cap between VREF and AGND.	
N15		AGND		Analog ground for reference voltage	POWER GND	A		Clean analog ground connected to 1 plane	
C4	I^2C SmartReflex™	I2C.SR.SDA		SmartReflex I^2C data	IO	D		Floating if not used	Floating
D6		VMODE2		Digital voltage scaling linked with VDD2	I	D		Digital voltage scaling. GND If not used.	GND
		I2C.SR.SCL		SmartReflex I^2C data	IO	D		GND if not used.	
D4	I^2C	I2C.CNTL.SDA		General-purpose I^2C data	IO	D			
D5		I2C.CNTL.SCL		General-purpose I^2C clock	I	D			
R1	PCM	PCM.VCK		Data clock (voice port)	IO	D		All voice PCM signals must be routed symetrically. TP.	Floating
T2		PCM.VDR		Data receive (voice port)	IO	D		All voice PCM signals must be routed symetrically. TP. Grounded if not used.	GND
T15		PCM.VDX		Data transmit (voice port)	IO	D		All voice PCM signals must be routed symetrically. TP.	Floating
R16		PCM.VFS		Frame synchro (voice port)	IO	D		All voice PCM signals must be routed symetrically. TP.	Floating
L3	TDM	I2S.CLK		Clock signal (audio port)	IO	D		All audio I2S signals must be routed symetrically. TP.	Floating
K6		I2S.SYNC		Synchronization signal (audio port)	IO	D		All audio I2S signals must be routed symetrically. TP.	Floating

(1) Output is used for PM bus to output data (for test).

Table 1. TPS65950 Schematic Checklist (continued)

Ball Name	TPS65950 Pinlist	Default Configuration	SW Pin Muxing (Reg Name/Bit Name/Value)	Description	Type	A/D	Output Default Value	Recommended Connectivity	Connectivity When Function is not Used
K4		I2S.DIN		Data receive (audio port)	I	D		All audio I2S signals must be routed symetrically. TP. Grounded if not used.	GND
K3		I2S.DOUT		Data transmit (audio port)	O	D		All audio I2S signals must be routed symetrically. TP.	Floating
E2	ANA.MIC	MIC.MAIN.P		Main microphone left input (P)	I	A		Route symmetrically with MIC.MAIN.M, shielded, with TDMA filtering cap and coupling capacitor. Cap to ground if not used.	Floating
F2		MIC.MAIN.M		Main microphone left input (M)	I	A		Route symmetrically with MIC.MAIN.P, shielded, with TDMA filtering cap and coupling capacitor. Cap to ground if not used.	Floating
G2		MIC.SUB.P		Main microphone right input (P)	I	A		Route symmetrically with MIC.SUB.M, shielded, with TDMA filtering cap and coupling capacitor. Cap to ground if not used.	Floating
		DIG.MIC.0		Digital microphone 0 input data	I	A		Digital microphone input. TP. Cap to ground if not used.	
H2		MIC.SUB.M		Main microphone right input (M)	I	A		Route symmetrically with MIC.SUB.P, shielded, with TDMA filtering cap and coupling capacitor. Cap to ground if not used.	Floating
		DIG.MIC.1		Digital microphone 1 input data	I	A		Digital microphone input. TP. Cap to ground if not used.	
E3	Headset microphone	HSMIC.P		Headset microphone input (P)	I	A		Route symmetrically with HSMIC.M, shielded, with TDMA filtering cap and coupling capacitor. Cap to ground if not used.	Floating
F3		HSMIC.M		Headset microphone input (M)	I	A		Route symmetrically with HSMIC.P, shielded, with TDMA filtering cap and coupling capacitor. Cap to ground if not used.	Floating
D10	Hands-free	VBAT.LEFT		Battery voltage input	POWER	A		Filtering capacitor of 1 uF. Connected to VBAT if not used.	VBAT
D9		VBAT.LEFT		Battery voltage input	POWER	A		Filtering capacitor of 1 uF. Connected to VBAT if not used.	VBAT
B9		IHF.LEFT.P		Hands-free left speaker output (P)	O	A		Serial Ferrite cheap bead (high impedance at high frequency and low impedance at low frequency) or inductor + filtering 1 nF cap	Floating

Table 1. TPS65950 Schematic Checklist (continued)

Ball Name	TPS65950 Pinlist	Default Configuration	SW Pin Muxing (Reg Name/Bit Name/Value)	Description	Type	A/D	Output Default Value	Recommended Connectivity	Connectivity When Function is not Used
B10		IHF.LEFT.M		Hands-free left speaker output (M)	O	A		Serial Ferrite cheap bead (high impedance at high frequency and low impedance at low frequency) or inductor + filtering 1 nF cap	Floating
C10		GND.LEFT		GND	POWER GND	A		Ground connected to 1 plane	GND
C9		GND.LEFT		GND	POWER GND	A		Ground connected to 1 plane	GND
D12		VBAT.RIGHT		Battery voltage input	POWER	A		Filtering capacitor of 1 uF. Connected to VBAT if not used.	VBAT
D11		VBAT.RIGHT		Battery voltage input	POWER	A		Filtering capacitor of 1 uF. Connected to VBAT if not used.	VBAT
B11		IHF.RIGHT.P		Hands-free right speaker output (P)	O	A		Serial Ferrite cheap bead (high impedance at high frequency and low impedance at low frequency) or inductor + filtering 1 nF cap	Floating
B12		IHF.RIGHT.M		Hands-free right speaker output (M)	O	A		Serial Ferrite cheap bead (high impedance at high frequency and low impedance at low frequency) or inductor + filtering 1 nF cap	Floating
C12		GND.RIGHT		GND	POWER GND	A		Ground connected to 1 plane	GND
C11		GND.RIGHT		GND	POWER GND	A		Ground connected to 1 plane	GND
A6	Earpiece	EAR.P		Earpiece output differential output (P)	O	A		Route symetrically to EAR.M and add TDMA filtering cap	Floating
A7		EAR.M		Earpiece output differential output (M)	O	A		Route symetrically to EAR.P and add TDMA filtering cap	Floating
B4	Headset	HSOL		Differential/single-ended headset left output	O	A		Add decoupling 22 uF cap and add TDMA filtering cap. For anti-pop system, external FET need driven by GPIO6.	Floating
B7		PreDriv.LEFT		Predriver output left P for external class-D amplifier	O	A		Audio output to connect external device through coupling capacitor of at least 1 uF	Floating
		VMID			POWER	A		Headset output common mode voltage for specific applicative case without coupling cap. Controlled by Predriv.LEFT register.	
B5		HSOR		Differential/single-ended headset right output (P)	O	A		Add decoupling 22 uF cap and add TDMA filtering cap. For anti-pop system, external FET must be driven by GPIO6.	Floating

Table 1. TPS65950 Schematic Checklist (continued)

Ball Name	TPS65950 Pinlist	Default Configuration	SW Pin Muxing (Reg Name/Bit Name/Value)	Description	Type	A/D	Output Default Value	Recommended Connectivity	Connectivity When Function is not Used
B8		PreDriv.RIGHT		Predriver output right P for external class-D amplifier	O	A		Audio output to connect external device through coupling capacitor of at least 1 uF	GND
		ADCIN7		General-purpose ADC input 7	I	A		General-purpose. Prescaler integrated. Limited input voltage 2.5 V. Grounded if not used.	
F1	AUX input	AUXL		Auxiliary audio input left	I	A		Add TDMA filtering capacitor and 100 nF coupling cap. Cap to ground if not used.	Floating
G1		AUXR		Auxiliary audio input right	I	A		Add TDMA filtering capacitor and 100 nF coupling cap. Cap to ground if not used.	Floating
D1	VMIC BIAS	MICBIAS1.OUT		Analog microphone bias 1	POWER	A		Serial resistor required for filtering cap higher than 200 pF	Floating
		VMIC1.OUT		Digital microphone power supply 1	POWER	A		Digital microphone biasing. Add filtering capacitor.	
D2		MICBIAS2.OUT		Analog microphone bias 2	POWER	A		Serial resistor required for filtering cap higher than 200 pF	Floating
		VMIC2.OUT		Digital microphone power supply 2	POWER	A		Digital microphone biasing. Add filtering capacitor.	
E4		VHSMIC.OUT		Headset microphone bias	POWER	A		HS microphone biasing through serial resistor	Floating
D3		MICBIAS.GND		Dedicated ground for microphones	POWER GND			Connected to AGND	GND
J4/J6/J7/J8/E5		AVSS1		Analog ground	POWER GND	A		Analog ground connected to 1 plane	
R10		AVSS2		Analog ground	POWER GND	A		Analog ground connected to 1 plane	
M 15		AVSS3		Analog ground	POWER GND	A		Analog ground connected to 1 plane	
C7		AVSS4		Analog ground	POWER GND	A		Analog ground connected to 1 plane	
B1	Headset UART	UART1.TXD		Headset UART transmit data	Open drain	D		External PU can be required to 1.8 or 3.3 V. Floating if not used.	Floating
D8		GPIO8		GPIO8	I	D		Floating if not used	Floating
		UART1.RXD	MCPC_CTRL/HS_UART=0b1	Headset UART receive data/switch detection	I	D		Floating if not used	

Table 1. TPS65950 Schematic Checklist (continued)

Ball Name	TPS65950 Pinlist	Default Configuration	SW Pin Muxing (Reg Name/Bit Name/Value)	Description	Type	A/D	Output Default Value	Recommended Connectivity	Connectivity When Function is not Used
N11	MCPC	RTSO/CLK64K.OUT/BERCLK.OUT	CARKIT_ANA_CTRL/SEL_MADC_MCPC=b0	Ready to send output/64-kHz output clock/BER clock out in test mode	OD	D		External PU can be required to 1.8 or 3.3 V. Serial resistance between 22 and 100 Ω + diode.	Floating
		ADCIN5	CARKIT_ANA_CTRL/SEL_MADC_MCPC=b1	Genera-purpose ADC input 5	I	A		General-purpose. Prescaler integrated. Limited input voltage 2.5 V. Grounded if not used.	
P11		CTSI/BERDATA.OUT	CARKIT_ANA_CTRL/SEL_MADC_MCPC=b0	Clear to send input/BERDATAOUT in test mode	OD/CMOS/IO	D		External PU can be required to 1.8 or 3.3 V. Serial 50 Ω RRTSO resistor.	GND
		ADCIN3	CARKIT_ANA_CTRL/SEL_MADC_MCPC=b1	General-purpose ADC input 3	I	A		General-purpose. Prescaler integrated. Limited input voltage 2.5 V. Grounded if not used.	
N8		TXAF	CARKIT_ANA_CTRL/SEL_MADC_MCPC=b0		I	A		Add 100 nF coupling capacitor to ground if not used.	GND
		ADCIN4	CARKIT_ANA_CTRL/SEL_MADC_MCPC=b1	General-purpose ADC input 4	I	A		General-purpose. Prescaler integrated. Limited input voltage 2.5 V.dd 100 nF coupling capacitor to ground if not used.	
N9		RXAF	CARKIT_ANA_CTRL/SEL_MADC_MCPC=b0		O	A		Add 1 uF coupling capacitor. Floating if not used.	Floating
		ADCIN6	CARKIT_ANA_CTRL/SEL_MADC_MCPC=b1	General-purpose ADC input 6	I	A		General-purpose. Prescaler integrated. Limited input voltage 2.5 V. Floating if not used.	
L10		MANU		Manufacturer pin	I	D		Floating if not required	Floating
N10	CLOCK	32KCLKOUT		Buffered output of the 32-kHz digital clock	O	D		No more than 40-pF load programmable	Floating
P16		32KXIN		Input of the 32-kHz oscillator	I	A		External capacitor to AGND to add. Value of this cap plus 5 pF internal must equal oscillator cap specification, symetrically to 32KXOUT.	

Table 1. TPS65950 Schematic Checklist (continued)

Ball Name	TPS65950 Pinlist	Default Configuration	SW Pin Muxing (Reg Name/Bit Name/Value)	Description	Type	A/D	Output Default Value	Recommended Connectivity	Connectivity When Function is not Used
P15		32KXOUT		Output of the 32-kHz oscillator	O	A		External capacitor to AGND to add. Value of this cap plus 5 pF internal must equal oscillator cap specification, symetrically to 32KXIN.	Floating
A14		HFCLKIN		Input of the digital (or sine) high-speed clock	I	A		For sine wave, no more than 1.45 Vpp amplitude	
R12		HFCLKOUT		High-speed clock output	O	D		No more than 40-pF load programmable	Floating
R8	USB PHY	VBUS		VBUS power rail	POWER	A		Directly connected to USB connector without resistive add. 4.7 uF cap connected between VBUS and VSSP.	GND
T10		DP/UART3.RXD		USB data P/USB carkit receive data/UART3 receive data	IO	A		Directly connected to USB symetrically with TXD	Floating
T11		DN/UART3.TXD		USB data N/USB Carkit transmit data/UART3 transmit data	IO	A		Directly connected to USB symetrically with RXD	Floating
R11		ID		USB ID	IO	A		Floating	Floating
L15	ULPI	UCLK		High-speed USB clock	IO	D		Connected to OMAP. Floating if not used.	Floating
L14		STP	IFC_CTRL/FSLSSERIALMODE_3PIN = b0	High-speed USB stop	I	D		Connected to OMAP. Floating if not used.	Floating
		GPIO9		GPIO9	IO	D			
L13		DIR		High-speed USB direction	O	D		Connected to OMAP. Floating if not used.	Floating
		GPIO10		GPIO10	IO	D			
M13		NXT	IFC_CTRL/FSLSSERIALMODE_3PIN = b0	High-speed USB next	O	D		Connected to OMAP. Floating if not used.	Floating
		GPIO11		GPIO11	IO	D			

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K14		DATA0	IFC_CTRL/FSLSSERIALMODE_3PIN = b0, MCPC_CTRL/RTSCTSSW = b0	High-speed USB data0	IO	D		Connected to OMAP. Floating if not used.	Floating
		UART4.TXD	IFC_CTRL/FSLSSERIALMODE_3PIN = b1, MCPC_CTRL/RTSCTSSW = b1	UART4.TXD	I	D		Connected to OMAP. Floating if not used.	
K13		DATA1	IFC_CTRL/FSLSSERIALMODE_3PIN = b0, MCPC_CTRL/RTSCTSSW = b0	High-speed USB data1	IO	D		Connected to OMAP. Floating if not used.	Floating
		UART4.RXD	IFC_CTRL/FSLSSERIALMODE_3PIN = b1, MCPC_CTRL/RTSCTSSW = b1	UART4.RXD	O	D		Connected to OMAP. Floating if not used.	
J14		DATA2	IFC_CTRL/FSLSSERIALMODE_3PIN = b0, MCPC_CTRL/RTSCTSSW = b0	High-speed USB data2	IO	D		Connected to OMAP. Floating if not used.	Floating
		UART4.RTSI	IFC_CTRL/FSLSSERIALMODE_3PIN = b1, MCPC_CTRL/RTSCTSSW = b1	UART4.RTSI	I	D		Connected to OMAP. Floating if not used.	

Table 1. TPS65950 Schematic Checklist (continued)

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J13		DATA3	IFC_CTRL/FSLSSERIALMODE_3PIN = b0, MCPC_CTRL/RTSCTSSW = b0	High-speed USB data3	IO	D		Connected to OMAP. Floating if not used.	Floating
		UART4.CTSO	IFC_CTRL/FSLSSERIALMODE_3PIN = b1, MCPC_CTRL/RTSCTSSW = b1	UART4.CTSO	O	D		Connected to OMAP. Floating if not used.	
		GPIO12		GPIO12	IO	D			
G14		DATA4	IFC_CTRL/FSLSSERIALMODE_3PIN = b0	High-speed USB data4	IO	D		Connected to OMAP. Floating if not used.	Floating
		GPIO14		GPIO14	IO	D			
G13		DATA5	IFC_CTRL/FSLSSERIALMODE_3PIN = b0	High-speed USB data5	IO	D		Connected to OMAP. Floating if not used.	Floating
		GPIO3		GPIO3	IO	D			
F14		DATA6	IFC_CTRL/FSLSSERIALMODE_3PIN = b0	High-speed USB data6	IO	D		Connected to OMAP. Floating if not used.	Floating
		GPIO4		GPIO4	IO	D			
F13		DATA7	IFC_CTRL/FSLSSERIALMODE_3PIN = b0	High-speed USB data7	IO	D		Connected to OMAP. Floating if not used.	Floating
		GPIO5		GPIO5	IO	D			
T16	TEST	TEST.RESET		Reset T2 device (except power state-machine)	I	A/D		PD, cannot be used for application !	GND
T1		TESTV1		Analog test	IO	A		TP or floating if not used	Floating
A16		TESTV2		Analog test	IO	A		TP or floating if not used	Floating

Table 1. TPS65950 Schematic Checklist (continued)

Ball Name	TPS65950 Pinlist	Default Configuration	SW Pin Muxing (Reg Name/Bit Name/Value)	Description	Type	A/D	Output Default Value	Recommended Connectivity	Connectivity When Function is not Used
A1		TEST		Selection between JTAG mode and application mode for JTAG/GPIOs (with PU or PD)	I	D		Connected to VIO for JTAG use or floating as internal PD if JTAG not used	Floating
A15		JTAG.TDI/ BERDATA		JTAG.TDI/BERDATA	I	D		Grounded if not used	GND
B16		JTAG.TCK/ BERCLK		JTAG.TCK/BERCLK	I	D		Grounded if not used	GND
R7	USB CP	CP.IN		Charge pump input voltage	POWER	A		Cap of 10 uF. Cap must be as close as possible to device.	VBAT
T7		CP.CAPP		Charge pump flying capacitor P	O	A		Connected to CP.CAPM by a cap of 2.2 uF	Floating
T6		CP.CAPM		Charge pump flying capacitor M	O	A		Connected to CP.CAPP by a cap of 2.2 uF	Floating
R6		CP.GND		Charge pump ground	POWER GND	A		Connected to ground	GND
R9	VBAT.USB	VBAT.USB		USB LDOs (VINTUSB1P5, VINTUSB1P8, VUSB.3P1) VBAT	POWER	A		Cap of 1 uF. Cap must be as close as possible to device.	VBAT
P9	USB LDO	VUSB.3P1		USB LDO output	POWER	A		Cap of 1 uF. Do not use externally.	
L1	VAUX1	VAUX12S.IN		VAUX1/VAUX2/VSIM LDO input voltage	POWER	A		Cap of 1 uF. Cap must be as close as possible to device.	VBAT
M2		VAUX1.OUT		VAUX1 LDO output voltage	POWER	A		Cap of 1 uF	Floating
M3	VAUX2	VAUX2.OUT		VAUX2 LDO output voltage	POWER	A		Cap of 1 uF	Floating
H15	VPLLA3R	VPLLA3R.IN		Input for VPLL1, VPLL2, VAUX3, VRTC LDOs	POWER	A		Cap of 1 uF. Important to get separate filtering.Cap must be as close as possible to device.	VBAT
K16	VRTC	VRTC.OUT		VRTC internal LDO output (internal use only)	POWER	A		Cap of 1 uF. Do not use externally.	
H14	VPLL1	VPLL1.OUT		LDO output voltage	POWER	A		Cap of 1 uF	Floating
J15	VPLL2	VSDI.CSI.OUT		oRegulator output voltage	POWER	A		Cap of 1 uF	Floating

Table 1. TPS65950 Schematic Checklist (continued)

Ball Name	TPS65950 Pinlist	Default Configuration	SW Pin Muxing (Reg Name/Bit Name/Value)	Description	Type	A/D	Output Default Value	Recommended Connectivity	Connectivity When Function is not Used
G16	VAUX3	VAUX3.OUT		VAUX3 LDO output voltage	POWER	A		Cap of 1 uF	Floating
B2	VAUX4	VAUX4.IN		VAUX4 LDO input voltage	POWER	A		Cap of 1 uF. Cap must be as close as possible to device.	VBAT
B3		VAUX4.OUT		VAUX4 LDO output voltage	POWER	A		Cap of 1 uF	Floating
C1	VMMC1	VMMC1.IN		VMMC1 LDO input voltage	POWER	A		Cap of 1 uF. Cap must be as close as possible to device.	VBAT
C2		VMMC1.OUT		VMMC1 LDO output voltage	POWER	A		Cap of 1 uF	Floating
A3	VMMC2	VMMC2.IN		VMMC2 LDO input voltage	POWER	A		Cap of 1 uF. Cap must be as close as possible to device.	VBAT
A4		VMMC2.OUT		VMMC2 LDO output voltage	POWER	A		Cap of 1 uF	Floating
K2	VSIM	VSIM.OUT		VSIM LDO output voltage	POWER	A		Cap of 1 uF	Floating
P8	VINTUSB1P5	VINTUSB1P5.OUT		VINTUSB1P5 internal LDO output (Internal use only)	POWER	A		Cap of 1 uF. Do not use externally.	Floating
P10	VINTUSB1P8	VINTUSB1P8.OUT		VINTUSB1P8 internal LDO output (Internal use only)	POWER	A		Cap of 1 uF. Do not use externally.	Floating
K1	Video DAC	VDAC.IN		Input for VDAC, VINTANA1, and VINTANA2 LDOs	POWER	A		Cap of 1 uF. Cap must be as close as possible to device.	VBAT
L2		VDAC.OUT		Regulator output voltage	POWER	A		Cap of 1 uF	Floating
K15	VINT	VINT.IN		Input for VINTDIG LDO	POWER	A		Cap of 1 uF. Cap must be as close as possible to device.	VBAT
H3	VINTANA1	VINTANA1.OUT		VINTANA1 internal LDO output (internal use only)	POWER	A		Cap of 1 uF. Do not use externally.	
J2	VINTANA2	VINTANA2.OUT		VINTANA2 internal LDO output (internal use only)	POWER	A		Cap of 1 uF. Do not use externally.	
B6		VINTANA2.OUT		VINTANA2 internal LDO output (internal use only)	POWER	A		Cap of 1 uF. Do not use externally.	

Table 1. TPS65950 Schematic Checklist (continued)

Ball Name	TPS65950 Pinlist	Default Configuration	SW Pin Muxing (Reg Name/Bit Name/Value)	Description	Type	A/D	Output Default Value	Recommended Connectivity	Connectivity When Function is not Used
L16	VINTDIG	VINTDIG.OUT		VINTDIG internal LDO output (internal use only)	POWER	A		Cap of 1 uF. Do not use externally.	
E15	VDD1	VDD1.IN		VDD1 DCDC input voltage	POWER	A		Cap of 10 uF. Cap must be as close as possible to device.	VBAT
E14		VDD1.IN		VDD1 DCDC input voltage	POWER	A			VBAT
D14		VDD1.IN		VDD1 DCDC input voltage	POWER	A			VBAT
D16		VDD1.SW		VDD1 DCDC switch	O	A		L= 1uH to the device pad and C = 10 uF on the other end of inductor.	Floating
D15		VDD1.SW		VDD1 DCDC switch	O	A			
C14		VDD1.SW		VDD1 DCDC switch	O	A			
E13		VDD1.FB		VDD1 DCDC output voltage (feedback)	I	A		Connect to the LC circuit (capacitor end).	GND
C16		VDD1.GND		VDD1 DCDC ground	POWER GND	A		Connected to ground	GND
C15		VDD1.GND		VDD1 DCDC ground	POWER GND	A		Connected to ground	GND
B15		VDD1.GND		VDD1 DCDC ground	POWER GND	A		Connected to ground	GND
R13	VDD2	VDD2.IN		VDD2 DCDC input voltage	POWER	A		Cap of 10 uF. Cap must be as close as possible to device.	VBAT
P14		VDD2.IN		VDD2 DCDC input voltage	POWER	A			VBAT
N13		VDD2.FB		VDD2 DCDC output voltage (feedback)	I	A		Connect to the LC circuit (capacitor end).	GND
T13		VDD2.SW		VDD2 DCDC switch	O	A		L= 1uH to the device pad and C = 10 uF on the other end of inductor.	Floating
R14		VDD2.SW		VDD2 DCDC switch	O	A			
T14		VDD2.GND		VDD2 DCDC ground	POWER GND	A		Connected to ground	GND

Table 1. TPS65950 Schematic Checklist (continued)

Ball Name	TPS65950 Pinlist	Default Configuration	SW Pin Muxing (Reg Name/Bit Name/Value)	Description	Type	A/D	Output Default Value	Recommended Connectivity	Connectivity When Function is not Used
R15		VDD2.GND		VDD2 DCDC ground	POWER GND	A		Connected to ground	GND
P3	VIO	VIO.IN		VIO DCDC input voltage	POWER	A		Cap of 10 uF. Cap must be as close as possible to device.	VBAT
R4		VIO.IN		VIO DCDC input voltage	POWER	A			VBAT
N3		VIO.FB		VIO DCDC output voltage (feedback)	I	A		Connect to the LC circuit (capacitor end).	GND
R3		VIO.SW		VIO DCDC switch	O	A		L= 1uH to the device pad and C = 10 uF on the other end of inductor	Floating
T4		VIO.SW		VIO DCDC switch	O	A			
R2		VIO.GND		VIO DCDC ground	POWER GND	A		Connected to ground	GND
T3		VIO.GND		VIO DCDC ground	POWER GND	A		Connected to ground	GND
M14	Backup BAT	BKBAT		Backup battery	POWER	A		2.5- to 3.2-V backup battery. Grounded if not used.	GND
C8	Digital VDD	IO.1P8		TPS65950 I/O input	POWER	A		To connect to VIO. Add filtering cap.	
H13/H9/H10/H11	Digital ground	DGND		Digital ground	POWER GND	A		Connected to ground	GND
F16	LED driver	LEDGND		LED driver ground	POWER GND	A		Connected to ground	GND
G11		GPIO13		GPIO13	IO	D		Can be left floating if not used	Floating
		LEDSYNC		LED synchronization input	I	D		TP. Can be left floating if not used.	
F15		LEDA		LED leg A	Open drain	A		Do not connect to LEDB. 2.5 times LED drive.	Floating
		VIBRA.P		H-bridge vibrator P	Open drain	A		Connected differentially with VIBRA.M. Floating if not used.	
G15		LEDB		LED leg B	Open drain	A		Do not connect to LEDA.	Floating
		VIBRA.M		H-bridge vibrator M	Open drain	A		Connected differentially with VIBRA.P. Floating if not used.	
G8	Keypad	KPD.C0		Keypad column 0	Open drain	D		Floating if not used	Floating
H7		KPD.C1		Keypad column 1	Open drain	D		Floating if not used	Floating
G6		KPD.C2		Keypad column 2	Open drain	D		Floating if not used	Floating

Table 1. TPS65950 Schematic Checklist (continued)

Ball Name	TPS65950 Pinlist	Default Configuration	SW Pin Muxing (Reg Name/Bit Name/Value)	Description	Type	A/D	Output Default Value	Recommended Connectivity	Connectivity When Function is not Used
F7		KPD.C3		Keypad column 3	Open drain	D		Floating if not used	Floating
G7		KPD.C4		Keypad column 4	Open drain	D		Floating if not used	Floating
F4		KPD.C5		Keypad column 5	Open drain	D		Floating if not used	Floating
H6		KPD.C6		Keypad column 6	Open drain	D		Floating if not used	Floating
G4		KPD.C7		Keypad column 7	Open drain	D		Floating if not used	Floating
K9		KPD.R0		Keypad row 0	I	D		Floating if not used	Floating
K8		KPD.R1		Keypad row 1	I	D		Floating if not used	Floating
L8		KPD.R2		Keypad row 2	I	D		Floating if not used	Floating
K7		KPD.R3		Keypad row 3	I	D		Floating if not used	Floating
L9		KPD.R4		Keypad row 4	I	D		Floating if not used	Floating
J10		KPD.R5		Keypad row 5	I	D		Floating if not used	Floating
K10		KPD.R6		Keypad row 6	I	D		Floating if not used	Floating
L7		KPD.R7		Keypad row 7	I	D		Floating if not used	Floating
C3	Bluetooth™ (BT)	GPIO16		GPIO16	IO	D		Floating if not used	Floating
		BT.PCM.VDR		Bluetooth PCM receive data	IO	D		All BT PCM signals must be routed symetrically. TP.	
		DIG.MIC.CLK0		Digital microphone clock 0	O	D		Can be left floating if not used	
C5	GPIO17	GPIO17		GPIO17	IO	D		Floating if not used	Floating
		BT.PCM.VDX		BT PCM transmit data	IO	D		All BT PCM signals must be routed symetrically. TP.	
		DIG.MIC.CLK1		Digital microphone clock 1	O	D		Can be left floating if not used	
A2	RFID	RFID.EN		Enable for the RFID device	O	D	0	Can be left floating if not used	Floating

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