

–36V, –200mA, ULTRALOW-NOISE, NEGATIVE LINEAR REGULATOR

FEATURES

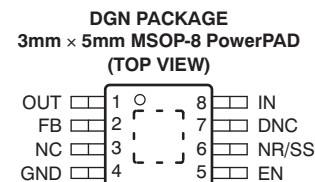
- **Input Voltage Range:** –3V to –36V
- **Noise:**
 - $14\mu\text{V}_{\text{RMS}}$ (20Hz to 20kHz)
 - $15.1\mu\text{V}_{\text{RMS}}$ (10Hz to 100kHz)
- **Power-Supply Ripple Rejection:**
 - 72dB (120Hz)
 - $\geq 55\text{dB}$ (10Hz to 700kHz)
- **Adjustable Output:** –1.18V to –35V
- **Maximum Output Current:** 200mA
- **Dropout Voltage:** 216mV at 100mA
- **Stable with Ceramic Capacitors** $\geq 2.2\mu\text{F}$
- **CMOS Logic-Level-Compatible Enable Pin**
- **Built-In, Fixed, Current-Limit and Thermal Shutdown Protection**
- **Available in High Thermal Performance MSOP-8 PowerPAD™ Package**

APPLICATIONS

- **Supply Rails for Op Amps, DACs, ADCs, and Other High-Precision Analog Circuitry**
- **Audio**
- **Post DC/DC Converter Regulation and Ripple Filtering**
- **Test and Measurement**
- **RX, TX, and PA Circuitry**
- **Industrial Instrumentation**
- **Base Stations and Telecom Infrastructure**
- **–12V and –24V Industrial Buses**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**



DESCRIPTION

The TPS7A3001 is a negative, high-voltage (–36V), ultralow-noise ($15.1\mu\text{V}_{\text{RMS}}$, 72dB PSRR) linear regulator capable of sourcing a maximum load of 200mA.

These linear regulators include a CMOS logic-level-compatible enable pin and capacitor-programmable soft-start function that allows for customized power-management schemes. Other features available include built-in current limit and thermal shutdown protection to safeguard the device and system during fault conditions.

The TPS7A3001 is designed using bipolar technology, and is ideal for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This design makes it an excellent choice to power operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other high-performance analog circuitry.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

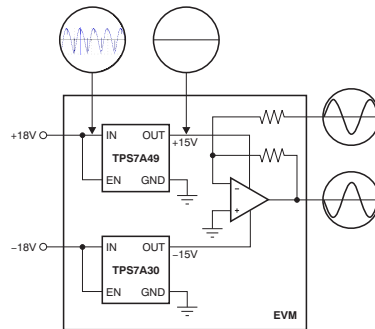
PowerPAD is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

In addition, the TPS7A3001 of linear regulators is suitable for post dc/dc converter regulation. By filtering out the output voltage ripple inherent to dc/dc switching conversion, maximum system performance is provided in sensitive instrumentation, test and measurement, audio, and RF applications.

For applications where positive and negative high-performance rails are required, consider TI's [TPS7A49xx](#) family of positive high-voltage, ultralow-noise linear regulators.

Figure 1. Typical Application



Post DC/DC Converter Regulation for High-Performance Analog Circuitry



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

T _J	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–55°C to 125°C	DGN	TPS7A3001MDGNTEP	PXCM	V62/11619-01XE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range (unless otherwise noted).

		VALUE		
		MIN	MAX	UNIT
Voltage	IN pin to GND pin	–36	+0.3	V
	OUT pin to GND pin	–33	+0.3	V
	OUT pin to IN pin	–0.3	+36	V
	FB pin to GND pin	–2	+0.3	V
	FB pin to IN pin	–0.3	+36	V
	EN pin to IN pin	–0.3	+36	V
	EN pin to GND pin	–36	+36	V
	NR/SS pin to IN pin	–0.3	+36	V
	NR/SS pin to GND pin	–2	+0.3	V
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T _J	–55	+135	°C
	Storage, T _{stg}	–65	+150	°C
Electrostatic discharge rating	Human body model (HBM)		1500	V
	Charged device model (CDM)		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		TPS7A3001		UNITS
		DGN		
		8 PINS		
θ _{JA}	Junction-to-ambient thermal resistance	69.3		°C/W
θ _{JC(top)}	Junction-to-case(top) thermal resistance	40.3		
θ _{JB}	Junction-to-board thermal resistance	39.0		
ψ _{JT}	Junction-to-top characterization parameter	2.4		
ψ _{JB}	Junction-to-board characterization parameter	38.7		
θ _{JC(bottom)}	Junction-to-case(bottom) thermal resistance	17.8		

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com/lit/zip/spr953).

ELECTRICAL CHARACTERISTICS⁽¹⁾

At $T_J = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $|V_{IN}| = |V_{OUT(NOM)}| + 1.0\text{V}$ or $|V_{IN}| = 3.0\text{V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 1\text{mA}$, $C_{IN} = 2.2\mu\text{F}$, $C_{OUT} = 2.2\mu\text{F}$, $C_{NR/SS} = 0\text{nF}$, and the FB pin tied to OUT, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		-36.0		-3.0	V
V_{REF}	Internal reference	$V_{NR/SS} = V_{REF}$	-1.22	-1.184	-1.142	V
V_{OUT}	Output voltage range ⁽²⁾	$ V_{IN} \geq V_{OUT(NOM)} + 1.0\text{V}$	-35.0		V_{REF}	V
	Nominal accuracy	$T_J = +25^\circ\text{C}$, $ V_{IN} = V_{OUT(NOM)} + 0.5\text{V}$	-1.5		+1.5	% V_{OUT}
	Overall accuracy	$ V_{OUT(NOM)} + 1.0\text{V} \leq V_{IN} \leq 35\text{V}$ $1\text{mA} \leq I_{OUT} \leq 200\text{mA}$	-2.85		+2.85	% V_{OUT}
$\left \frac{\Delta V_{OUT}(\Delta V_{IN})}{V_{OUT(NOM)}} \right $	Line regulation	$T_J = +25^\circ\text{C}$, $ V_{OUT(NOM)} + 1.0\text{V} \leq V_{IN} \leq 35\text{V}$		0.14		% V_{OUT}
$\left \frac{\Delta V_{OUT}(\Delta I_{OUT})}{V_{OUT(NOM)}} \right $	Load regulation	$T_J = +25^\circ\text{C}$, $1\text{mA} \leq I_{OUT} \leq 200\text{mA}$		0.04		% V_{OUT}
$ V_{DO} $	Dropout voltage	$V_{IN} = 95\% V_{OUT(NOM)}$, $I_{OUT} = 100\text{mA}$		216		mV
		$V_{IN} = 95\% V_{OUT(NOM)}$, $I_{OUT} = 200\text{mA}$		325	600	mV
I_{LIM}	Current limit	$V_{OUT} = 90\% V_{OUT(NOM)}$	220	330	500	mA
I_{GND}	Ground current	$I_{OUT} = 0\text{mA}$		55	100	μA
		$I_{OUT} = 100\text{mA}$		950		μA
$ I_{SHDN} $	Shutdown supply current	$V_{EN} = +0.4\text{V}$		1.0	3.0	μA
		$V_{EN} = -0.4\text{V}$		1.0	3.0	μA
I_{FB}	Feedback current ⁽³⁾			14	100	nA
$ I_{EN} $	Enable current	$V_{EN} = V_{IN} = V_{OUT(NOM)} + 1.0\text{V}$		0.48	1.0	μA
		$V_{IN} = V_{EN} = -35\text{V}$		0.51	1.0	μA
		$V_{IN} = -35\text{V}$, $V_{EN} = +15\text{V}$		0.50	1.2	μA
V_{+EN_HI}	Positive enable high-level voltage	$T_J = -55^\circ\text{C}$ to $+125^\circ\text{C}$	+2.0		+15	V
V_{+EN_LO}	Positive enable low-level voltage		0		+0.4	V
V_{-EN_HI}	Negative enable high-level voltage		V_{IN}		-2.0	V
V_{-EN_LO}	Negative enable low-level voltage		-0.4		0	V
V_{NOISE}	Output noise voltage	$V_{IN} = -3\text{V}$, $V_{OUT(NOM)} = V_{REF}$, $C_{OUT} = 10\mu\text{F}$, $C_{NR/SS} = 10\text{nF}$, $BW = 10\text{Hz}$ to 100kHz		15.1		μV_{RMS}
		$V_{IN} = -6.2\text{V}$, $V_{OUT(NOM)} = -5\text{V}$, $C_{OUT} = 10\mu\text{F}$, $C_{NR/SS} = C_{BYP}^{(4)} = 10\text{nF}$, $BW = 10\text{Hz}$ to 100kHz		17.5		μV_{RMS}
PSRR	Power-supply rejection ratio	$V_{IN} = -6.2\text{V}$, $V_{OUT(NOM)} = -5\text{V}$, $C_{OUT} = 10\mu\text{F}$, $C_{NR/SS} = C_{BYP}^{(4)} = 10\text{nF}$, $f = 120\text{Hz}$		72		dB
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		+170		$^\circ\text{C}$
		Reset, temperature decreasing		+150		$^\circ\text{C}$
T_J	Operating junction temperature range		-55		+125	$^\circ\text{C}$

(1) At operating conditions, $V_{IN} \leq 0\text{V}$, $V_{OUT(NOM)} \leq V_{REF} \leq 0\text{V}$. At regulation, $V_{IN} \leq V_{OUT(NOM)} - |V_{DO}|$. $I_{OUT} > 0$ flows from OUT to IN.

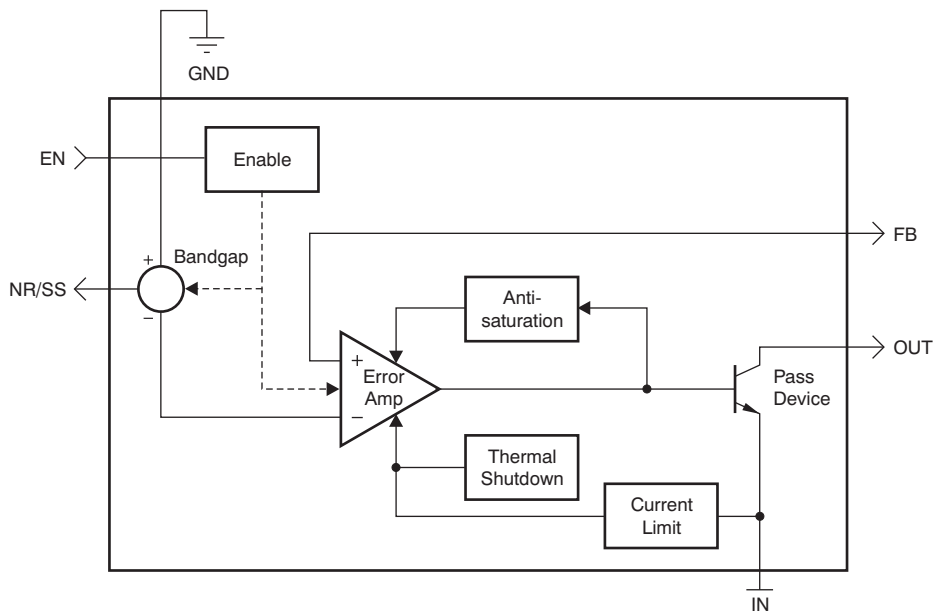
(2) To ensure stability at no load conditions, a current from the feedback resistive network equal to or greater than $5\mu\text{A}$ is required.

(3) $I_{FB} > 0$ flows into the device.

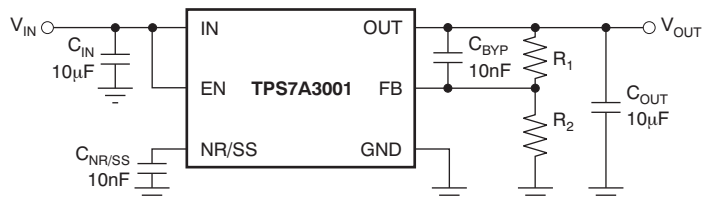
(4) C_{BYP} refers to a bypass capacitor connected to the FB and OUT pins.

DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUIT



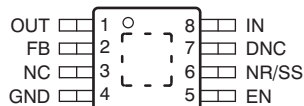
Where: $\frac{V_{OUT}}{R_1 + R_2} \geq 5\mu A$, and

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$$

Maximize PSRR Performance and Minimize RMS Noise

PIN CONFIGURATION

DGN PACKAGE MSOP-8 (TOP VIEW)



PIN DESCRIPTIONS

NAME	NO.	DESCRIPTION
OUT	1	Regulator output. A capacitor $\geq 2.2\mu\text{F}$ must be tied from this pin to ground to assure stability.
FB	2	This pin is the input to the control-loop error amplifier. It is used to set the output voltage of the device.
NC	3	Not internally connected. This pin must either be left open or tied to GND.
GND	4	Ground
EN	5	This pin turns the regulator on or off. If $V_{\text{EN}} \geq V_{+\text{EN_HI}}$ or $V_{\text{EN}} \leq V_{-\text{EN_HI}}$, the regulator is enabled. If $V_{+\text{EN_LO}} \geq V_{\text{EN}} \geq V_{-\text{EN_LO}}$, the regulator is disabled. The EN pin can be connected to IN, if not used. $ V_{\text{EN}} \leq V_{\text{IN}} $.
NR/SS	6	Noise reduction pin. Connecting an external capacitor to this pin bypasses noise generated by the internal bandgap. This capacitor allows RMS noise to be reduced to very low levels and also controls the soft-start function.
DNC	7	DO NOT CONNECT. Do not route this pin to any electrical net, not even GND or IN.
IN	8	Input supply
PowerPAD		Must either be left open or tied to GND. Solder to printed circuit board (PCB) plane to enhance thermal performance.

TYPICAL CHARACTERISTICS

At $T_J = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $|V_{IN}| = |V_{OUT(NOM)}| + 1.0\text{V}$ or $|V_{IN}| = 3.0\text{V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 1\text{mA}$, $C_{IN} = 2.2\mu\text{F}$, $C_{OUT} = 2.2\mu\text{F}$, $C_{NR/SS} = 0\text{nF}$, and the FB pin tied to OUT, unless otherwise noted.

FEEDBACK VOLTAGE vs INPUT VOLTAGE

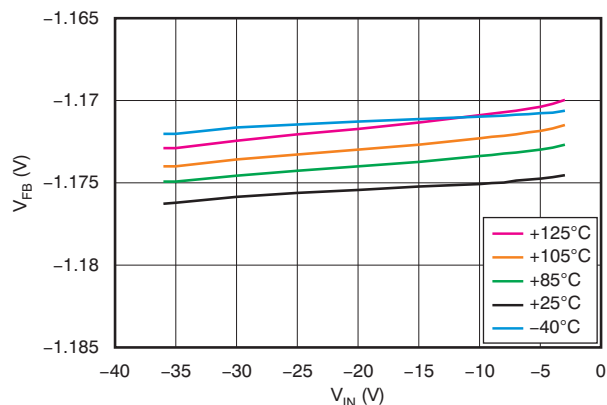


Figure 2.

FEEDBACK CURRENT vs TEMPERATURE

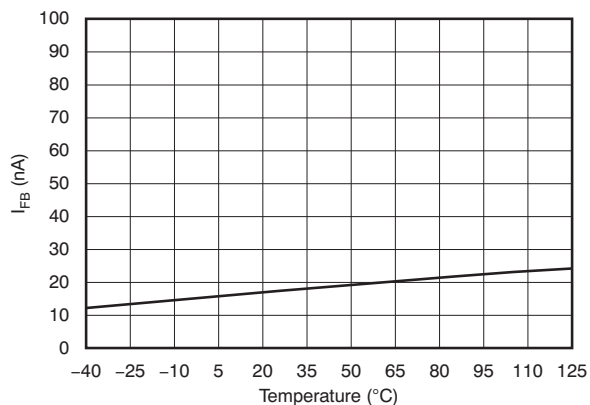


Figure 3.

GROUND CURRENT vs INPUT VOLTAGE

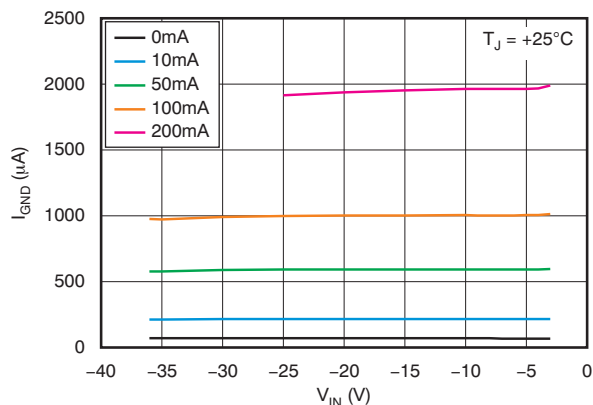


Figure 4.

GROUND CURRENT vs INPUT VOLTAGE

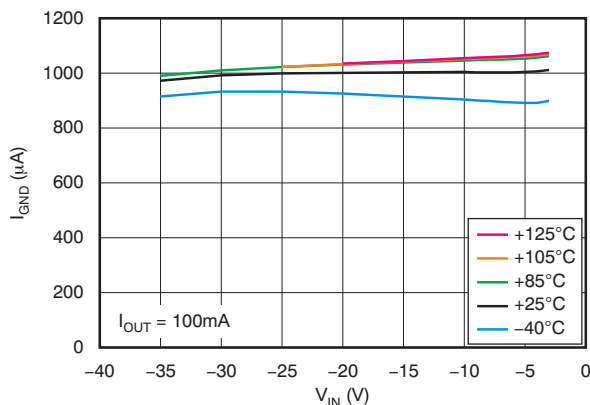


Figure 5.

GROUND CURRENT vs OUTPUT CURRENT

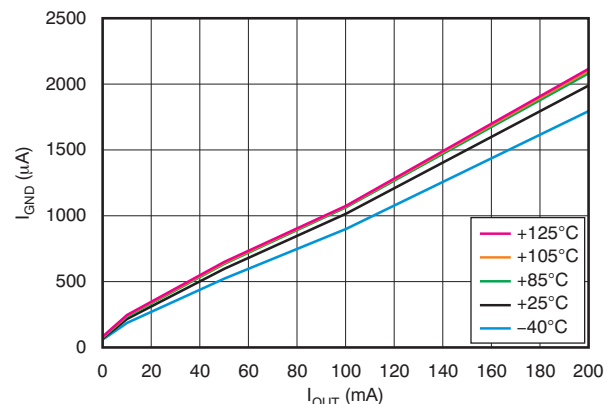


Figure 6.

ENABLE CURRENT vs ENABLE VOLTAGE

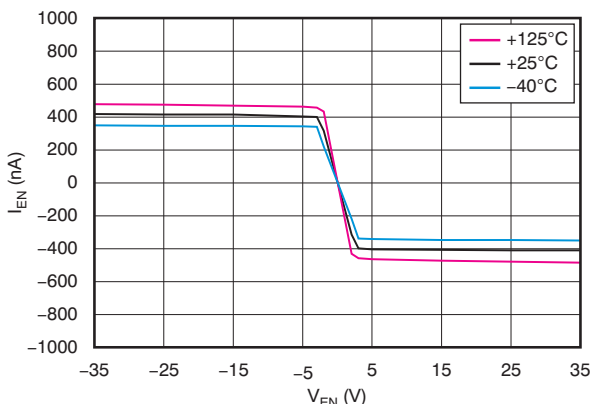


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At $T_J = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $|V_{IN}| = |V_{OUT(NOM)}| + 1.0\text{V}$ or $|V_{IN}| = 3.0\text{V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 1\text{mA}$, $C_{IN} = 2.2\mu\text{F}$, $C_{OUT} = 2.2\mu\text{F}$, $C_{NR/SS} = 0\text{nF}$, and the FB pin tied to OUT, unless otherwise noted.

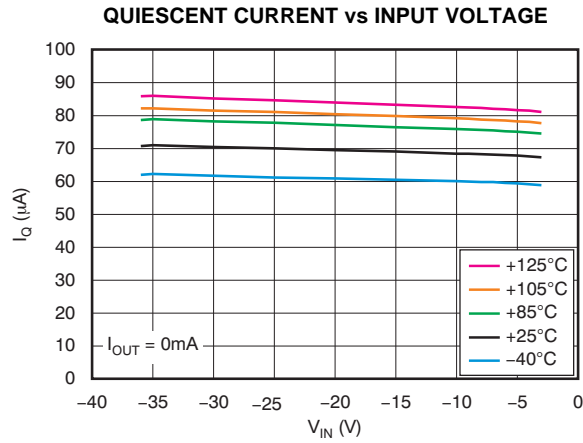


Figure 8.

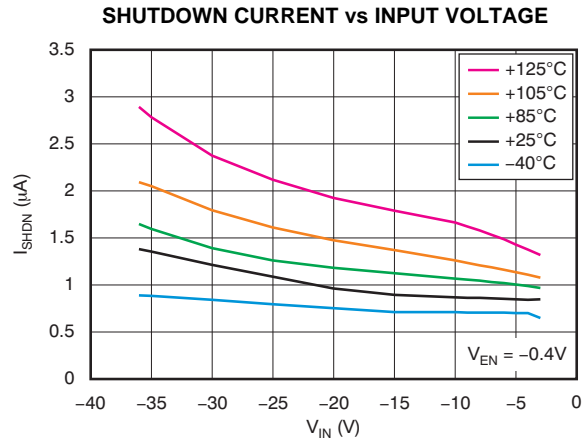


Figure 9.

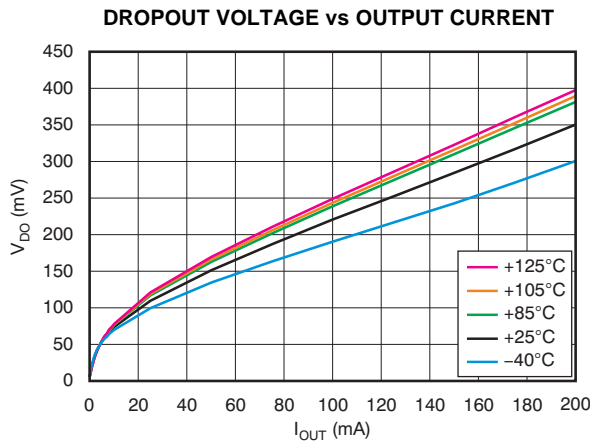


Figure 10.

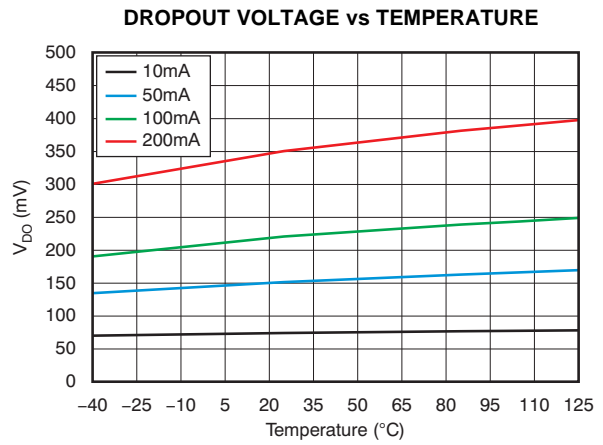


Figure 11.

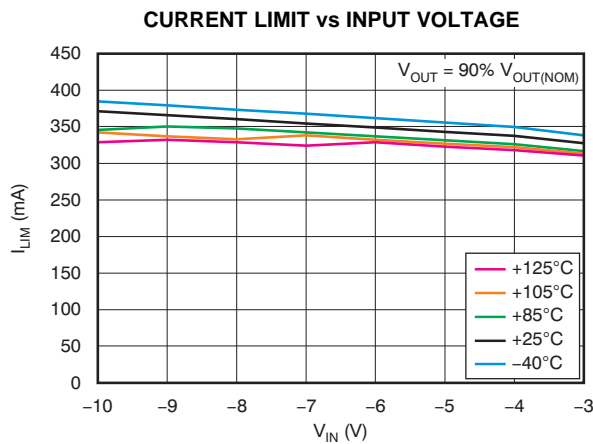


Figure 12.

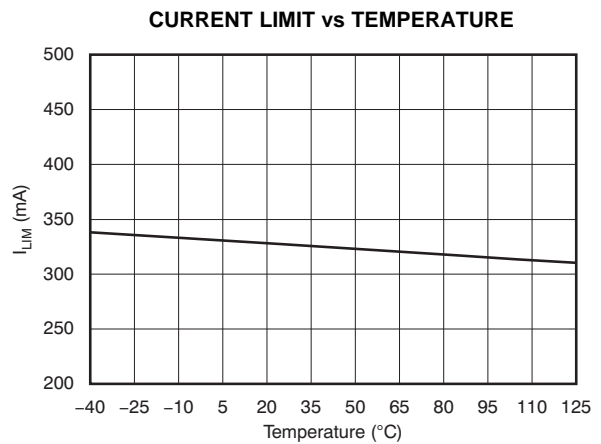


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At $T_J = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $|V_{IN}| = |V_{OUT(NOM)}| + 1.0\text{V}$ or $|V_{IN}| = 3.0\text{V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 1\text{mA}$, $C_{IN} = 2.2\mu\text{F}$, $C_{OUT} = 2.2\mu\text{F}$, $C_{NR/SS} = 0\text{nF}$, and the FB pin tied to OUT, unless otherwise noted.

ENABLE THRESHOLD VOLTAGE vs TEMPERATURE

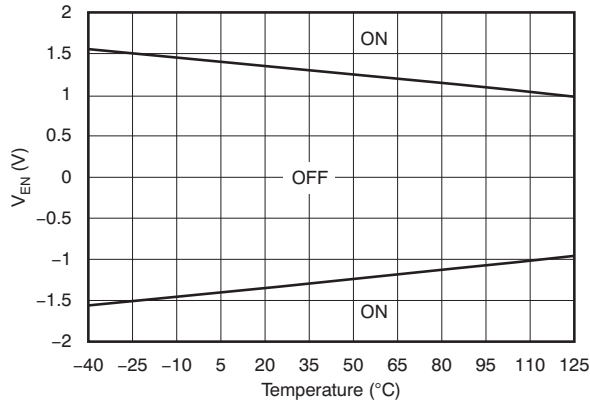


Figure 14.

POWER-SUPPLY REJECTION RATIO vs C_OUT

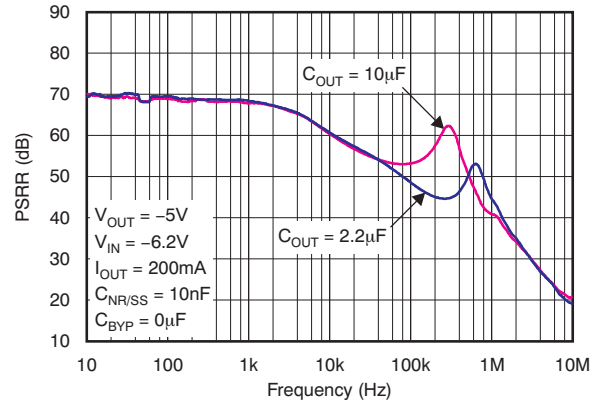


Figure 15.

LINE REGULATION

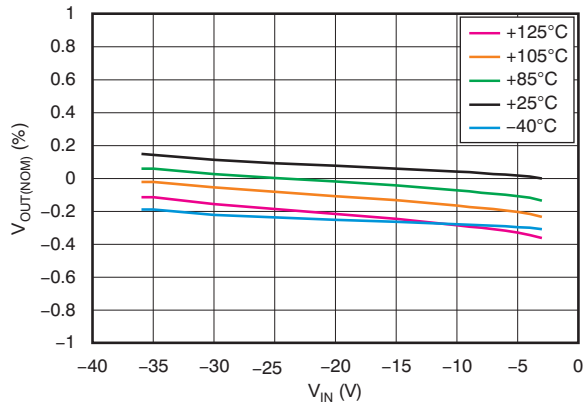


Figure 16.

POWER-SUPPLY REJECTION RATIO vs C_NR/SS

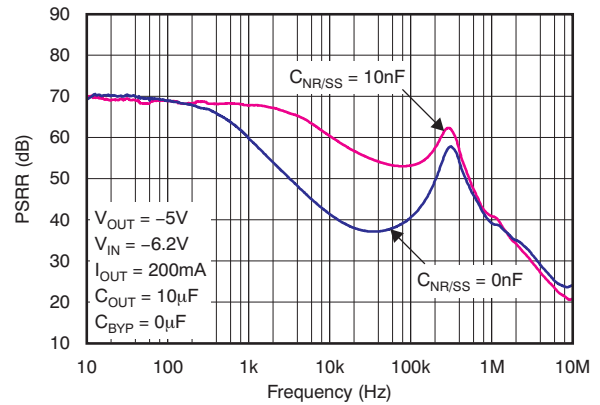


Figure 17.

LOAD REGULATION

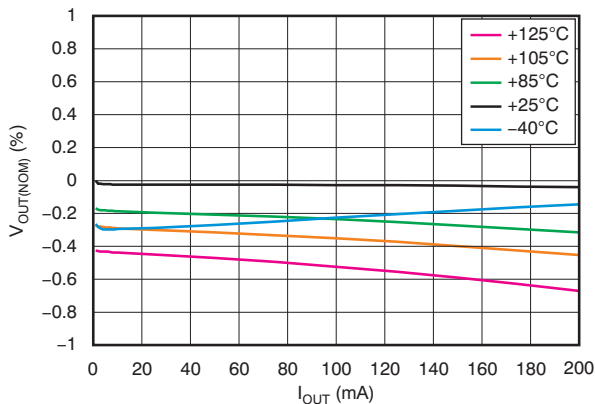


Figure 18.

POWER-SUPPLY REJECTION RATIO vs C_BYP

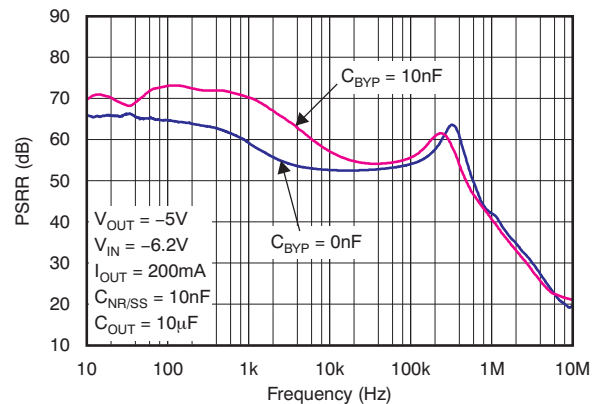
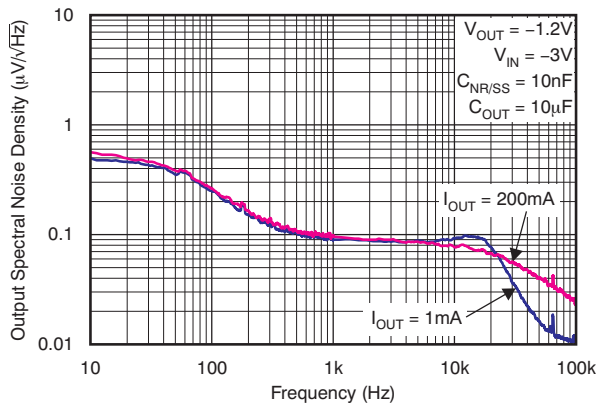


Figure 19.

TYPICAL CHARACTERISTICS (continued)

At $T_J = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $|V_{IN}| = |V_{OUT(NOM)}| + 1.0\text{V}$ or $|V_{IN}| = 3.0\text{V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 1\text{mA}$, $C_{IN} = 2.2\mu\text{F}$, $C_{OUT} = 2.2\mu\text{F}$, $C_{NR/SS} = 0\text{nF}$, and the FB pin tied to OUT, unless otherwise noted.

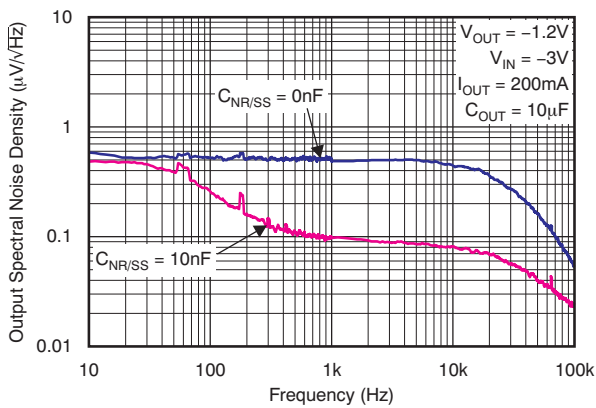
OUTPUT SPECTRAL NOISE DENSITY vs OUTPUT CURRENT



I_{OUT}	RMS NOISE	
	10Hz to 100kHz	100Hz to 100kHz
1mA	15.13	14.73
200mA	17.13	16.71

Figure 20.

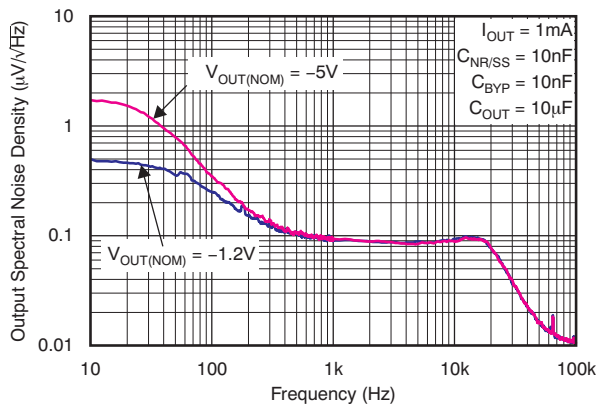
OUTPUT SPECTRAL NOISE DENSITY vs $C_{NR/SS}$



$C_{NR/SS}$	RMS NOISE	
	10Hz to 100kHz	100Hz to 100kHz
0nF	80.00	79.83
10nF	17.29	16.81

Figure 21.

OUTPUT SPECTRAL NOISE DENSITY vs $V_{OUT(NOM)}$



$V_{OUT(NOM)}$	RMS NOISE	
	10Hz to 100kHz	100Hz to 100kHz
-5V	17.50	15.04
-1.2V	15.13	14.73

Figure 22.

TYPICAL CHARACTERISTICS (continued)

At $T_J = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $|V_{IN}| = |V_{OUT(NOM)}| + 1.0\text{V}$ or $|V_{IN}| = 3.0\text{V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 1\text{mA}$, $C_{IN} = 2.2\mu\text{F}$, $C_{OUT} = 2.2\mu\text{F}$, $C_{NR/SS} = 0\text{nF}$, and the FB pin tied to OUT, unless otherwise noted.

CAPACITOR-PROGRAMMABLE SOFT START

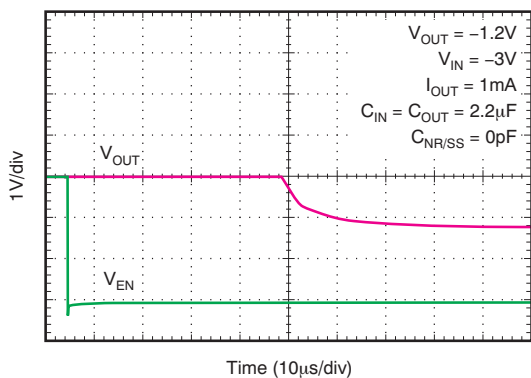


Figure 23.

CAPACITOR-PROGRAMMABLE SOFT START

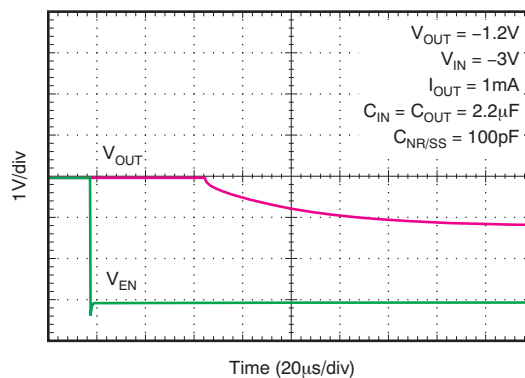


Figure 24.

CAPACITOR-PROGRAMMABLE SOFT START

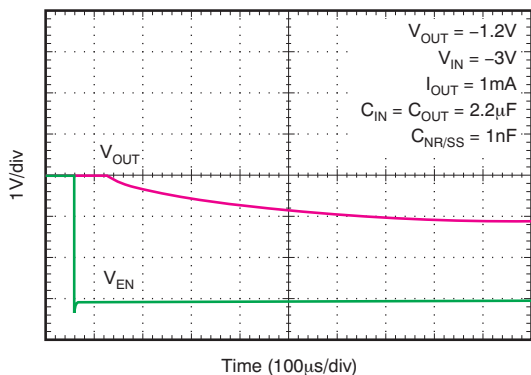


Figure 25.

CAPACITOR-PROGRAMMABLE SOFT START

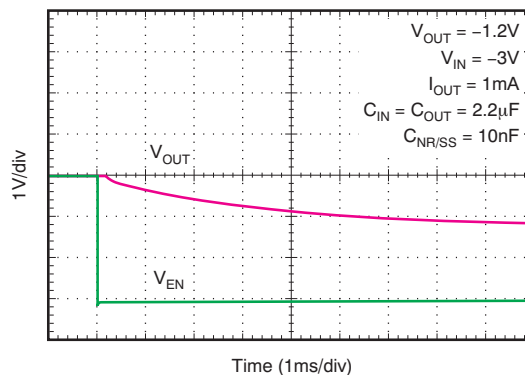


Figure 26.

LINE TRANSIENT RESPONSE

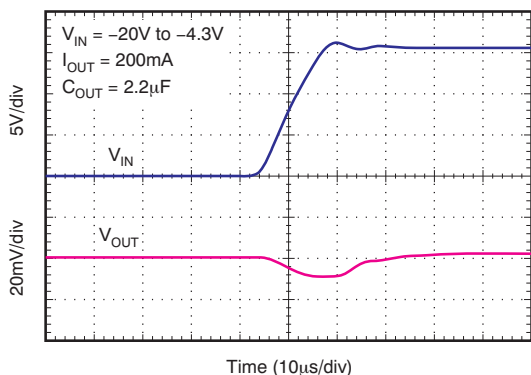


Figure 27.

LINE TRANSIENT RESPONSE

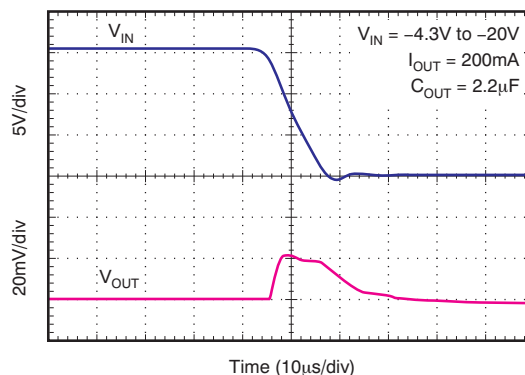


Figure 28.

TYPICAL CHARACTERISTICS (continued)

At $T_J = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $|V_{IN}| = |V_{OUT(NOM)}| + 1.0\text{V}$ or $|V_{IN}| = 3.0\text{V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 1\text{mA}$, $C_{IN} = 2.2\mu\text{F}$, $C_{OUT} = 2.2\mu\text{F}$, $C_{NR/SS} = 0\text{nF}$, and the FB pin tied to OUT, unless otherwise noted.

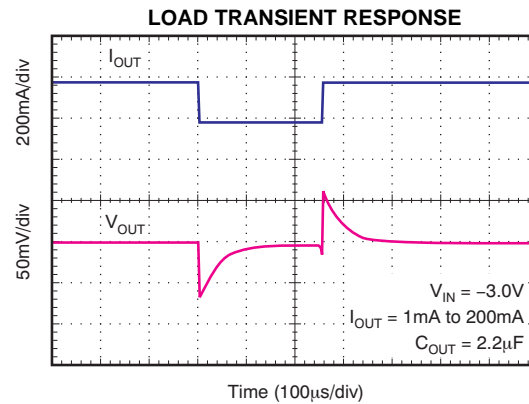


Figure 29.

THEORY OF OPERATION

GENERAL DESCRIPTION

The TPS7A3001 belongs to a family of new generation linear regulators that use an innovative bipolar process to achieve ultralow-noise and very high PSRR levels at a wide input voltage range. These features, combined with a high thermal performance MSOP-8 with PowerPAD package make this device ideal for high-performance analog applications.

ADJUSTABLE OPERATION

The TPS7A3001 has an output voltage range of -1.174 to -35 V. The nominal output voltage of the device is set by two external resistors, as shown in [Figure 30](#).

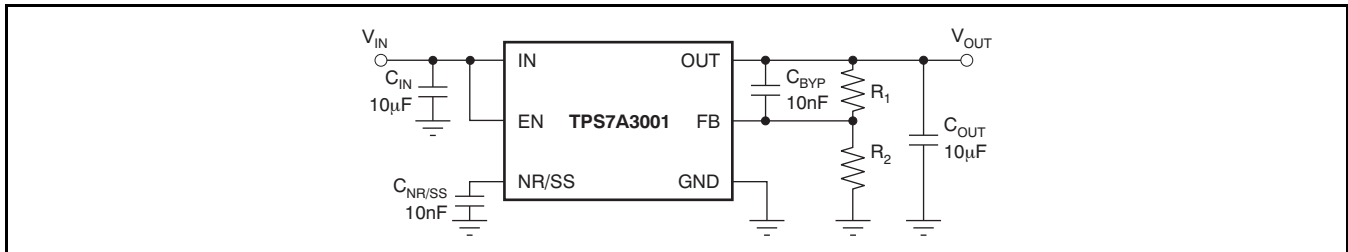


Figure 30. Adjustable Operation for Maximum AC Performance

R_1 and R_2 can be calculated for any output voltage range using the formula shown in [Equation 1](#). To ensure stability under no load conditions, this resistive network must provide a current equal to or greater than $5\mu\text{A}$.

$$R_1 = R_2 \left(\frac{V_{\text{OUT}}}{V_{\text{REF}}} - 1 \right), \quad \text{where } \frac{V_{\text{OUT}}}{R_1 + R_2} \geq 5\mu\text{A} \quad (1)$$

If greater voltage accuracy is required, take into account the output voltage offset contributions because of the feedback pin current and use 0.1% tolerance resistors.

ENABLE PIN OPERATION

The TPS7A3001 provides a dual polarity enable pin (EN) that turns on the regulator when $|V_{\text{EN}}| > 2.0\text{V}$, whether the voltage is positive or negative, as shown in [Figure 31](#).

This functionality allows for different system power management topologies:

- Connecting the EN pin directly to a negative voltage, such as V_{IN} , or
- Connecting the EN pin directly to a positive voltage, such as the output of digital logic circuitry.

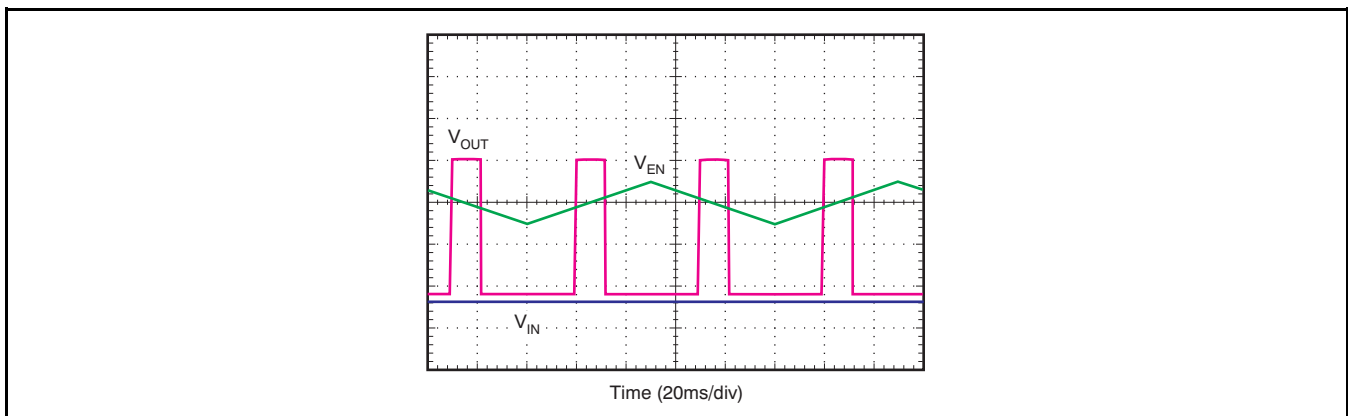


Figure 31. Enable Pin Positive/Negative Threshold

CAPACITOR RECOMMENDATIONS

Low ESR capacitors should be used for the input, output, noise reduction, and bypass capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved over-temperature performance, while ceramic X5R capacitors are the most cost-effective and are available in higher values.

Note that high ESR capacitors may degrade PSRR.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

This negative, high-voltage linear regulator achieves stability with a minimum input and output capacitance of 2.2 μ F; however, it is highly recommended to use a 10 μ F capacitor to maximize ac performance.

NOISE REDUCTION AND BYPASS CAPACITOR REQUIREMENTS

Although noise reduction and bypass capacitors ($C_{NR/SS}$ and C_{BYP} , respectively) are not needed to achieve stability, it is highly recommended to use 0.01 μ F capacitors to minimize noise and maximize ac performance.

MAXIMUM AC PERFORMANCE

In order to maximize noise and PSRR performance, it is recommended to include 10 μ F or higher input and output capacitors, and 0.01 μ F noise reduction and bypass capacitors, as shown in [Figure 30](#). The solution shown delivers minimum noise levels of 15.1 μ V_{RMS} and power-supply rejection levels above 55dB from 10Hz to 700kHz; see [Figure 19](#) and [Figure 20](#).

OUTPUT NOISE

The TPS7A3001 provides low output noise when a noise reduction capacitor ($C_{NR/SS}$) is used.

The noise reduction capacitor serves as a filter for the internal reference. By using a 0.01 μ F noise reduction capacitor, the output noise is reduced by almost 80% (from 80 μ V_{RMS} to 17 μ V_{RMS}); see [Figure 21](#).

TPS7A3001 low output voltage noise makes it an ideal solution for powering noise-sensitive circuitry.

POWER-SUPPLY REJECTION

The 0.01 μ F noise reduction capacitor greatly improves TPS7A3001 power-supply rejection, achieving up to 20dB of additional power-supply rejection for frequencies between 110Hz and 400kHz.

Additionally, ac performance can be maximized by adding a 0.01 μ F bypass capacitor (C_{BYP}) from the FB pin to the OUT pin. This capacitor greatly improves power-supply rejection at lower frequencies, for the band from 10Hz to 200kHz; see [Figure 19](#).

The very high power-supply rejection of the TPS7A3001 makes it a good choice for powering high-performance analog circuitry, such as operational amplifiers, ADCs, DACs, and audio amplifiers.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

APPLICATION INFORMATION

POWER FOR PRECISION ANALOG

One of the primary TPS7A3001 applications is to provide ultralow noise voltage rails to high-performance analog circuitry in order to maximize system accuracy and precision.

In conjunction with its positive counterpart, the TPS7A49xx family of positive high-voltage linear regulators, this negative high voltage linear regulator provides ultralow noise positive and negative voltage rails to high-performance analog circuitry, such as operational amplifiers, ADCs, DACs, and audio amplifiers.

Because of the ultralow noise levels at high voltages, analog circuitry with high-voltage input supplies can be used. This characteristic allows for high-performance analog solutions to optimize the voltage range, maximizing system accuracy.

POST DC/DC CONVERTER FILTERING

Most of the time, the voltage rails available in a system do not match the voltage specifications demanded by one or more of its circuits; these rails must be stepped up or down, depending on specific voltage requirements.

DC/DC converters are the preferred solution to step up or down a voltage rail when current consumption is not negligible. They offer high efficiency with minimum heat generation, but they have one primary disadvantage: they introduce a high-frequency component, and the associated harmonics, on top of the dc output signal.

This high-frequency component, if not filtered properly, degrades analog circuitry performance, reducing overall system accuracy and precision.

The TPS7A3001 offers a wide-bandwidth, very-high power-supply rejection ratio. This specification makes it ideal for post dc/dc converter filtering, as shown in Figure 32. It is highly recommended to use the maximum performance schematic shown in Figure 30. Also, verify that the fundamental frequency (and its first harmonic, if possible) is within the bandwidth of the regulator PSRR, shown in Figure 19.

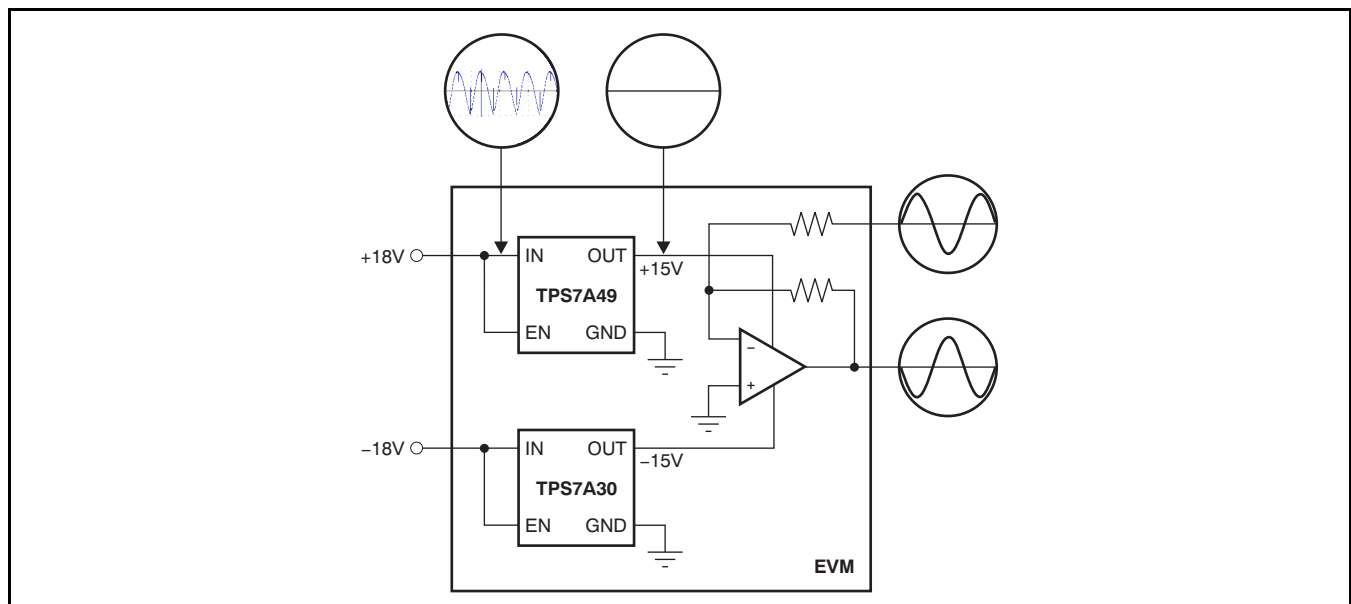


Figure 32. Post DC/DC Converter Regulation to High-Performance Analog Circuitry

AUDIO APPLICATIONS

Audio applications are extremely sensitive to any distortion and noise in the audio band from 20Hz to 20kHz. This stringent requirement demands clean voltage rails to power critical high-performance audio systems.

The very-high power-supply rejection ratio (> 55dB) and low noise at the audio band of the TPS7A3001 maximize performance for audio applications; see Figure 19.

LAYOUT

PACKAGE MOUNTING

Solder pad footprint recommendations for the TPS7A3001 are available at the end of this product datasheet and at www.ti.com.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and equivalent series resistance (ESR) must be minimized in order to maximize performance and ensure stability. Every capacitor (C_{IN} , C_{OUT} , $C_{NR/SS}$, C_{BYP}) must be placed as close as possible to the device and on the same side of the printed circuit board (PCB) as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance denoted in this product datasheet, use the same layout pattern used for TPS7A30 evaluation board, available at www.ti.com.

THERMAL PROTECTION

Thermal protection disables the output when the junction temperature rises to approximately +170°C, allowing the device to cool. When the junction temperature cools to approximately +150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to a maximum of +125°C. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A3001 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A3001 into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element, as shown in [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) I_{OUT} \quad (2)$$

SUGGESTED LAYOUT AND SCHEMATIC

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with a X5R or X7R dielectric.

The GND pin should be tied directly to the PowerPAD under the IC. The PowerPAD should be connected to any internal PCB ground planes using multiple vias directly under the IC.

It may be possible to obtain acceptable performance with alternate PCB layouts; however, the layout shown in [Figure 33](#) and the schematic shown in [Figure 34](#) have been shown to produce good results and are meant as a guideline.

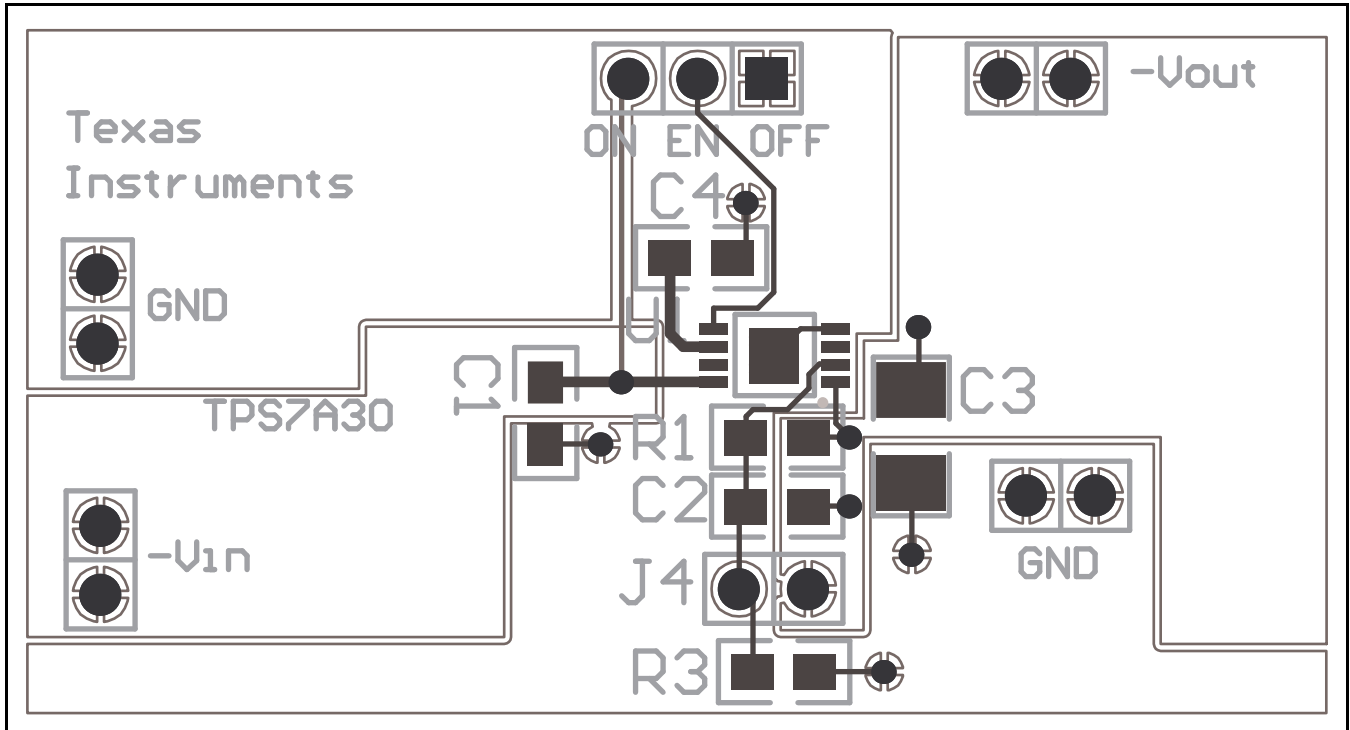


Figure 33. PCB Layout Example

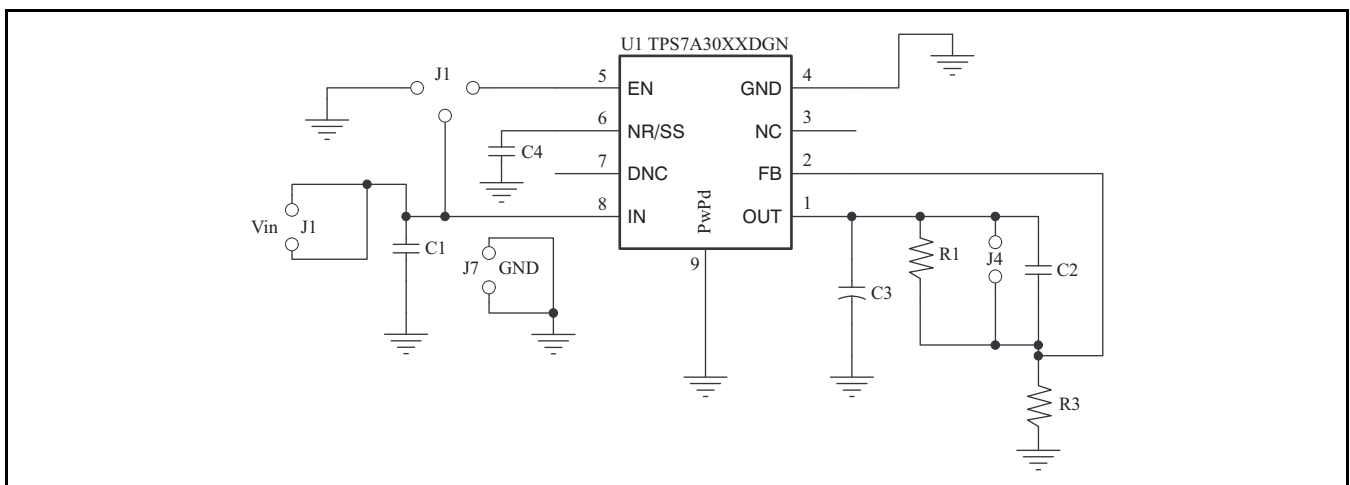


Figure 34. Schematic for PCB Layout Example

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A3001MDGNTEP	ACTIVE	HVSSOP	DGN	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	PXCM	Samples
V62/11619-01XE	ACTIVE	HVSSOP	DGN	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	PXCM	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A3001MDGNTEP	HVSSOP	DGN	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A3001MDGNTEP	HVSSOP	DGN	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

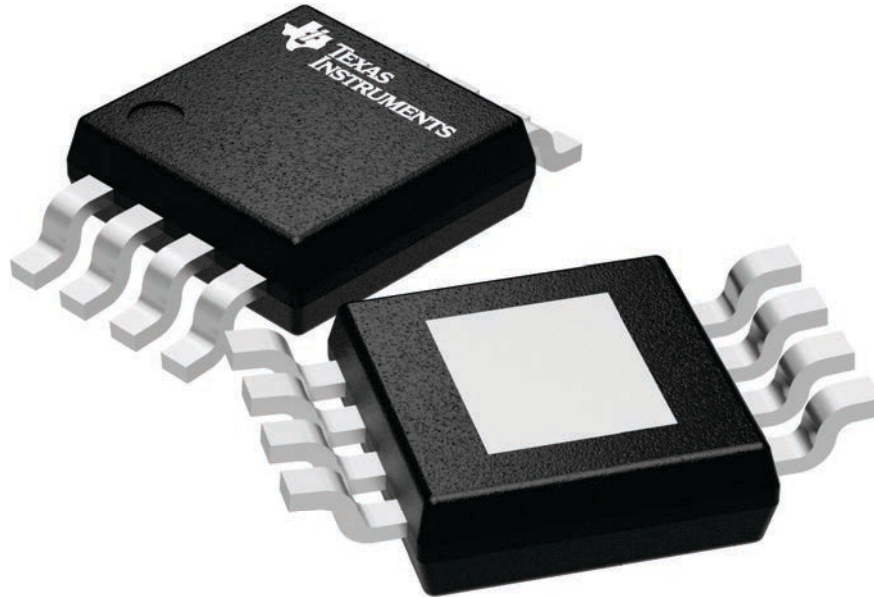
DGN 8

PowerPAD VSSOP - 1.1 mm max height

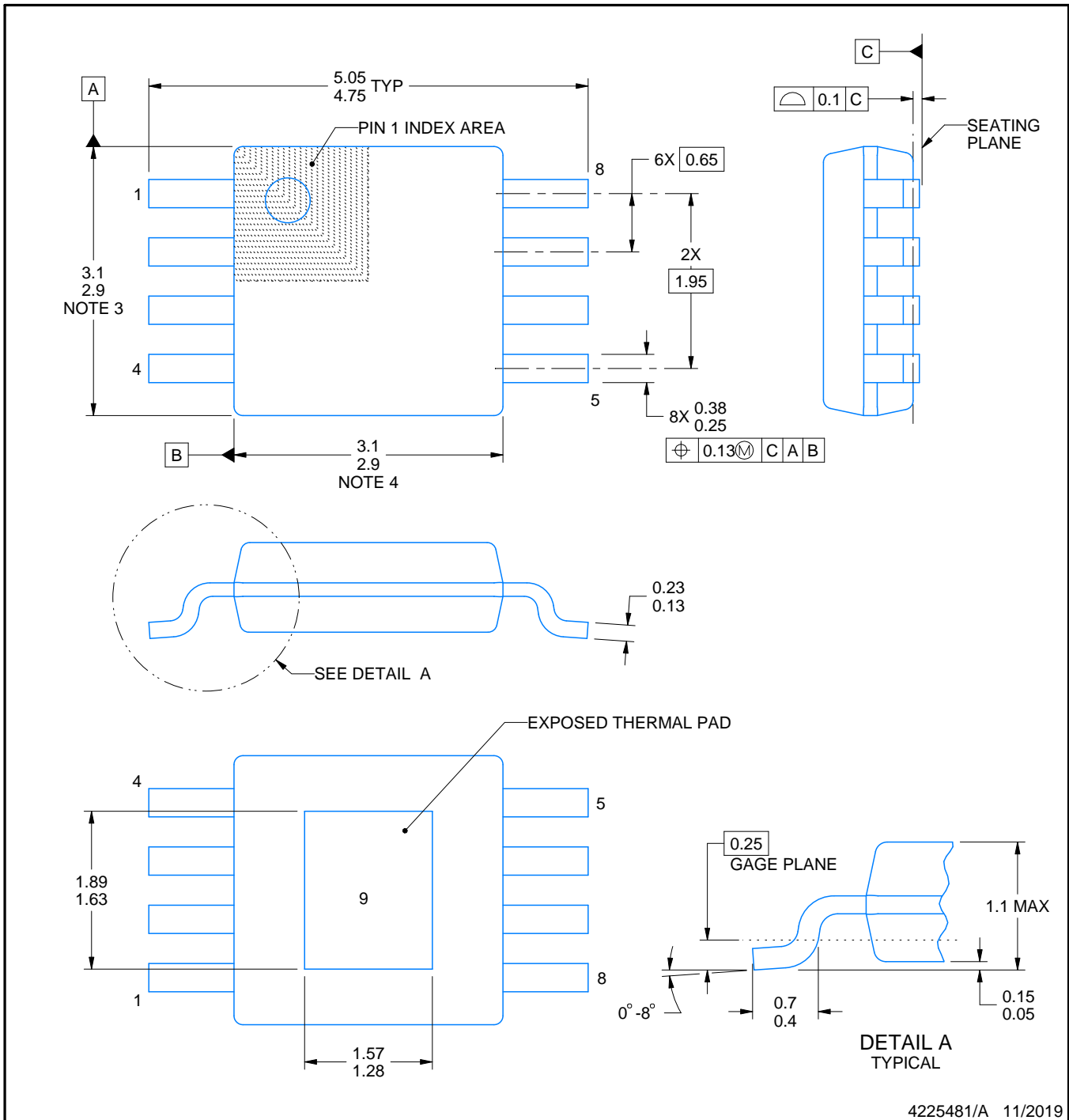
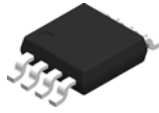
3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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4225481/A 11/2019

PowerPAD is a trademark of Texas Instruments.

NOTES:

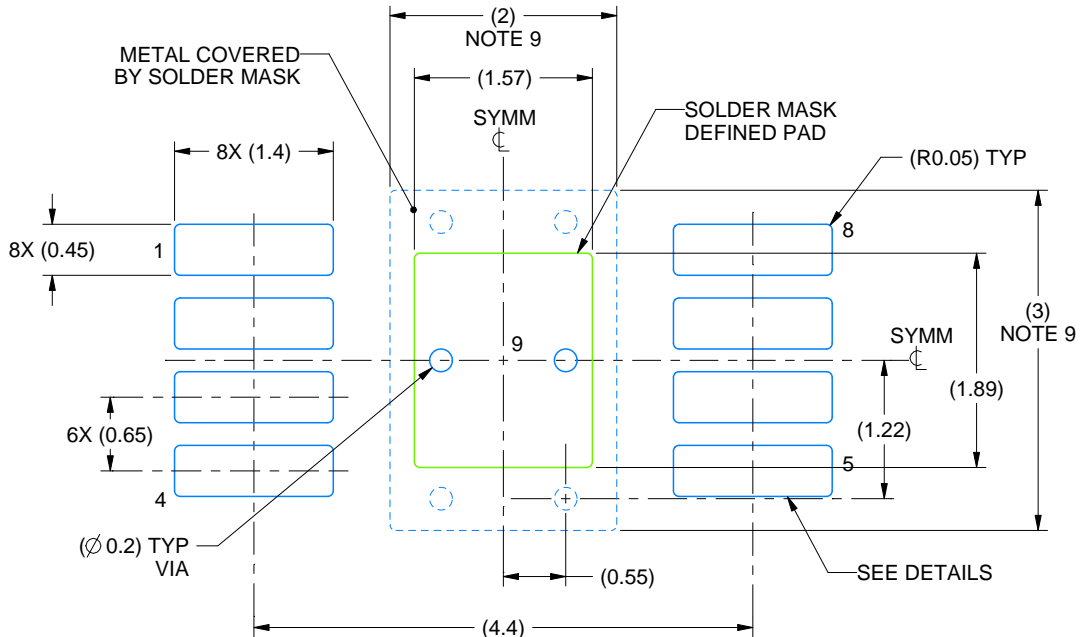
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

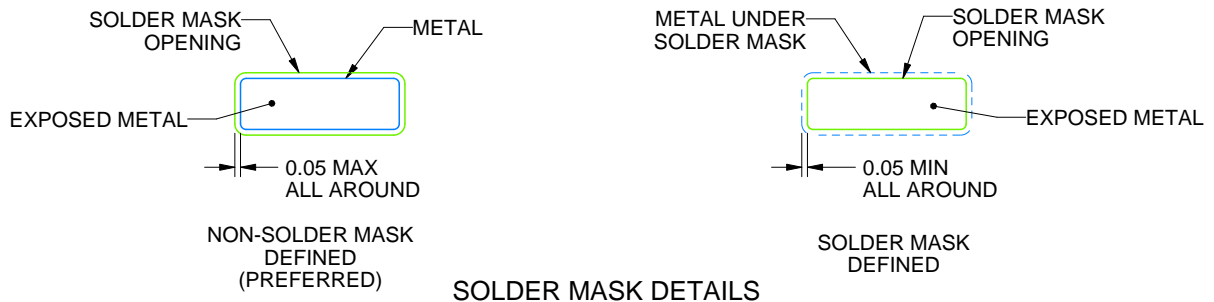
DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



4225481/A 11/2019

NOTES: (continued)

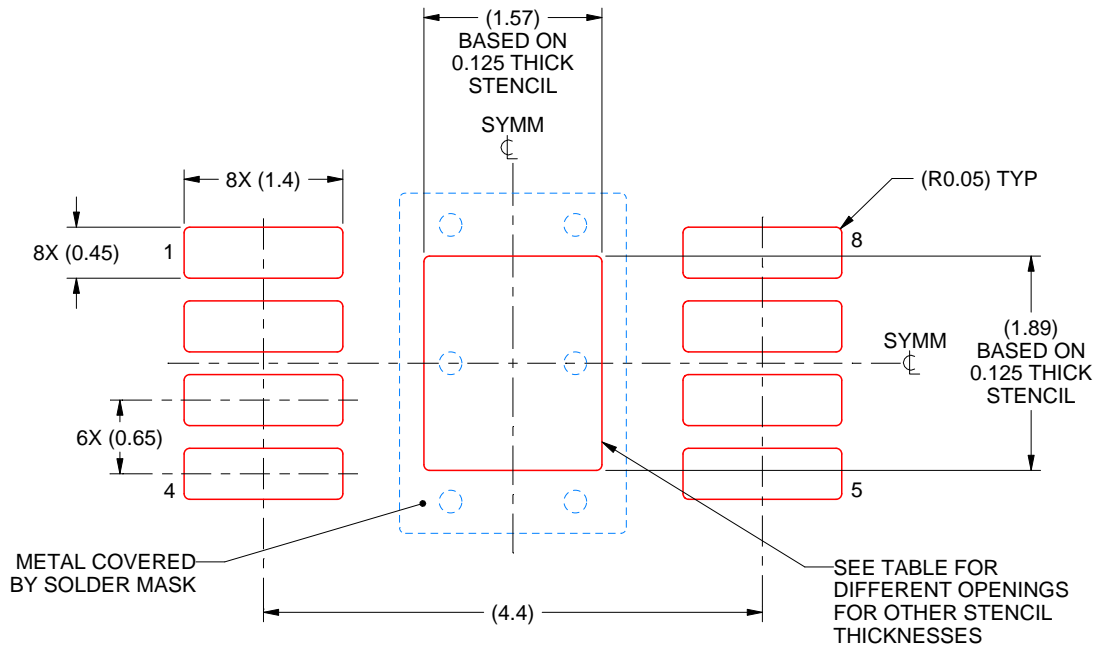
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
 EXPOSED PAD 9:
 100% PRINTED SOLDER COVERAGE BY AREA
 SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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