Application Report

Paralleling LED Driver Channels to Support Higher Currents Using TPS92520-Q1 or TPS92519-Q1

ABSTRACT

As requirements continue to evolve in the automotive LED headlight market, greater flexibility is expected in LED drivers. The TPS92520-Q1 is a flexible dual 1.6-A monolithic synchronous buck with SPI control, while the TPS92519-Q1 is a standalone dual 2.0-A monolithic synchronous buck. This application report provides some general guidelines on how to use the TPS92520-Q1's dual channels to create a single 3.2-A output and how to use the TPS92519-Q1's dual channels to create a single 4-A output, which supports a wider application space with the same device.

Table of Contents

List of Figures

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1 Introduction to Paralleling Current Sources

Both the TPS92520-Q1 and the TPS92519-Q1 are dual, synchronous buck LED drivers that can drive each channel as independent current sources. Connecting the device's channels together allows for the summation of each output current from the channels to a single channel, which means paralleling the drive currents. Paralleling the channels for each device is implemented differently. This application report will cover the different design considerations for the TPS92520-Q1 and the TPS92519-Q1.

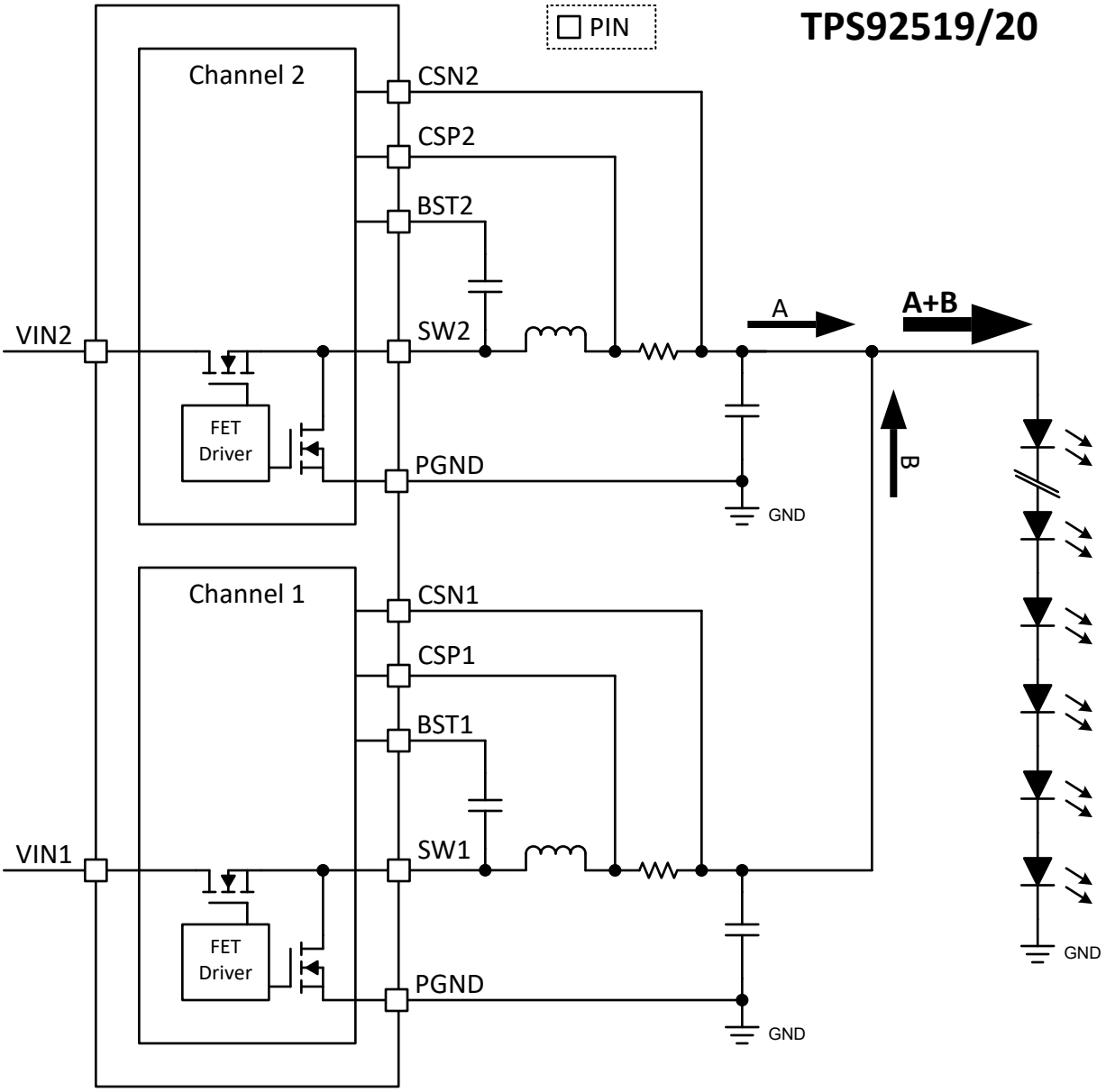

Figure 1-1. Dual Channel LED Driver Connected in Parallel - TPS92519-Q1 and TPS92520-Q1

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1.1 TPS92520-Q1

The TPS92520-Q1 can be programed using SPI, so that each channel is an independent constant current, synchronous buck output. There are a variety of registers that control output current setpoints: switching frequency, PWM control, and modes of operation. There are also registers that give information on the status of the device and other measurements, such as input voltage and output voltage.

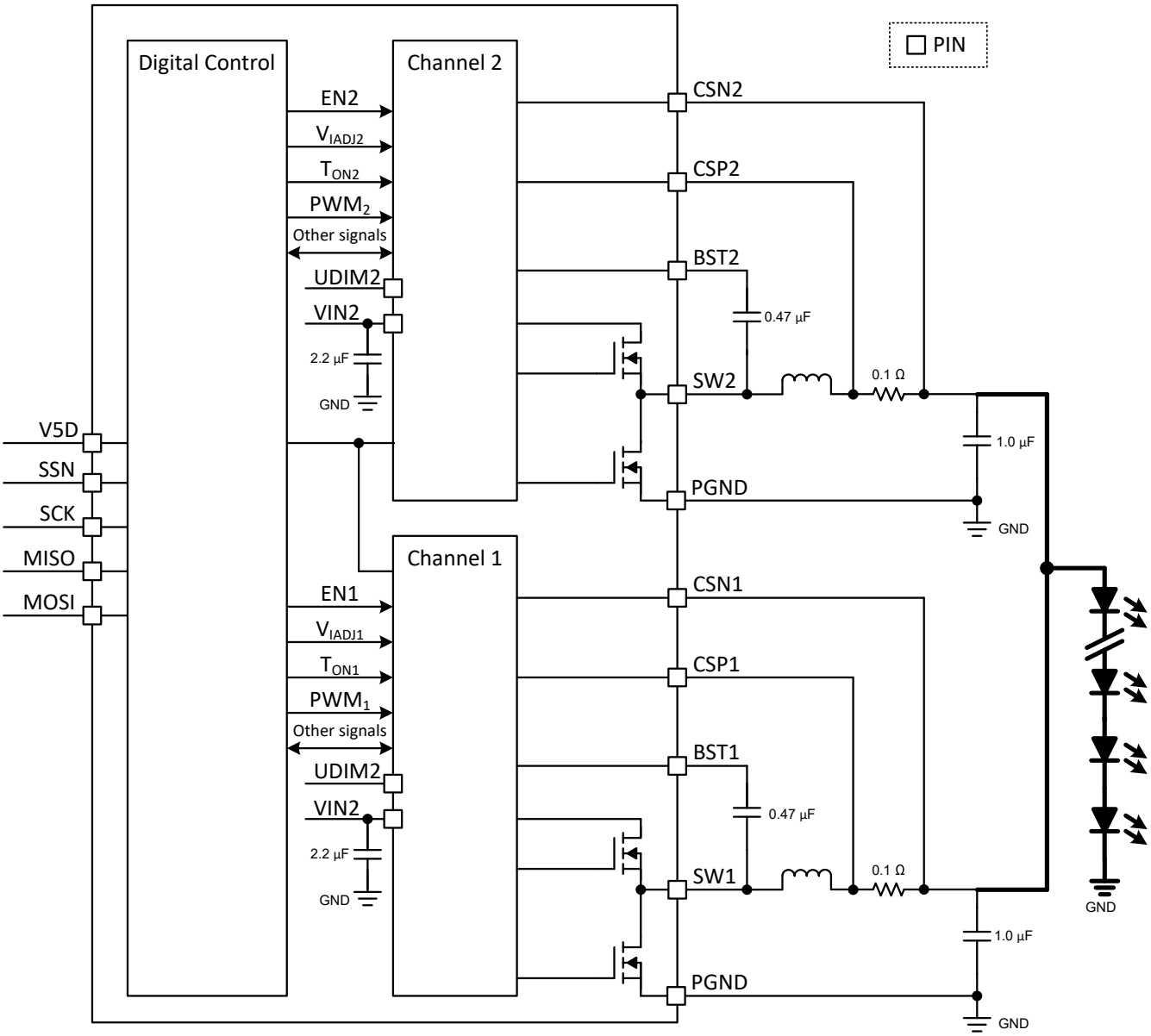

Figure 1-2. High level Connections for TPS92520-Q1 Dual Synchronous Buck LED Driver

The device has a floating gate driver that depends on charging the BST cap by turning on the Low-Side FET (LS-FET), which creates a 5-V supply that is floating on the switch node and drives the High-Side FET (HS-FET). The TPS92520-Q1 turns on the LS-FET for approximately 200 µs during the initial start-up to perform the initial charge of the BST cap and is constantly charged by the switching action of the buck converter during steady state operation. See Figure 1-3 and Figure 1-4.

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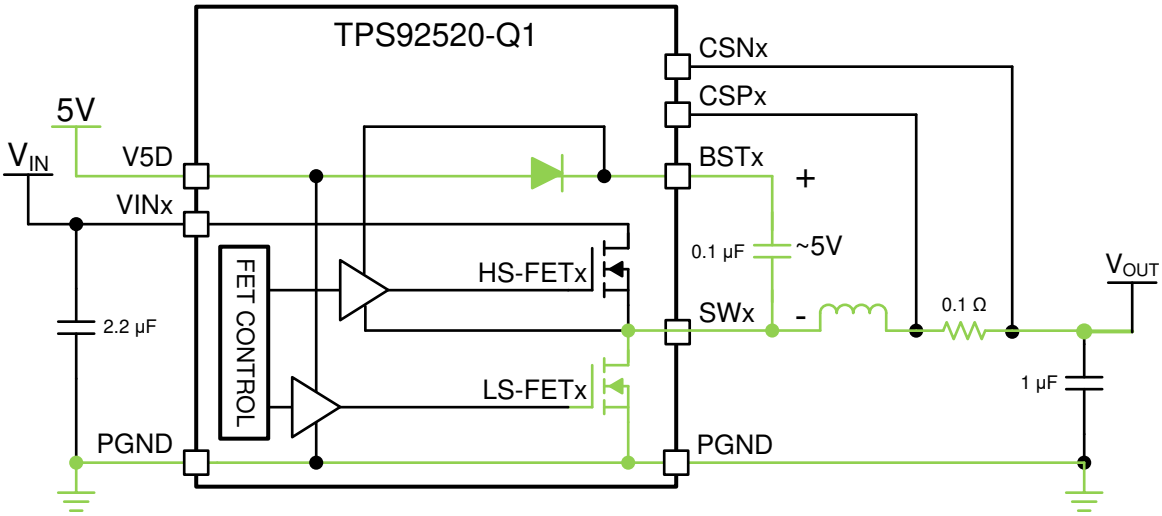

Figure 1-3. BSTx Capacitor Charging at Start-up

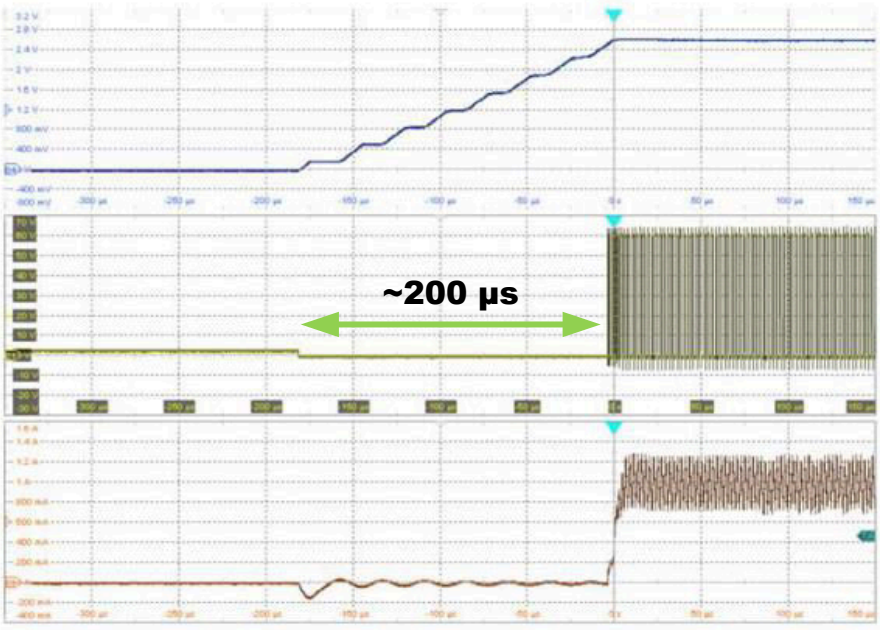

Figure 1-4. Start-up Waveform for a Single Channel

Achieving 3.2 A of output current is as simple as connecting the two output channels together and ensuring that both channels perform their start-up sequence at the same time. See Figure 1-5.

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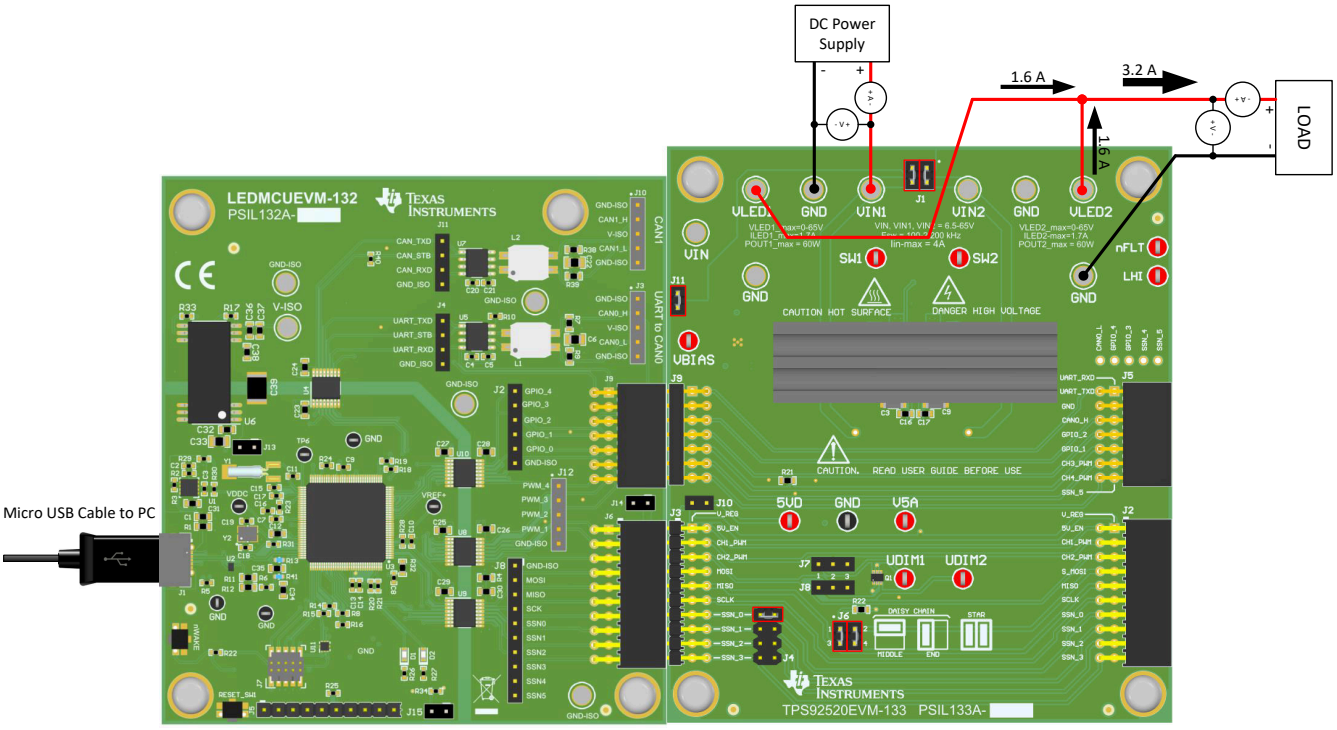

Figure 1-5. Parallel Connection of Outputs Using the TPS92520EVM-133 and LEDMCUEVM-132 Controller

Synchronization of the start-up sequence is achieved by turning on both channels at the same time (CH1EN and CH2EN bits) by performing a single write to the SYSCFG1 register (address 0x00h). If using the internal PWM registers to perform PWM dimming, then the PWM phase bit (PWMPH) must be set to 1 to establish 0 phase shift between both channels. See Figure 1-6.

7	6	5	4	3	2	1	0
FPINRST	PWMPH	LHSW	CMWEN	CH2INTPWM	CH2EN	CH1INTPWM	CH1EN
W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-0b	R/W-0b	R/W-0b
x	1	x	x	x	1	x	1

Figure 1-6. CH1EN, CH2EN, and PWMPH Bits in SYSCFG1 Register (0x00h)

If external PWM dimming is performed using the UDIM pints, then the signals to UDIM1 and UDIM2 pins must be tied together or be precisely controlled so that they are synchronized with very small delays. Figure 1-7 shows external PWM signal from external source and not the LEDMCUEVM-132 board's external PWM signals (PWM-1 and PWM-2). See LEDMCUEVM-132 User's Guide for more details.

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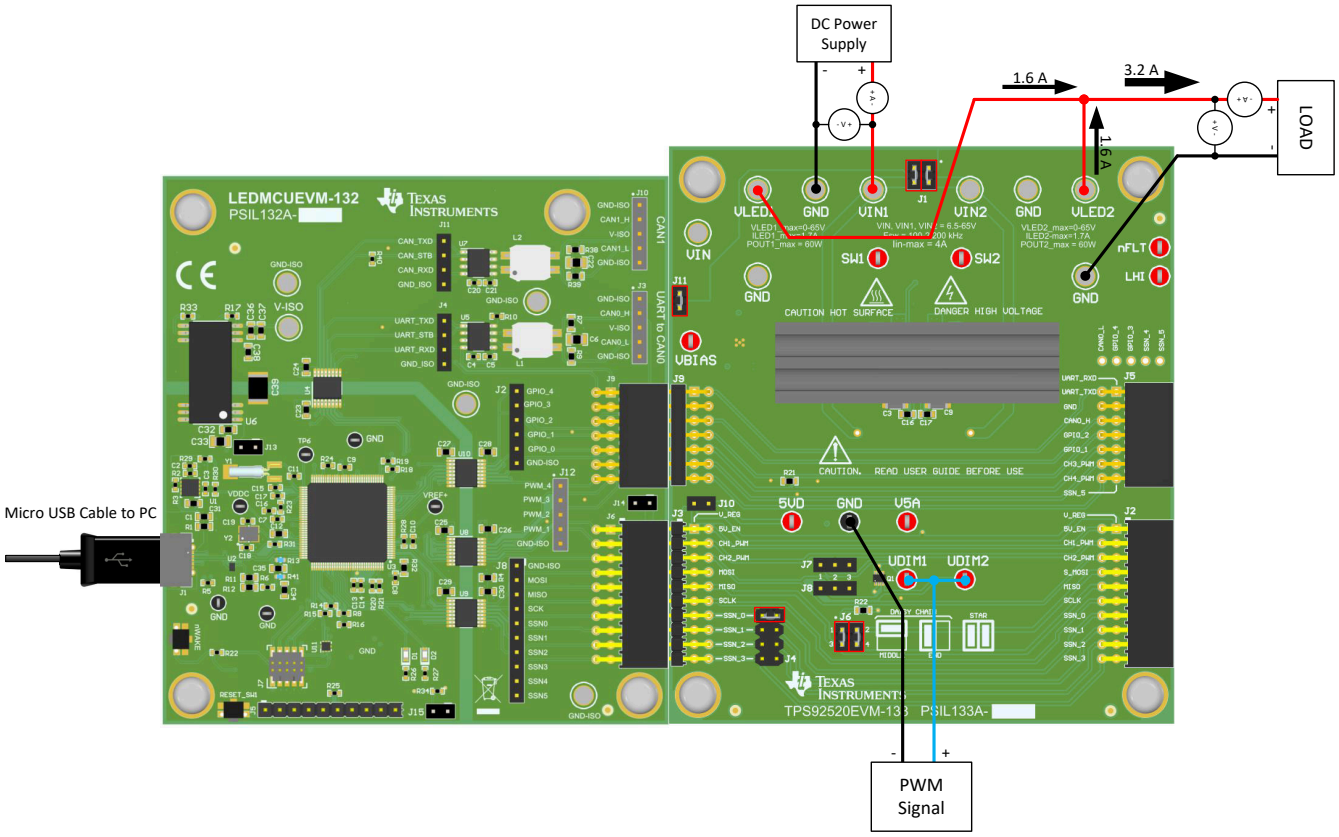

Figure 1-7. PWM Dimming Using External Signals to UDIM1 and UDIM2 Pins

1.2 TPS92520-Q1 Design Considerations

Ideally, both channels must be set up to be symmetric with respect to components and settings. For example, if a 2-A output is needed, then each channel must be set to 1 A and use relatively close output capacitance, BST capacitance, switching frequency, COMP capacitance, and inductance. This action ensures a balanced thermal approach that evenly distributes the power dissipation, and it ensures that mismatches in the circuits are minimal and do not affect the relative start-up sequence.

1.2.1 Example Setup of Parallel Channels Generating 2-A Output Using TPS92520EVM-133 Board and GUI

Connect the LEDMCUEVM-132 to the TPS92520EVM-133, and connect the USB cable from the computer to the LEDMCUEVM-132. See instructions for GUI installation and operation that are in the TPS92520EVM-133 User's Guide and the LEDMCUEVM-133 User's Guide.

Start by selecting the *En 520 No WD* button to disable the watchdog timer (CMWEN bit in SYSCFG1 register). Before turning on the channels, use the GUI to set the channels to the desired set points for IADJ, TON, and so forth. In this example, *Analog Current* is set to 600 decimal, which is approximately 1 A for each channel. Both use the default *On Time* of 7 decimal which is approximately 440 kHz. See Figure 1-8.

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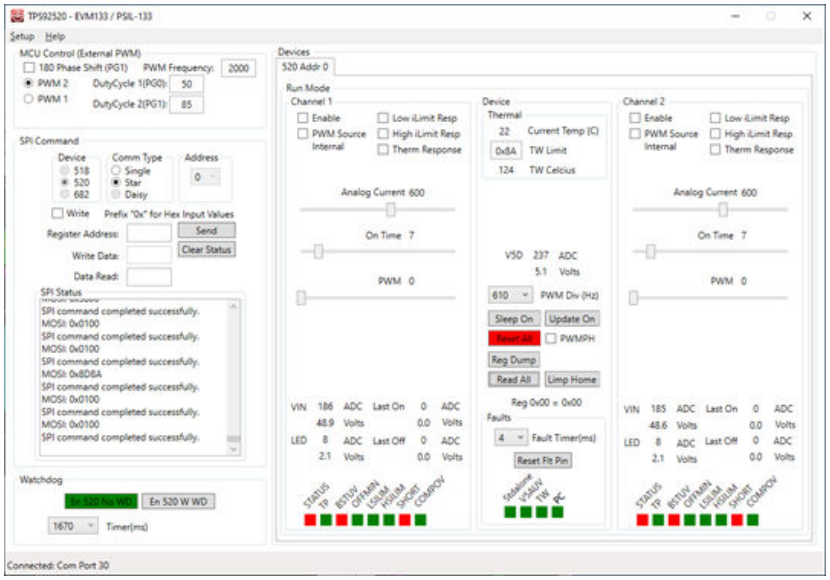

Figure 1-8. GUI After *En 520 No WD* Button is Selected, Which Disabled the Watch Dog Timer

Then, use the SPI command window to do a single write to the SYSCFG1 register (0x00h), such that the CH1EN, CH2EN, and PWMPH bits are high. In this example, we write 0x45h to register address 0x00h (SYSCFG1). See Figure 1-9.

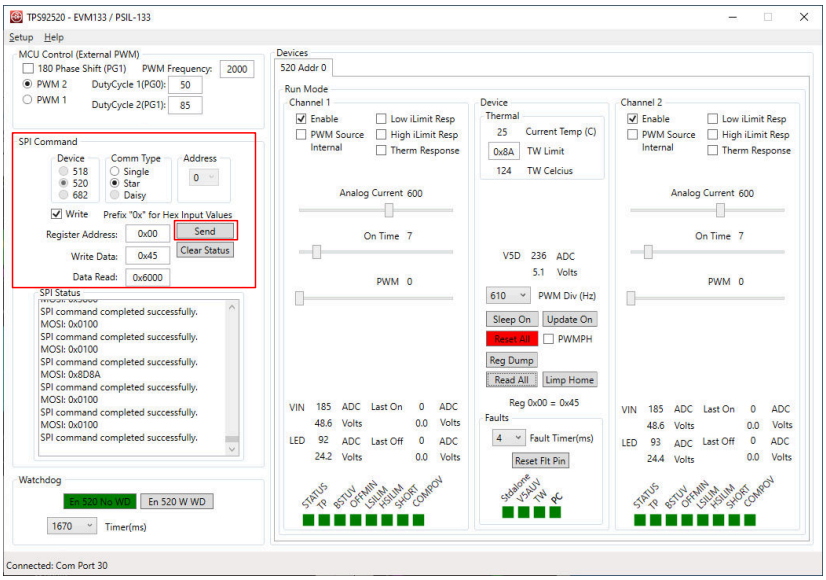

Figure 1-9. Using GUI to Write 0x45h to SYSCFG1 Register at Address 0x00h

Channels 1 and 2 will then synchronously start-up and ramp up to 2 A at the outputs that are tied together. See Figure 1-10.

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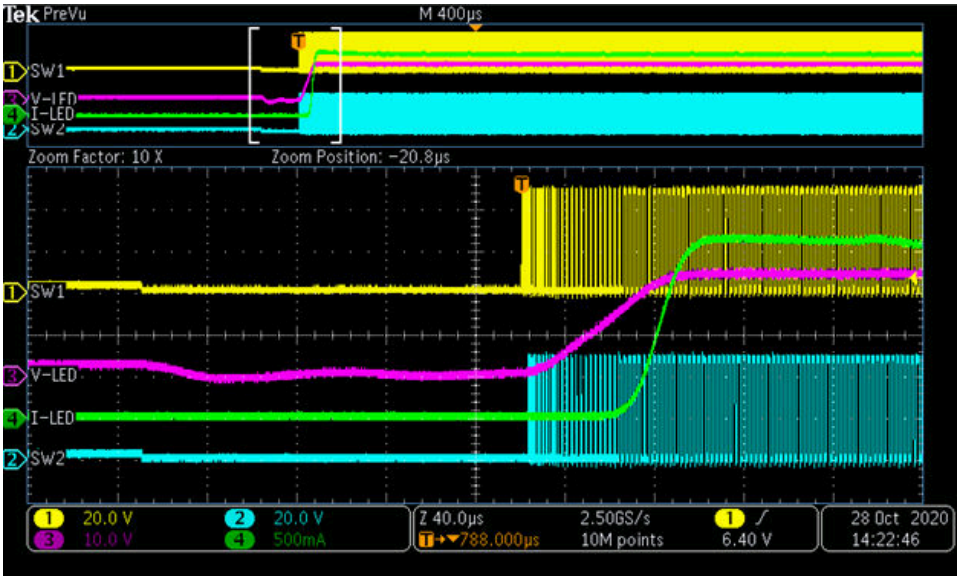

CH1-SW1 voltage, CH2=SW2 voltage, CH3-VLED voltage, and CH4 is ILED current.

Figure 1-10. Start-up of Parallel Connections With Synchronized Start-up

Internal PWM dimming can be used at this point because the PWMPH bit is set high (PWM phase between channels is 0). We can see each channel has different duty cycles setting. See Figure 1-11 for GUI setting and see Figure 1-12 for oscope screen shot of two channels on at different duty cycles.

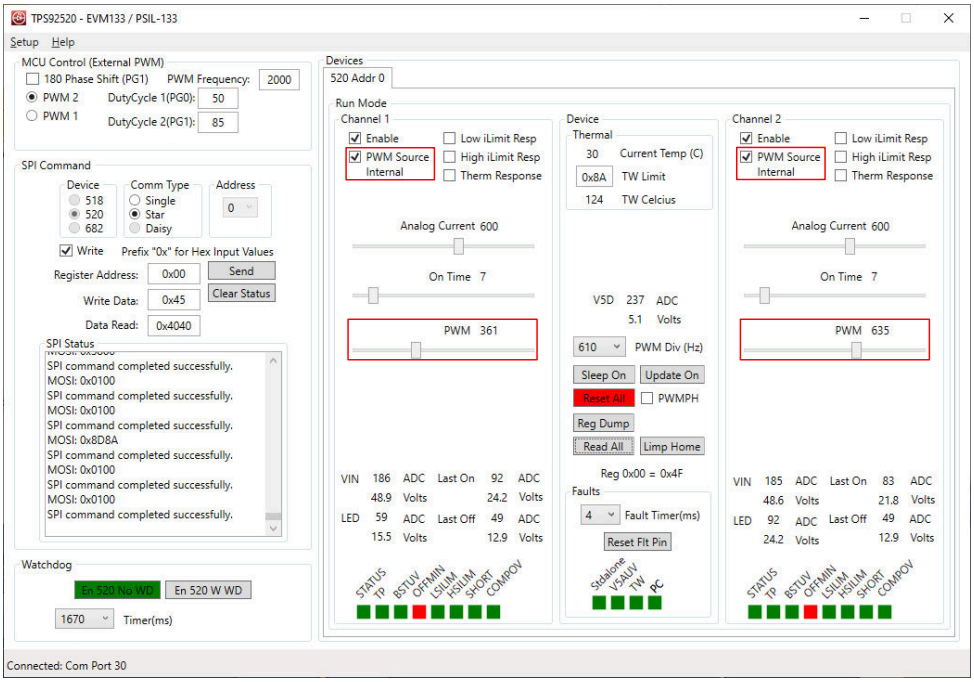

Figure 1-11. Parallel Channels Using Internal PWM Settings Using the GUI

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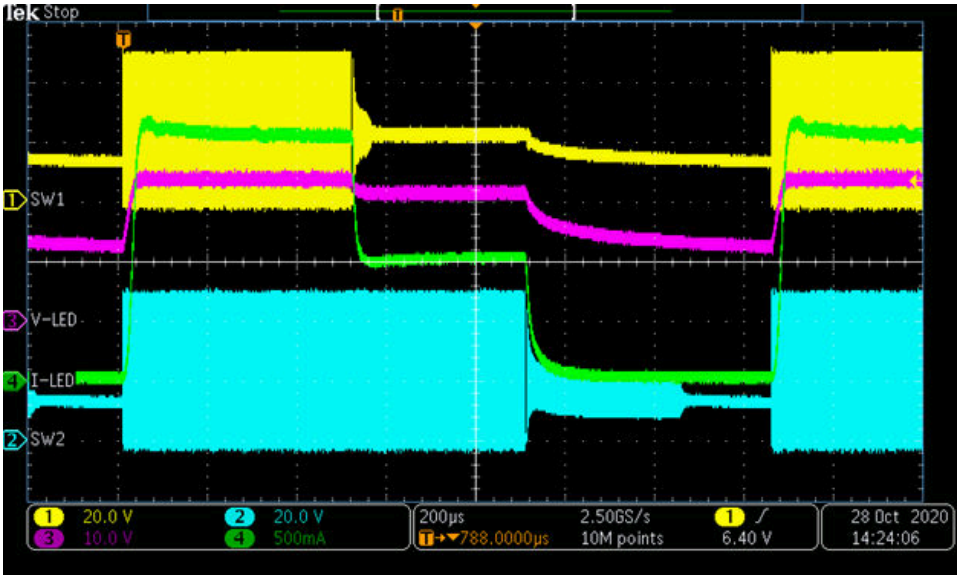

CH1-SW1 voltage, CH2=SW2 voltage, CH3-VLED voltage, and CH4 is ILED current.

Figure 1-12. Parallel Channels With Different PWM Duty Cycles for Each Channel

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1.3 TPS92519-Q1

The TPS92519-Q1 is a standalone, dual buck LED driver that can have each channel's current controlled by IADJ pins and be PWM dimmed by UDIM pins for each respective channel. The 5-V supply for V5D is used by both channels and the EN pin enables or disabled both channels to put the device in sleep mode. The FLT pins indicated if there is a short or open condition for each channel. Each channel controls the output current by applying a voltage from 0.14 to 2.4 V on the IADJx pins. Similarly, the PWM dimming for each channel is adjusted by applying the PWM signal to the UDIMx pins.

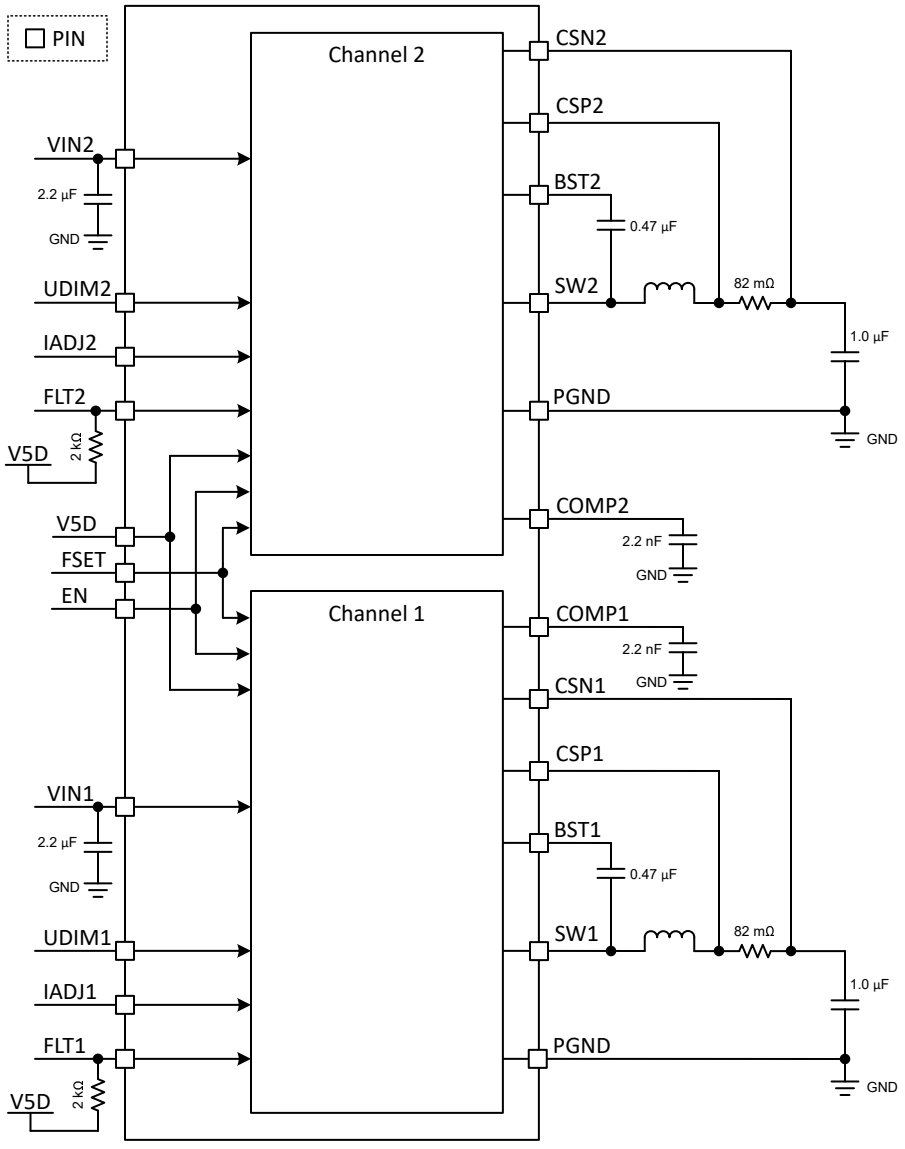

Figure 1-13. High Level Connections for TPS92519-Q1 Dual Synchronous Buck LED Driver

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1.4 TPS92519-Q1 Design Considerations

There are several design considerations that need to be addressed when paralleling the two channels of the TPS92519-Q1.

The COMPx pins for each channel need to be connected together with apposing diodes. See Figure 1-14. The two channels are independent, but in order for both control loops to engage the fault detection properly, then the diodes need to be placed between COMP1 and COMP2. The channels must have the channel currents controlled symmetrically, which means attaching IADJ1 and IADJ2 together. PWM control can be performed independently or synchronized between both channels.

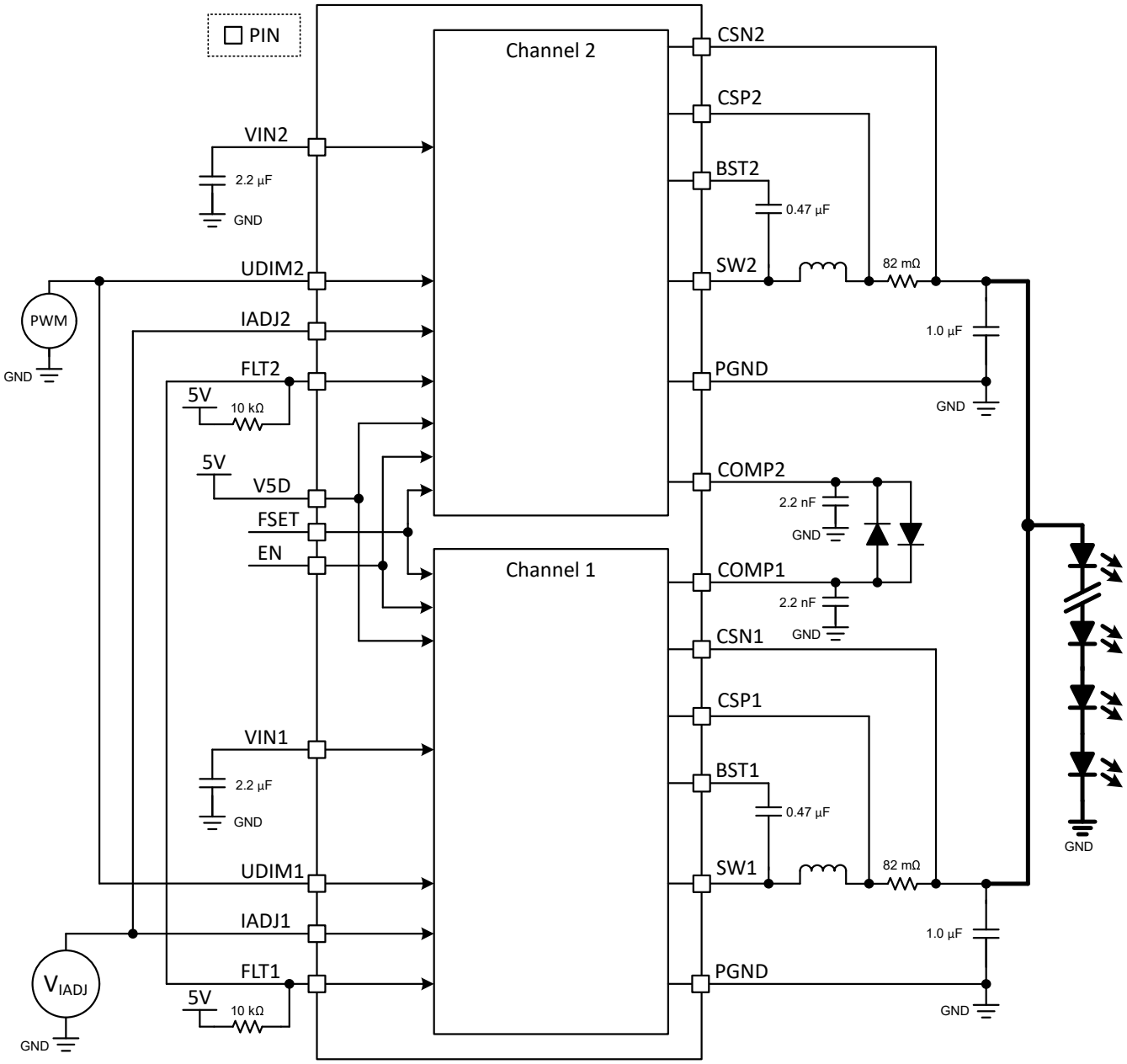

Figure 1-14. TPS92519-Q1 Connections Needed to Support Parallel Channel Operation

The TPS92519EVM-169 needs to be modified to include the two diodes. See Figure 1-15. IADJ1 and IADJ2 are connected together and PWM1 and PWM2 are also connected together (PWMx test points inverter UDIMx signals). LED1+ and LED2+ test points need to be connected together and routed to the load (most cases are LEDs) along with the GND connections. The power supply, which was set to 48 V, is connected to either VIN2 or VIN1 (they are attached together on the TPS92519EVM-169 via R20 and the GND needs to be connected

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between the DC power supply and the EVM). A separate 5-V supply needs to be connected to the 5-V test point and GND test point on the TPS92519EVM-169.

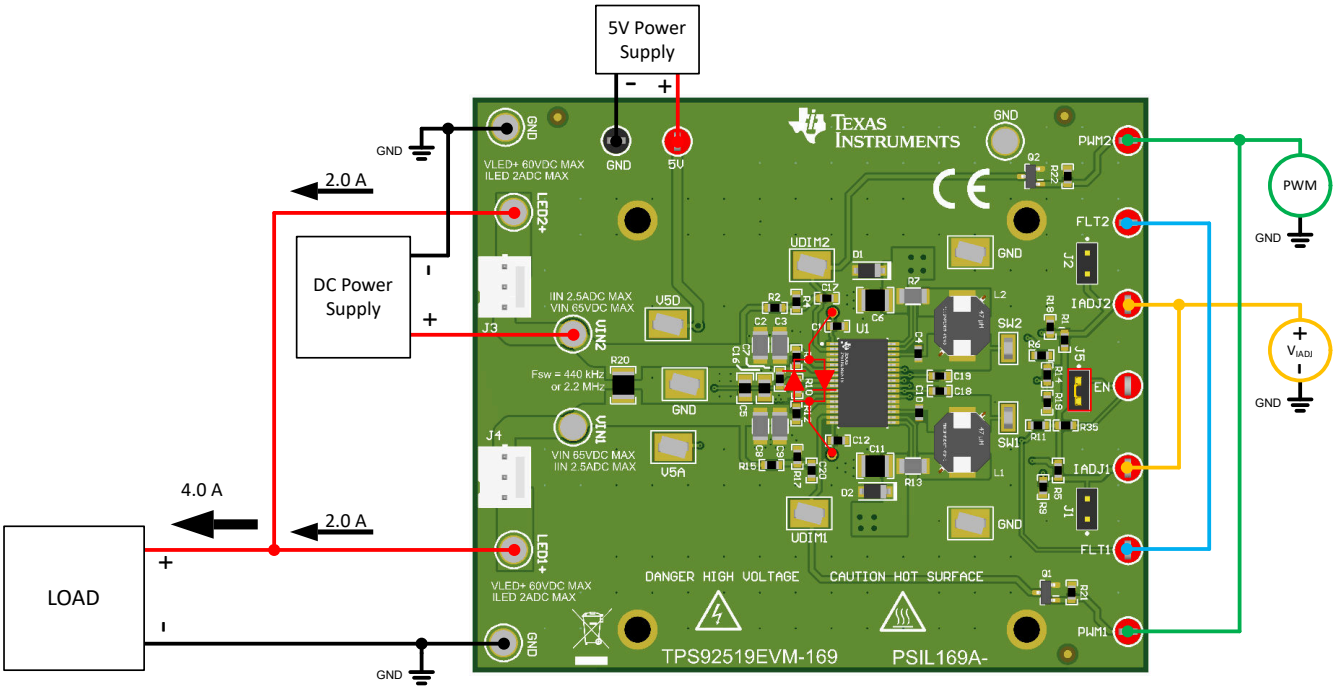

Figure 1-15. Connecting TPS92519EVM-169 for Parallel Operation

Figure 1-16 illustrates the start-up of the parallel channels to achieve 4 A of drive current. V_{IADJ} is set to 2.4 V on both channels of the EVM.

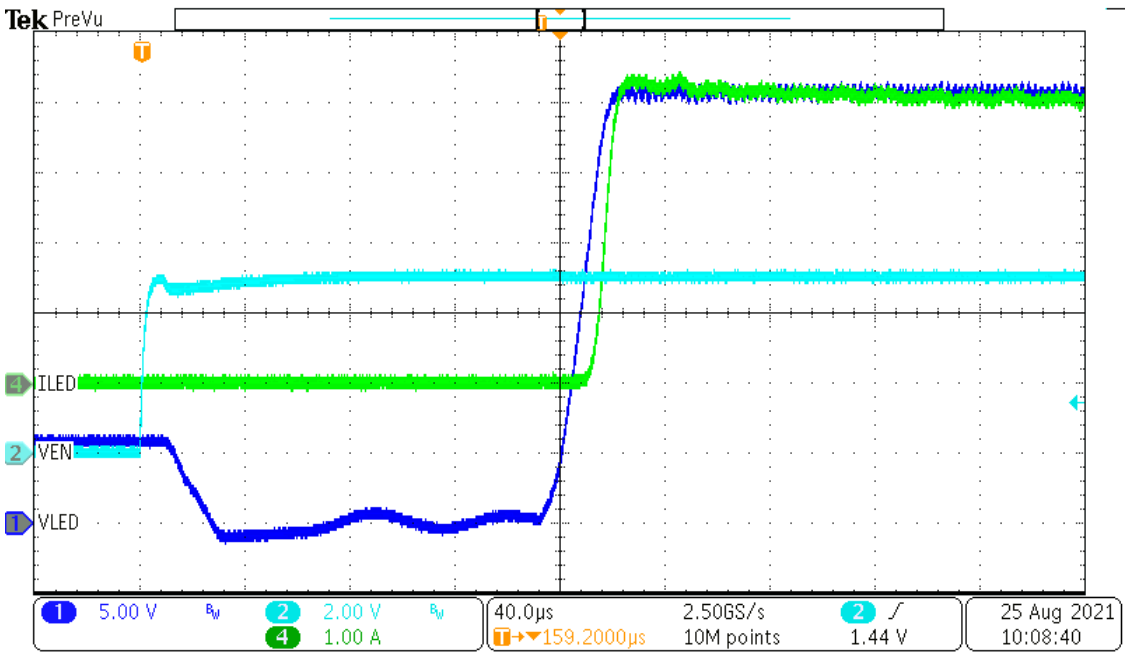

Figure 1-16. Parallel Channels Start-up Using Modified TPS92519EVM-1

Figure 1-17 demonstrates PWM control of the two parallel channels using PWM1 and PWM2 test points on the TPS92519EVM-169.

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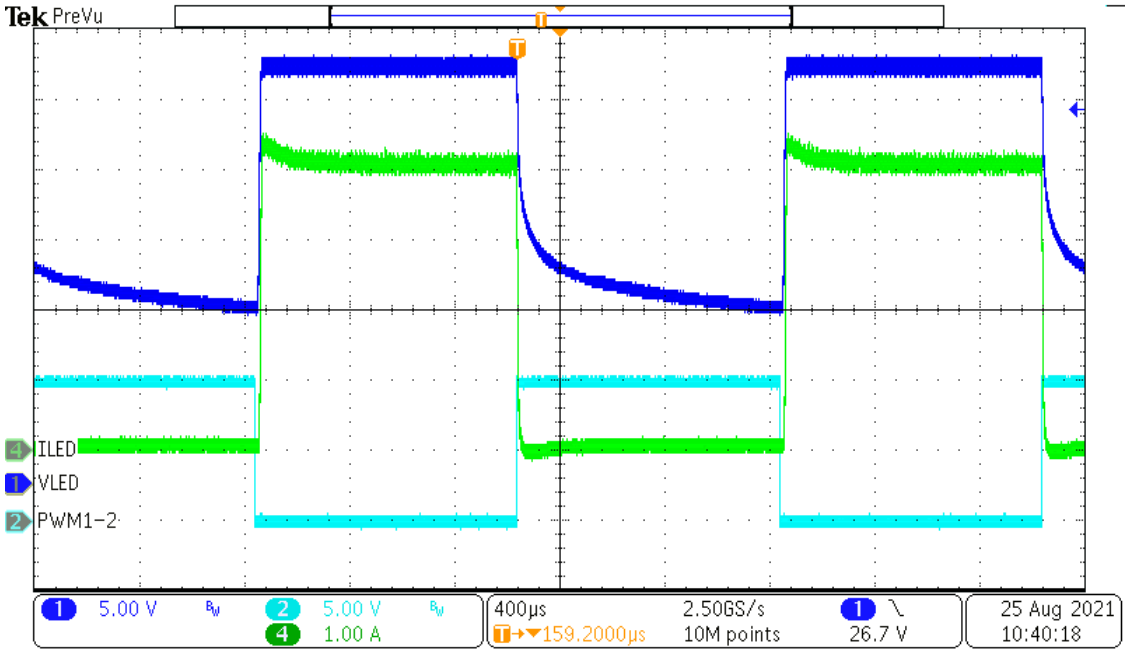

Figure 1-17. Parallel Channels Controlled by PWM Dimming Using Modified TPS92519EVM-169

Figure 1-18 illustrates the FLT flag being triggered when a short is applied to the parallel channels using the modified TPS92519EVM-169. FLT1 and FLT2 test points are tied together on TPS92519EVM-169.

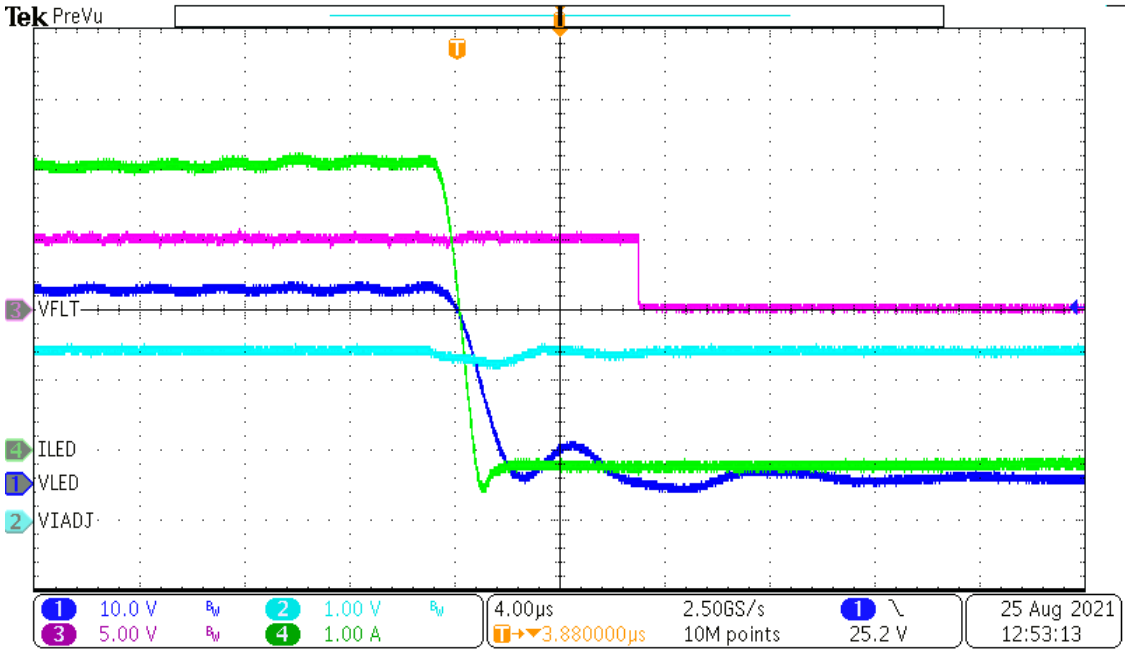

Figure 1-18. Parallel Channels Exposed to Short Circuit Condition Using Modified TPS92519EVM-169

Figure 1-19 illustrates the FLT flag being triggered when modified TPS92519EVM-169 is exposed to an open condition.

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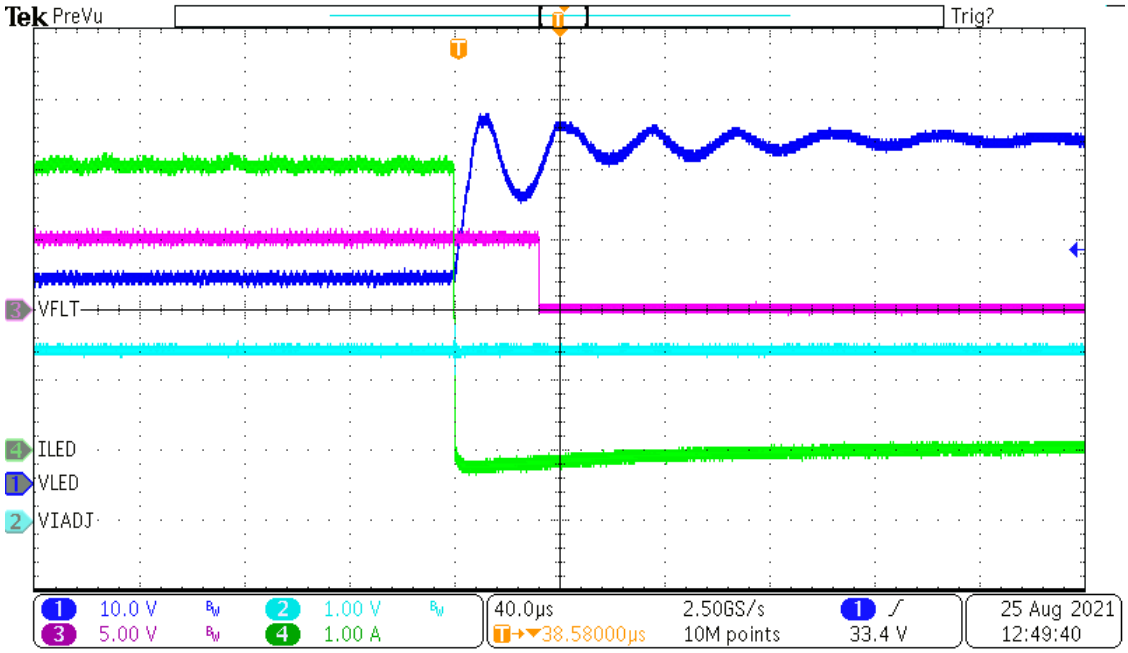

Figure 1-19. Parallel Channels Exposed to Open Circuit Condition Using Modified TPS92519EVM-169

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2 Summary

The TPS92520-Q1 and the TPS92519-Q1 are highly integrated, dual channel solutions which, when connected, controlled, and programmed properly, have the additional ability to parallel their two channels. The TPS92520-Q1 can support up to 3.2 A, and the TPS92519-Q1 can support up to 4 A, assuming all thermal considerations have been addressed.

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