TPSI2140-Q1 1400-V, 50-mA, Automotive Isolated Switch with 2-mA Avalanche Rating

1 Features

- Qualified for automotive applications
  - AEC-Q100 grade 1: –40 to 125°C ambient operating temperature
- Integrated MOSFETs with 2-mA avalanche rating, up to 5 mA with TPSI2140T-Q1 version
  - 1400-V standoff voltage
  - R_{ON} = 130 Ω (T_J = 25°C)
  - T_{ON}, T_{OFF} < 350 µs
- Low primary side supply current
  - 7.5-mA ON state current
  - 6-µA OFF state current
- Robust isolation barrier:
  - > 26 year projected lifetime at 1000-V_{RMS} / 1414-V_{DC} working voltage
  - Isolation rating, V_{ISO}, up to 3750 V_{RMS} / 5300 V_{DC}
  - Peak surge, V_{IOSM}, up to 6000 V
  - ± 100-V/ns typical CMTI
- SOIC (DWQ-11) package with wide pins for improved thermal capability
  - Creepage and clearance ≥ 8 mm (primary-secondary)
  - Creepage and clearance ≥ 6 mm (across switch terminals)
- Safety-related certifications
  - (Planned) DIN VDE V 0884-11:2017-01
  - (Planned) UL 1577 component recognition program

2 Applications

- Solid state relay
- Hybrid, electric, and power train systems
- Battery Management Systems (BMS)
- Solar energy
- Onboard charger
- Electric vehicle chargers (EV)

3 Description

The TPSI2140-Q1 is an isolated solid state relay designed for high voltage automotive and industrial applications. The TPSI2140-Q1 uses TI's high reliability capacitive isolation technology in combination with internal back-to-back MOSFETs to form a completely integrated solution requiring no secondary side power supply.

The entire primary side of the device requires only 7.5 mA of input current, enabling the user to drive both the VDD and EN pins from a single microcontroller GPIO and eliminating the need for an external low side switch used in photo relay solutions. The user can also choose to connect the VDD pin to a system supply between 5 V–20 V and drive the EN pin from a GPIO. The EN pin is fail-safe preventing any possibility of back powering the VDD supply.

The secondary side consists of back-to-back MOSFETs with a standoff voltage of ±1.4 kV from S1 to S2. The TPSI2140-Q1 MOSFET's avalanche robustness and thermally conscious package design allow it to survive system level High Potential (HiPot) screening and DC fast charger surge currents of up to 2 mA without requiring any external components. The TPSI2140T-Q1 version of the device is equipped with TI's Thermal Avalanche Protection (TAP) feature allowing it to support avalanche currents up to 5 mA.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPSI2140-Q1	SOIC 11-pin (DWQ)	10.3 mm × 7.5 mm
TPSI2140T-Q1	SOIC 11-pin (DWQ)	10.3 mm × 7.5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

TPSI2140-Q1 Simplified Application Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2022	*	Initial Release

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5 Pin Configuration and Functions

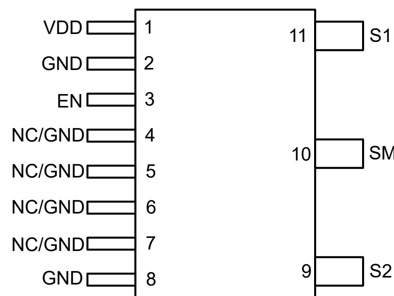

Figure 5-1. TPSI2140 DWQ Production Package 11-Pin SOIC-WB Top View

Table 5-1. Pin Functions

PIN NO.	PIN NAME	I/O(1)	DESCRIPTION
1	VDD	P	Power supply for primary side
2	GND	GND	Ground supply for primary side
3	EN	I	Active high switch enable signal
4	NC/GND	NC/GND	Internally connected, connect externally to ground or leave floating
5	NC/GND	NC/GND	Internally connected, connect externally to ground or leave floating
6	NC/GND	NC/GND	Internally connected, connect externally to ground or leave floating
7	NC/GND	NC/GND	Internally connected, connect externally to ground or leave floating
8	NC/GND	NC/GND	Internally connected, connect externally to ground or leave floating
9	S2	I/O	Switch input
10	SM	NC	For thermal dissipation only, leave floating
11	S1	I/O	Switch input

(1) P = power, GND = ground, NC = no connect

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
V_{VDD}	Primary side supply voltage(2)	–0.3	20.7	V
V_{EN}	Enable voltage(2)	–0.3	20.7	V
$I_{S1,S2}$	Switch current	–50	50	mA
I_{AVA}	Repetitive avalanche rating, TPSI2140-Q1 (3)	–2	2	mA
I_{AVA}	Repetitive avalanche rating, TPSI2140T-Q1(3)	–5	5	mA
I_{AVA_tran}	Transient avalanche rating(4)	–5	5	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to GND.
(3) Cumulative of 5 minutes accumulated over lifetime in increments of 60 second periods, duty cycle < 10%.
(4) Maximum of 1 second period.

6.2 ESD Ratings

				VALUE	UNIT
HBM_{Prim}	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2(2)	Primary Side Pin No. 1-8	±2000	V
HBM_{Sec}		Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 1C(2)	Secondary Side Pin No. 9-11	±1000	V
CDM	Electrostatic discharge	Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4(3)		±750	V
IEC6100-4-2	Electrostatic discharge	Contact/Air Discharge, per IEC 61000-4-2(2) (3)	Isolation Barrier	±4000	V

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
(3) Testing is carried out in air or oil to determine the intrinsic capability of the device.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{VDD}	Primary side supply voltage[1]	4.5		20	V
V_{EN}	Enable voltage[1]	0		20	V
$V_{S2\text{-}S1}$	Switch input voltage	–1400		1400	V
$I_{S1,S2}$	Switch current	–50		50	mA
T_A	Ambient operating temperature	–40		125	°C
T_J	Junction operating temperature	–40		150	°C

(1) All voltage values are with respect to GND

6.4 Thermal Information

THERMAL METRIC [1]		DEVICE	UNIT
		DWQ (SOIC)	
		11 PINS	
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	70	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	22	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	26	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	21	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External Creepage[1]	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>10.5	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-III	
		Rated mains voltage ≤ 1000 V_{RMS}	I-II	
DIN V VDE 0884-11 (VDE V 0884-11): 2016-12[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1500	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test; see Figure 1	1000	V_{RMS}
		DC voltage	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification) $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	5300	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.3 \times V_{IOSM} = 7800\ V_{PK}$ (qualification)	6000	V_{PK}
q_{pd}	Apparent charge[4]	Method a: After I/O safety test subgroup 2/3,$V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM} = 1800\ V_{PK}$, t_m = 10 s	≤5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.3 \times V_{IORM}$ = 1950 V_{PK}, t_m = 10 s	≤5	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.5 \times V_{IORM} = 2250\ V_{PK}$, t_m = 1 s	≤5	
C_{IO}	Barrier capacitance, input to output[5]	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz	4	pF
R_{IO}	Insulation resistance, input to output[5]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		40/150/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification) $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	3750	V_{RMS}
Misc.				
V_{ISO}	Withstand isolation voltage		5300	V_{DC}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

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6.6 Safety-Related Certifications

<table>
<tr><th>VDE</th><th>CSA</th><th>UL</th><th>CQC</th><th>TUV</th></tr>
<tr><td>Plan to certify according to DIN V VDE V 0884-11:2017-01</td><td rowspan="3">Not Planned, contact TI to request.</td><td>Plan to certify according to UL 1577 Component Recognition Program</td><td rowspan="3">Not Planned, contact TI to request.</td><td rowspan="3">Not Planned, contact TI to request.</td></tr>
<tr><td>Maximum transient isolation voltage, 5300 V_{PK};
Maximum repetitive peak isolation voltage, 1500 V_{PK};
Maximum surge isolation voltage, 6000 V_{PK}</td><td>Single protection, 3750 V_{RMS}</td></tr>
<tr><td>Certificate planned</td><td>Certificate planned</td></tr>
</table>

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6.7 Electrical Characteristics

Unless otherwise noted, all minimum/maximum specifications are over recommended operating conditions. All typical values are measured at T_J = 25C, V_{VDD} = 5V, V_{EN} = 5V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PRIMARY SIDE SUPPLY (VDD)						
V_{UVLO_R}	VDD undervoltage threshold rising	VDD rising	2.5		4.4	V
V_{UVLO_F}	VDD undervoltage threshold falling	VDD falling	2.35		4.3	V
V_{UVLO_HYS}	VDD undervoltage threshold hysteresis		60		500	mV
I_{VDD_ON}	VDD current, device powered on	T_J = 25°C		7.5	8.5	mA
	VDD current, device powered on	–40°C ≤ T_J ≤ 150°C		7.5	8.5	mA
I_{VDD_OFF}	VDD current, 5 V, device powered off	V_{VDD} = 5 V, V_{EN} = 0 V, T_J = 25°C			6	µA
		V_{VDD} = 5 V, V_{EN} = 0 V, T_J = 105°C			10	µA
		V_{VDD} = 5 V, V_{EN} = 0 V, T_J = 125°C			16	µA
		V_{VDD} = 5 V, V_{EN} = 0 V, –40°C ≤ T_J ≤ 150°C			30	µA
	VDD current, 20 V, device powered off	V_{VDD} = 20 V, V_{EN} = 0 V, T_J = 25°C			10.5	µA
		V_{VDD} = 20 V, V_{EN} = 0 V, T_J = 105°C			17	
		V_{VDD} = 20 V, V_{EN} = 0 V, T_J = 125°C			25	
		V_{VDD} = 20 V, V_{EN} = 0 V, –40°C ≤ T_J ≤ 150°C			40	
FET CHARACTERISTICS (S1, S2)						
R_{DSON}	On resistance	I_O = 2 mA, T_J = 25°C		130	175	Ω
		I_O = 2 mA, T_J = 85°C		176	235	
		I_O = 2 mA, T_J = 105°C		192	250	
		I_O = 2 mA, T_J = 125°C		210	275	
		I_O = 2 mA, –40°C ≤ T_J ≤ 150°C			300	
$I_{OFF_TPSI2140}$	TPSI2140-Q1 Off leakage, 1400 V	V = +/–1400 V, T_J = 25°C		0.02	0.1	µA
		V = +/–1400 V, T_J = 85°C			0.5	
		V = +/–1400 V, T_J = 105°C			1.5	
		V = +/–1400 V, T_J = 125°C			6	
		V = +/–1400 V, –40°C ≤ T_J ≤ 150°C			50	
	TPSI2140-Q1 Off leakage, 1000 V	V = +/–1000 V, T_J = 25°C		0.02	0.1	µA
		V = +/–1000 V, T_J = 85°C			0.3	
		V = +/–1000 V, T_J = 105°C			1	
		V = +/–1000 V, T_J = 125°C			4	
		V = +/–1000 V, –40°C ≤ T_J ≤ 150°C			20	
$I_{OFF_TPSI2140T}$	TPSI2140T-Q1 Off leakage, 1400 V	V = +/–1400 V, T_J = 25°C		0.02	0.1	µA
		V = +/–1400 V, T_J = 85°C			0.5	
		V = +/–1400 V, T_J = 105 °C			1.5	
		V = +/–1400 V, T_J = 125°C			6	
		V = +/–1400 V, –40°C ≤ T_J ≤ 150°C			50	
	TPSI2140T-Q1 Off leakage, 1000 V	V = +/–1000 V, T_J = 25°C		0.02	0.1	µA
		V = +/–1000 V, T_J = 85°C			0.3	
		V = +/–1000 V, T_J = 105°C			1	
		V = +/–1000 V, T_J = 125°C			4	
		V = +/–1000 V, –40°C ≤ T_J ≤ 150°C			20	

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6.7 Electrical Characteristics (continued)

Unless otherwise noted, all minimum/maximum specifications are over recommended operating conditions. All typical values are measured at T_J = 25C, V_{VDD} = 5V, V_{EN} = 5V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{AVA}	Avalanche voltage	I_O = 10 µA, T_J = 25°C	1540	1640	1700	V
		I_O = 100 µA, T_J = 150°C	1540	1740	1900	
		I_O = TBD µA, T_J = 200°C	TBD	TBD	TBD	
		I_O = TBD µA, T_J = 250°C	TBD	TBD	TBD	
V_{SM_OFF}	SM voltage	S1 = 1000 V, S2 = 0 V OR S2 = 1000 V, S1 = 0 V	370		630	V
C_{OSS}	S1, S2 capacitance	$V_{S1,S2}$ = 0 V, SM float, F = 1 MHz		TBD		pF
T_{TAP_R}	Thermal Avalanche Protection rising threshold			180		C
T_{TAP_F}	Thermal Avalanche Protection falling threshold		125			C
T_{TAP_HYS}	Thermal Avalanche Protection hysteresis			20		C
LOGIC-LEVEL INPUT (EN						
V_{IL}	Input logic low voltage		0.0		0.8	V
V_{IH}	Input logic high voltage		2.1		20.0	V
V_{HYS}	Input logic hysteresis		100	200	300	mV
I_{IL}	Input logic low current	V_{EN} = 0 V	–0.1	0	0.1	µA
I_{IL}	Input logic low current	V_{EN} = 0.8 V	2	4	6.5	µA
I_{IH}	Input logic high current	V_{EN} = 5 V	10	22	50	µA
I_{IH}	Input logic high current	V_{EN} = 20 V	100	175	350	µA
I_{VDD_FS}	VDD fail-safe current	V_{EN} = 20 V, V_{VDD} = 0 V	–0.1		0.1	µA
R_{PD}	Pulldown resistance	Two point measurement, V_{EN} = 0.5 V and V_{EN} = 0.8 V	100	200	350	kΩ
NOISE IMMUNITY						
CMTI	Common-mode transient immunity	$\|V_{CM}\|$ = 1000 V			100.0	V/ns

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6.8 Switching Characteristics

Unless otherwise noted, all minimum/maximum specifications are over recommended operating conditions. All typical values are measured at T_A = 25C, V_{VDD} = 5V, V_{EN} = 5V.

MODE	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Switching Characteristics							
EN switching	t_{PD_ON}	Input HI to Output voltage falling propagation delay	V_{IN} = 1000 V R_L = 1 MΩ	50		300	µs
	t_F	Output fall time		20		100	
	t_{ON}	Input HI to Output LO delay		70		400	
	t_{PD_OFF}	Input LO to Output voltage rising propagation delay		80		200	
	t_R	Output rise time		20		50	
	t_{OFF}	Input LO to Output HI delay		100		250	
EN and VDD switching	t_{PD_ON}	Input HI to Output voltage falling propagation delay	V_{IN} = 1000 V R_L = 1 MΩ	130		500	µs
	t_F	Output fall time		20		100	
	t_{ON}	Input HI to Output LO delay		150		600	
	t_{PD_OFF}	Input LO to Output voltage rising propagation delay		80		200	
	t_R	Output rise time		20		50	
	t_{OFF}	Input LO to Output HI delay		100		250	

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7 Parameter Measurement Information

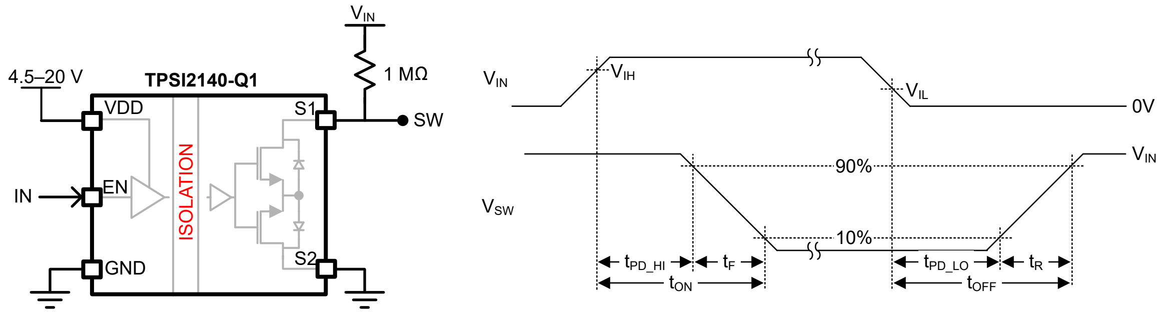

Figure 7-1. Timing Diagram, VDD/EN Pins Seperate

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8 Detailed Description

8.1 Overview

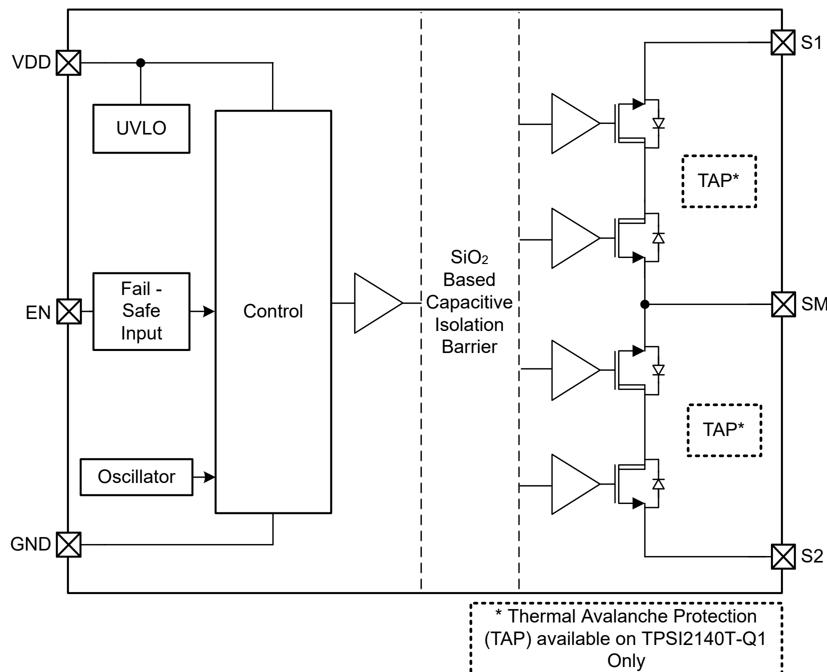
The TPSI2140-Q1 is an isolated solid state relay designed for high voltage automotive and industrial applications. TI's high reliability capacitive isolation technology in combination with back-to-back MOSFETs form a completely integrated solution requiring no secondary side power supply.

As seen in the *Functional Block Diagram*, below the primary side consists of four differential drivers which deliver power and enable logic information to each of the internal MOSFETs on the secondary side. The on-board oscillator controls the frequency of the drivers' operation and the Spread Spectrum Modulation (SSM) controller varies the driver frequency to improve system EMI performance. When the enable pin is brought HI, the oscillator starts and the drivers send power and a logic HI across the barrier. When the enable pin is brought LO or the VDD falls below the UVLO threshold, the drivers are disabled. The lack of activity communicates a logic LO to the secondary side and the MOSFETs are disabled.

Each MOSFET on the secondary side has a dedicated full-bridge rectifier to form its local power supply. These local power supplies feed a band pass amplifier and demodulator which determine the logic state delivered by the primary side through the capacitive isolation barrier. The slew rate drivers control the MOSFETs' gate according to the logic delivered.

The avalanche robust MOSFETs and the thermal benefits of the widened pins on the 11 DWQ package enable the TPSI2140-Q1 to withstand High Potential (HiPot) screening and DC fast charger surge currents of up to 2 mA without requiring any external protection components. The Thermal Avalanche Protection (TAP) feature included in the TPSI2140T-Q1 version of the device further improves the avalanche current capability by monitoring the junction temperature and enabling the MOSFETs to keep the temperature in a safe operating range.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Avalanche Robustness

When the secondary side MOSFETs are avalanching, the device is forced to dissipate a high amount of power. The custom designed 11 DWQ package with widened pins allows the TPSI2140-Q1 to dissipate heat efficiently enough to achieve 2-mA avalanche current capability for 60 second intervals. System designers requiring avalanche current support greater than this level for 60 second intervals should select the TPSI2140T-Q1 device which regulates the device power using the TI's Thermal Avalanche Protection (TAP) feature. For periods less than 1 second, both devices are robust up to 5 mA.

8.3.2 Thermal Avalanche Protection (TAP)

During overvoltage stresses, the TPSI2140T-Q1 device's TAP feature enhances the secondary side MOSFETs when the junction temperature crosses a threshold. This action enables the system designer to reduce the sense resistance in applications like isolation resistance monitoring and improve the accuracy of the measurement. Figure 8-1 shows how the TAP feature regulates the junction temperature during an overvoltage stress.

Each secondary side MOSFET is monitored by a thermal sensor. If the junction temperature rises above T_{TAP_R} the sensor enhances its corresponding MOSFET, reducing the voltage and power across it. The junction temperature decreases, protecting the MOSFET from thermal stress. When the junction temperature falls below T_{TAP_F}, the sensor disengages the MOSFET returning it to a blocking state.

If the overvoltage stress is still present and the junction temperature rises above T_{TAP_R} again, the sensor again enhances the MOSFET. This action repeats until the overvoltage stress is removed.

The thermal sensor is powered by the MOSFET drain voltage and does not require the presence of the primary side supply to operate.

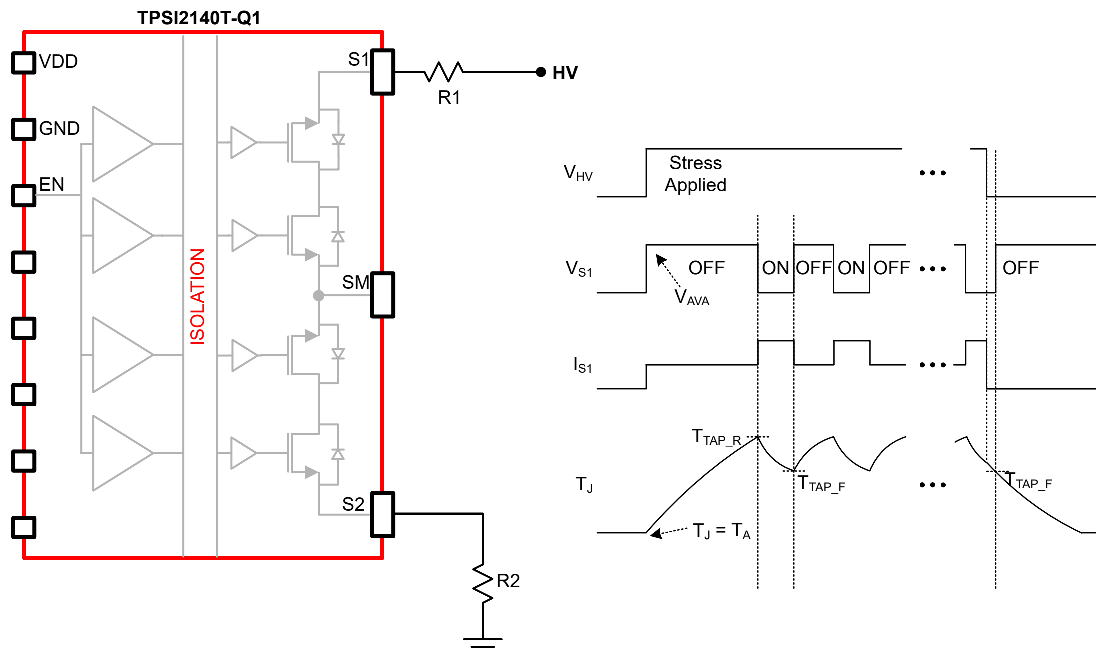

Figure 8-1. Thermal Avalanche Protection (TPSI2140T-Q1 Only)

8.4 Device Functional Modes

Table 8-1. Device Functional Modes

VDD	EN	S1-S2 State	COMMENTS
Powered Up[(1)]	L	OFF	VDD current is in OFF state range.
	H	ON	VDD current is in ON state range.
Powered Down[(2)]	L	OFF	VDD current is in OFF state range.
	H	OFF	Primary side analog is powered on, VDD current is between OFF state and ON state.

(1) VDD ≥ VDD undervoltage rising threshold.
(2) VDD ≤ VDD undervoltage falling threshold.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPSI2140-Q1 is a 1400-V, 50-mA automotive isolated switch used for high voltage measurements or high voltage switching across an isolation barrier. Intended applications include insulation resistance monitoring in solar panels, EV chargers, and EV BMS. The device enables the system designer to reduce cost and improve reliability by replacing mechanical relays and optically isolated devices. TPSI2140-Q1's enable input is fail safe and does not need to be driven from the same domain as its power supply.

The TPSI2140-Q1 supports an input voltage range of 4.5 V to 20 V on the primary supply pin and a logic high of 2 V to 20 V on the enable pin. The secondary side supports switching a high voltage range from –1400 V to 1400 V.

9.2 Typical Application

Insulation Resistance Monitoring

A common use case for the TPSI2140-Q1 is insulation resistance monitoring. Insulation resistance monitoring is also known as isolation check, insulation check, insulation monitoring, isolation monitoring, and so forth. In an ideal automotive electric vehicle system, the high voltage battery pack is entirely disconnected from the chassis of the car to protect the driver or electrical components inside from being damaged. This action theoretically measures an infinite resistance between the HV battery and chassis ground. In reality, however, there is a finite amount of resistance that must be monitored and can be modeled in the figure shown below as RISOP and RISON.

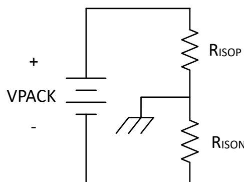

Figure 9-1. Insulation Resistance Model

There are multiple ways to design a system using TPSI2140-Q1 to measure these unknown insulation resistances, RISOP and RISON. Some methods rely on a microcontroller taking measurements from a high voltage board, while others rely on a microcontroller placed on a low voltage board, which is referred to as Battery V- Reference and Chassis Ground Reference respectively. The main difference between the two is where the MCU takes the GND reference. An example of a Battery V- MCU is the BQ79631-Q1 URI sensor.

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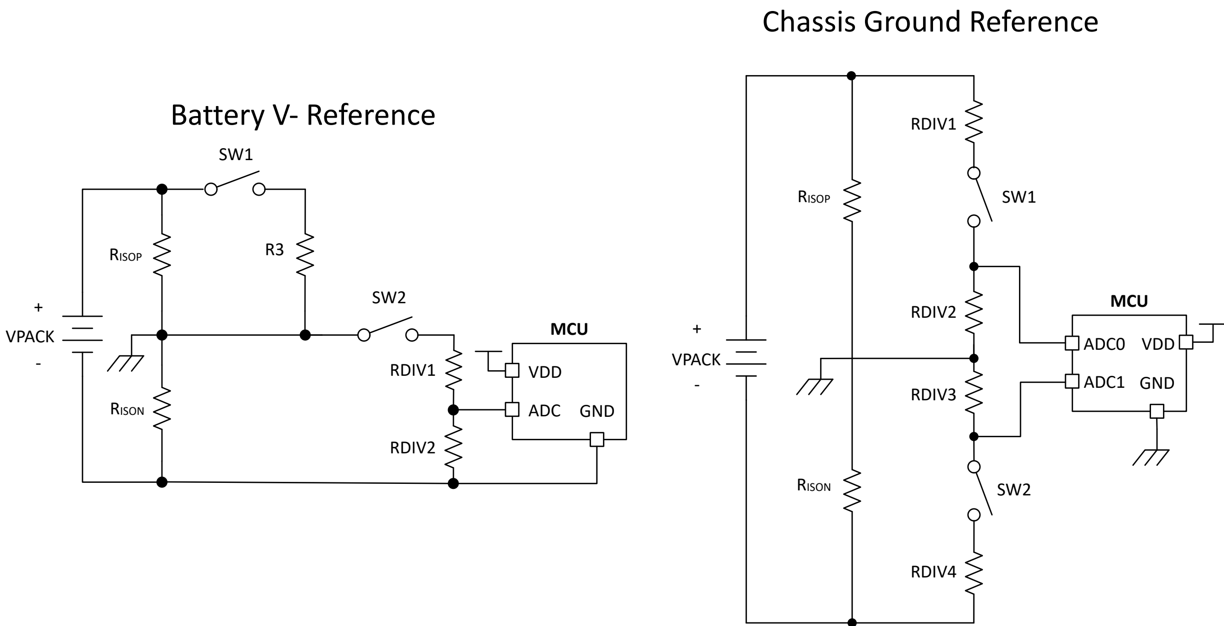

Figure 9-2. Different MCU ADC Reference Examples

A Battery V- Reference MCU-based architecture is shown below using the TPSI2140-Q1 modeled as a switch (SW1 and SW2). SW2 is used to safely disconnect the ADC pin from the circuit and reduce leakage current when measurements are not being taken. RDIV1 and RDIV2 form a voltage divider to keep the ADC voltage below its maximum voltage rating (for example, 5 V for a microcontroller).

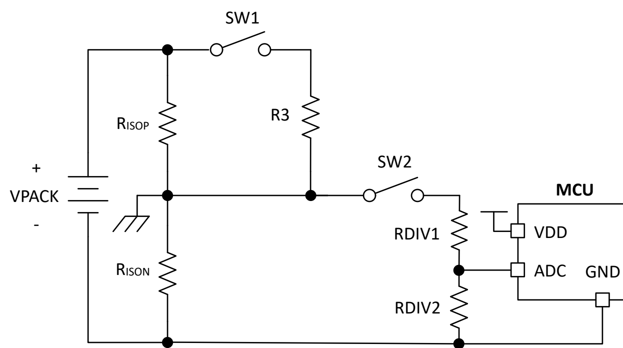

Figure 9-3. Battery V- Reference Architecture

In this setup, two voltage measurements are taken at ADC. The first measurement is used to obtain the relation of RISOP to RISON. The second measurement is used to obtain the relation of RISOP in parallel with R3, to RISON.

- V_{ADC1} measurement 1: SW1 open, SW2 closed
- V_{VADC2} measurement 2: SW1 closed, SW2 closed

The initial conditions below show how to solve the systems of equations:

Given:

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- R3 = 500 kΩ
- RDIV1 = 70 kΩ
- RDIV2 = 2 kΩ
- VPACK = 800 V

Record the following measurements:

- V_{ADC1} = 1.737 V
- V_{ADC2} = 4.017 V

The voltage across R_{ISON} condition 1 is shown in the figure below:

$$V_{RISON1} = V_{PACK} \times \frac{R_{ISON}||(R_{DIV1}+R_{DIV2})}{R_{ISOP}+(R_{ISON}||R_{DIV1}+R_{DIV2})} \tag{1}$$

$$V_{ADC1} = V_{RISON1} \times \frac{R_{DIV2}}{R_{DIV1}+R_{DIV2}} \tag{2}$$

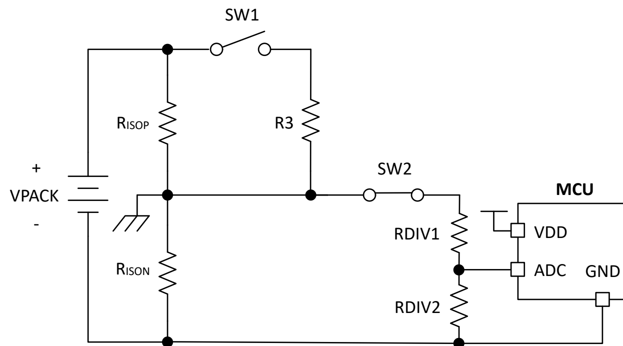

Figure 9-4. Battery V- Reference Architecture Condition 1 ADC1 SW1 Open, SW2 Closed

Now solve for condition 2 shown below:

$$V_{RISON2} = V_{PACK} \times \frac{R_{ISON}||(R_{DIV1}+R_{DIV2})}{(R_{ISOP}||R_3)+(R_{ISON}||(R_{DIV1}+R_{DIV2})} \tag{3}$$

$$V_{ADC2} = V_{RISON2} \times \frac{R_{DIV2}}{R_{DIV1}+R_{DIV2}} \tag{4}$$

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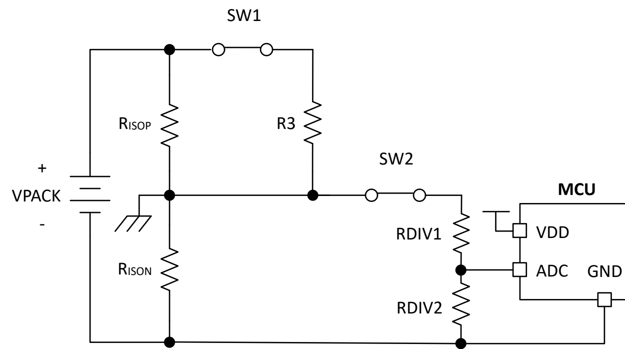

Figure 9-5. Battery V- Reference Architecture Condition 2 ADC2 SW1 Closed, SW2 Closed

With two equations and two unknowns, solve for RISOP and RISON:

R_{ISOP} = 801 kΩ

R_{ISON} = 1.2 MΩ

Another possible setup, chassis ground reference architecture, is shown below. Here, the microcontroller measures the voltage across RDIV2 and RISOP can be calculated by a voltage divider equation.

- VADC0: SW1 closed, SW2 open

$$V_{ADC0} = V_{RDIV2} = V_{PACK}\frac{(R_{ISOP}||(R_{DIV1}+R_{DIV2}))}{(R_{ISOP}||(R_{DIV1}+R_{DIV2})+R_{ISON})} \times \frac{R_{DIV2}}{R_{DIV1}+R_{DIV2}} \quad (5)$$

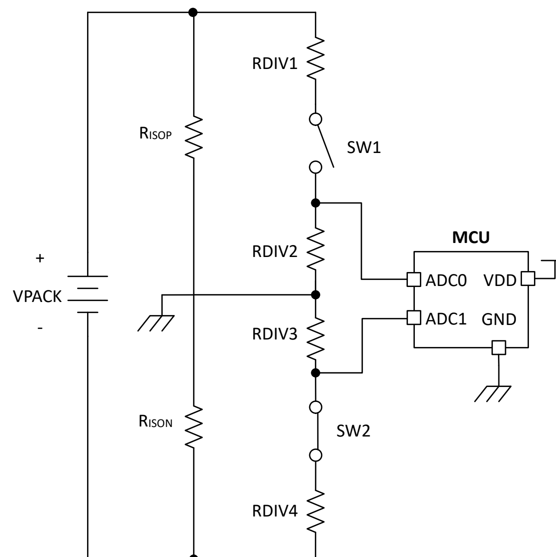

Figure 9-6. Chassis Ground Reference Architecture Condition 1

- VADC1: SW1 open, SW2 close

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$$V_{ADC1} = V_{RDIV4} = -V_{PACK}\frac{(R_{ISON}||(R_{DIV3}+R_{DIV4}))}{(R_{ISON}||(R_{DIV3}+R_{DIV4}))+R_{ISOP})} \times \frac{R_{DIV3}}{R_{DIV3}+R_{DIV4}} \quad (6)$$

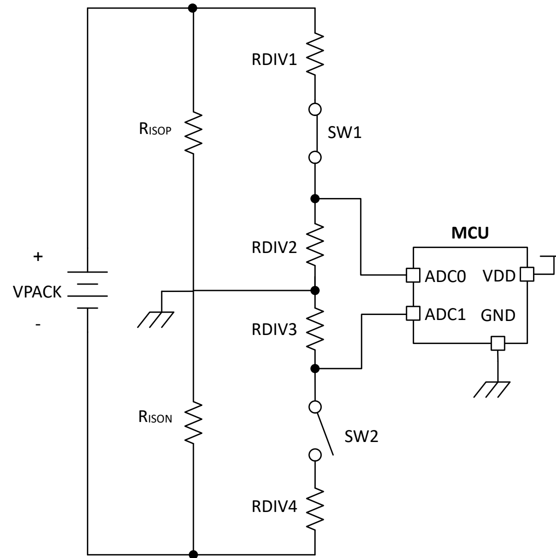

Figure 9-7. Chassis Ground Reference Architecture Condition 2

The circuits in Figure 9-8 and Figure 9-9 show typical application diagrams for isolation check with a pinout.

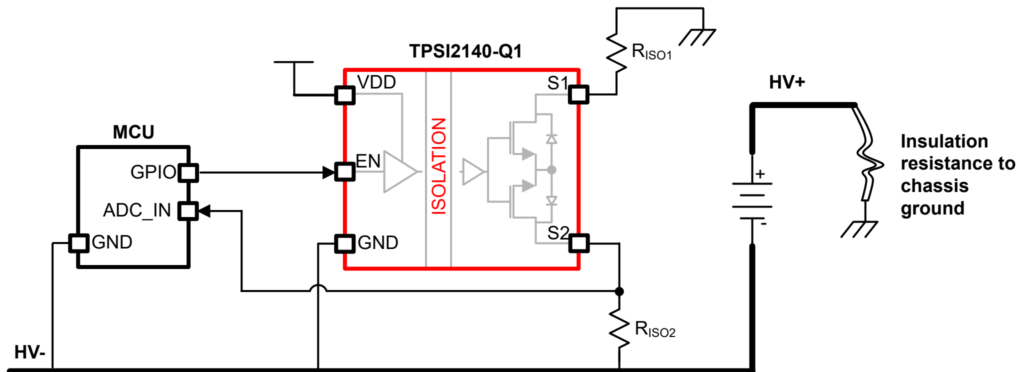

Figure 9-8. TPSI2140-Q1 Insulation Resistance Monitoring – Battery V- Reference

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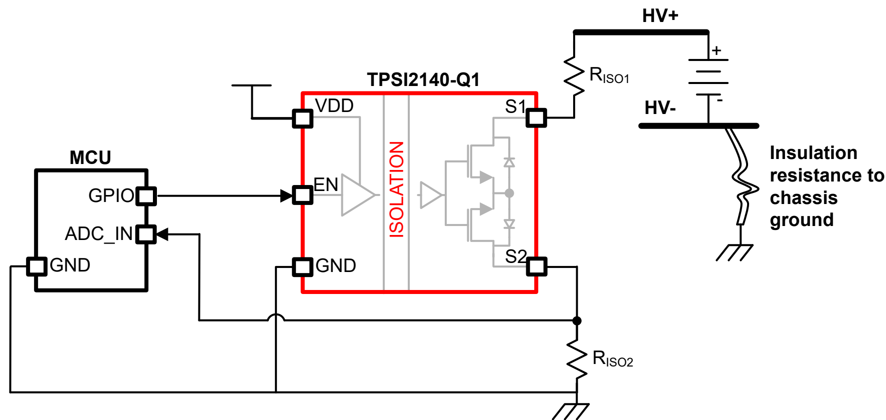

Figure 9-9. TPSI2140-Q1 Insulation Resistance Monitoring – Chassis Ground Reference

9.2.1 Design Requirements

Table 9-1 lists the Design Requirements for a typical Isolation Monitoring Application using a low voltage MCU to control the TPSI2140-Q1.

Table 9-1. Design Parameters TPSI2140-Q1 Isolation Resistance Monitoring – Chassis Ground Reference MCU

PARAMETER	VALUE
Max HV supply voltage	1000V
Primary side supply (V_{VDD})	5 V ±10 %
Isolation withstand voltage test	3000 V
	60 s
Surge voltage (IEC61000-3-5)	2500 V
Minimum isolation resistance	100 Ω / V

9.2.2 Detailed Design Procedure Chassis Ground Reference

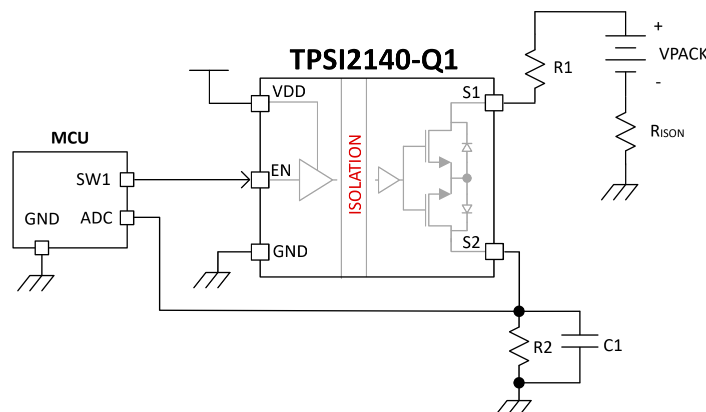

Figure 9-10. Chassis Ground Reference

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R1 Selection

Because the TPSI2140-Q1 is designed to survive up to 2 mA of avalanche current, R1 must be sized to limit current in an overvoltage condition. A high potential 3500-V test, S1 to S2 clamps above 1540 V (V_{AVA} minimum) R1 must be greater than 1 MΩ to limit avalanche current under 2 mA.

$$I_{AVA} = \frac{V_{HIPOT} - V_{S1-S2}}{R1} = \frac{3500V - 1.54V}{1\ \ M\Omega} = 1.96mA \quad (7)$$

Sizing R1 for a surge test follows a similar calculation but also must account for VPACK. The table below shows a quick overview for sizing R1 based on the overvoltage condition.

- Overvoltage = V_{HIPOT}

or

- Overvoltage = VPACK + V_{SURGE}

Overvoltage	R1 Minimum	Recommended R1 Resistor
2000 V	230 kΩ	232 kΩ 0.1% HV
2500 V	480 kΩ	481 kΩ 0.1% HV
3000 V	730 kΩ	732 kΩ 0.1% HV
3500 V	980 kΩ	1 MΩ 0.1% HV

C1 Selection and Measurement Accuracy

C1 is for smoothing the ADC pin voltage reading and must be sized to keep 1 / (R2*C1) below 8 MHz for filtering purposes.

- R2 = 6.3 kΩ

C1 > 20 pF

Using low tolerance resistors such as 0.1% is best for measurement accuracy. Because the absolute maximum value of Rdson is 250 Ω, given R1 = 1 MΩ and R2 = 6.3 kΩ, Rdson affects total resistance by 0.25%. ADC accuracy and battery pack voltage can also impact accuracy.

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10 Power Supply Recommendations

To help ensure a reliable supply voltage, TI recommends that a capacitor is placed between the VDD and GND. This capacitance consists of a 0.1-µF bypass capacitor for high frequency decoupling. The capacitor must be as close to the device's VDD pin as possible < 5 mm.

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11 Layout

11.1 Layout Guidelines

Component placement:

Decoupling capacitors intended for the filtering of high frequency signals must be placed as close as possible to the device pins. This action reduces the effect of trace inductance and achieves a cleaner signal.

EMI considerations:

To minimize EMI, maximize the ratio of the primary GND plane area to secondary GND area. As shown in the layout images for the front and back of the EVM, the primary GND plane is much larger than the small trace connecting the secondary side to the HV- terminal.

High-voltage considerations:

To ensure isolation performance between the primary and secondary side, avoid placing PCB or copper below the device. TI recommends a PCB cutout or groove to prevent contamination that can compromise the isolation performance. To ensure voltage creepage and clearance standards, avoid placing PCB or copper between the S1 to SM and SM to S2 that would reduce the clearance between the metal pins.

Thermal considerations:

Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction-to-board thermal impedance (θJB). A trace or plane can be connected to the SM pin for improved heat dissipation as shown in the layout images and layers of TPSI2140Q1EVM.

11.2 Layout Example

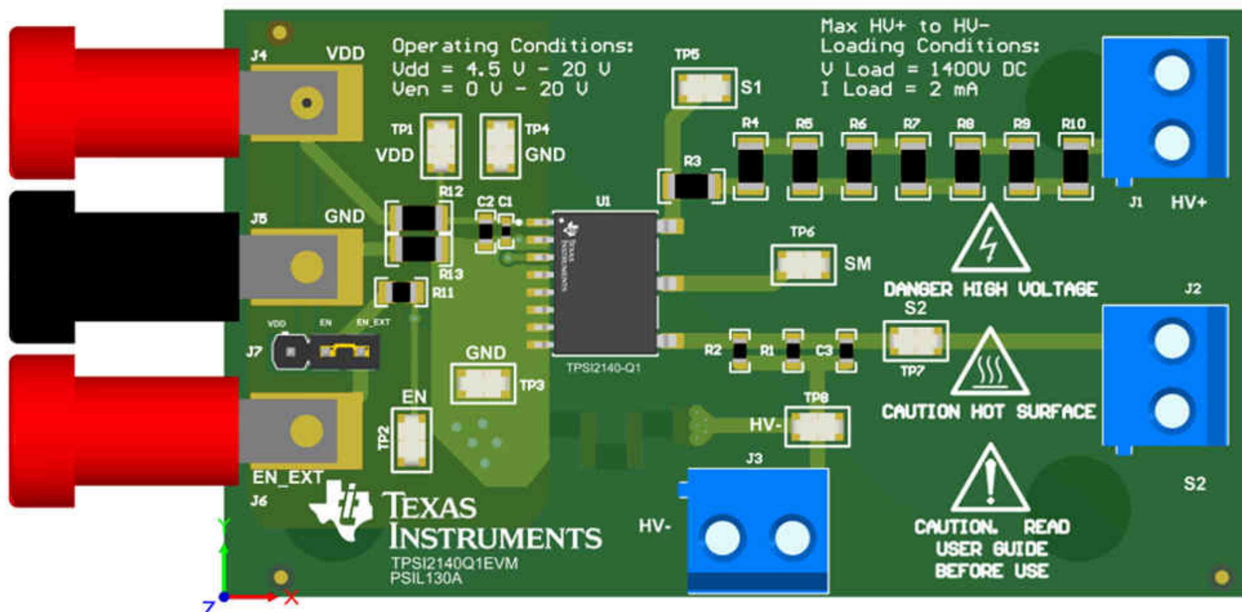

Figure 11-1. TPSI2140Q1EVM Example Layout

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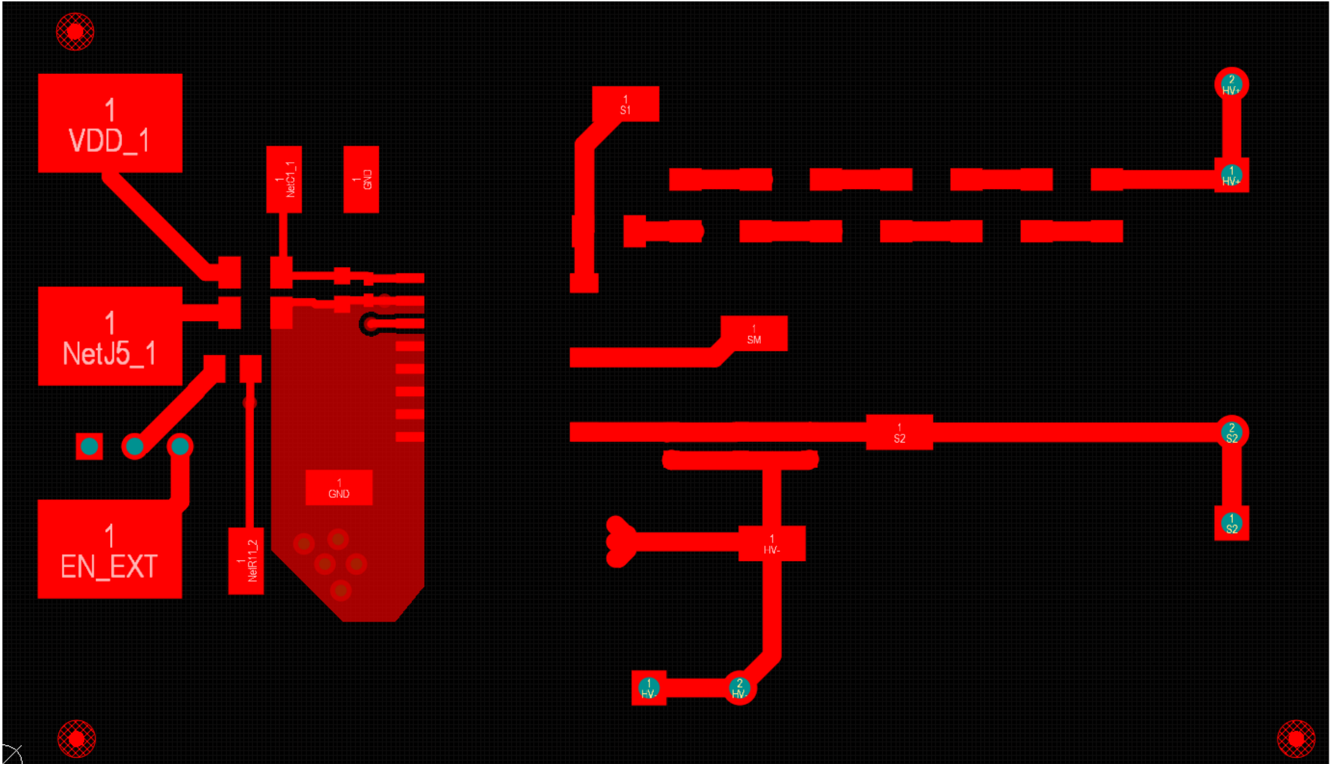

Figure 11-2. TPSI2140Q1EVM Top Layer

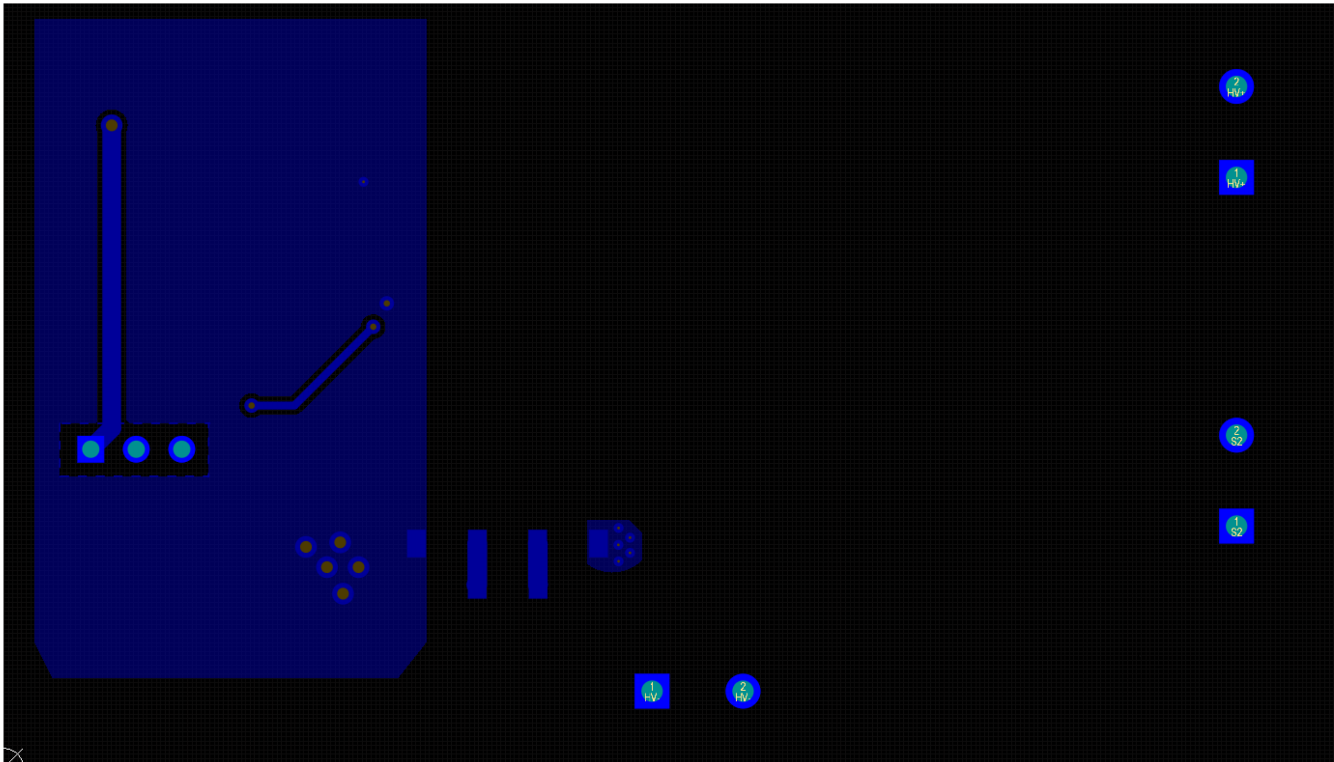

Figure 11-3. TPSI2140Q1EVM Bottom Layer

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12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.3 Trademarks

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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

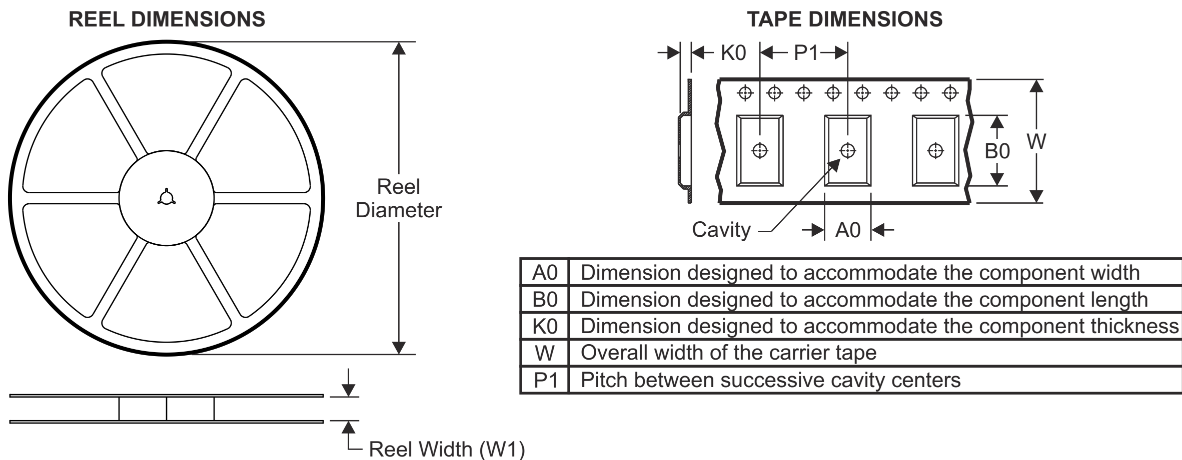
TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

13 Mechanical, Packaging, and Orderable Information

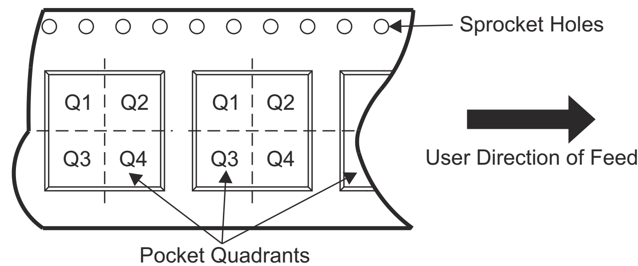
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Tape and Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTPSI2140QDWQR	SOIC	DWQ	11	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

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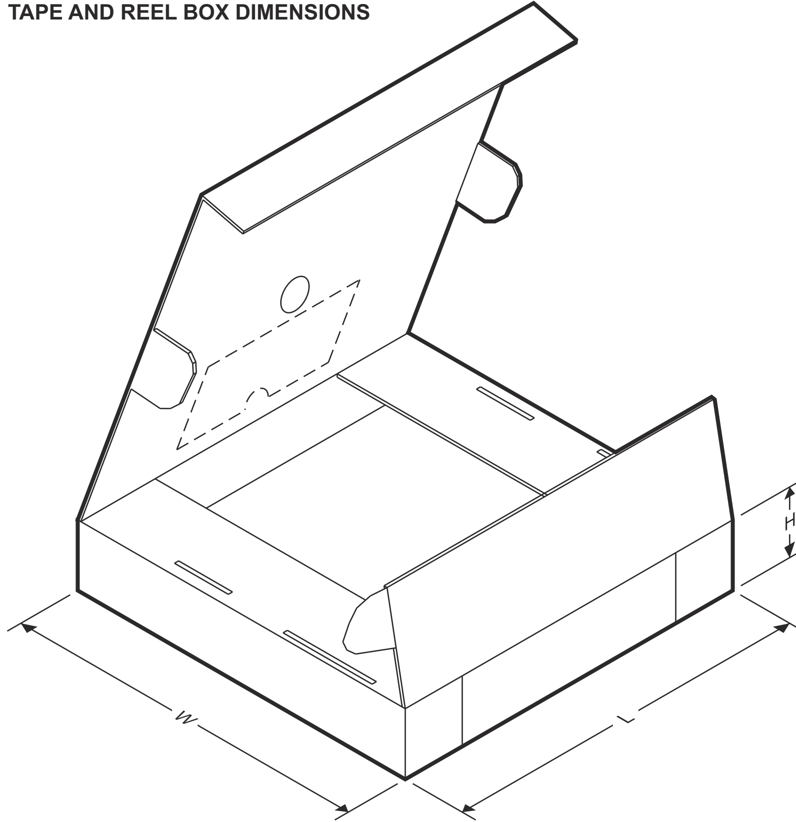
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTPSI2140QDWQR	SOIC	DWQ	11	1000	350.0	350.0	43.0

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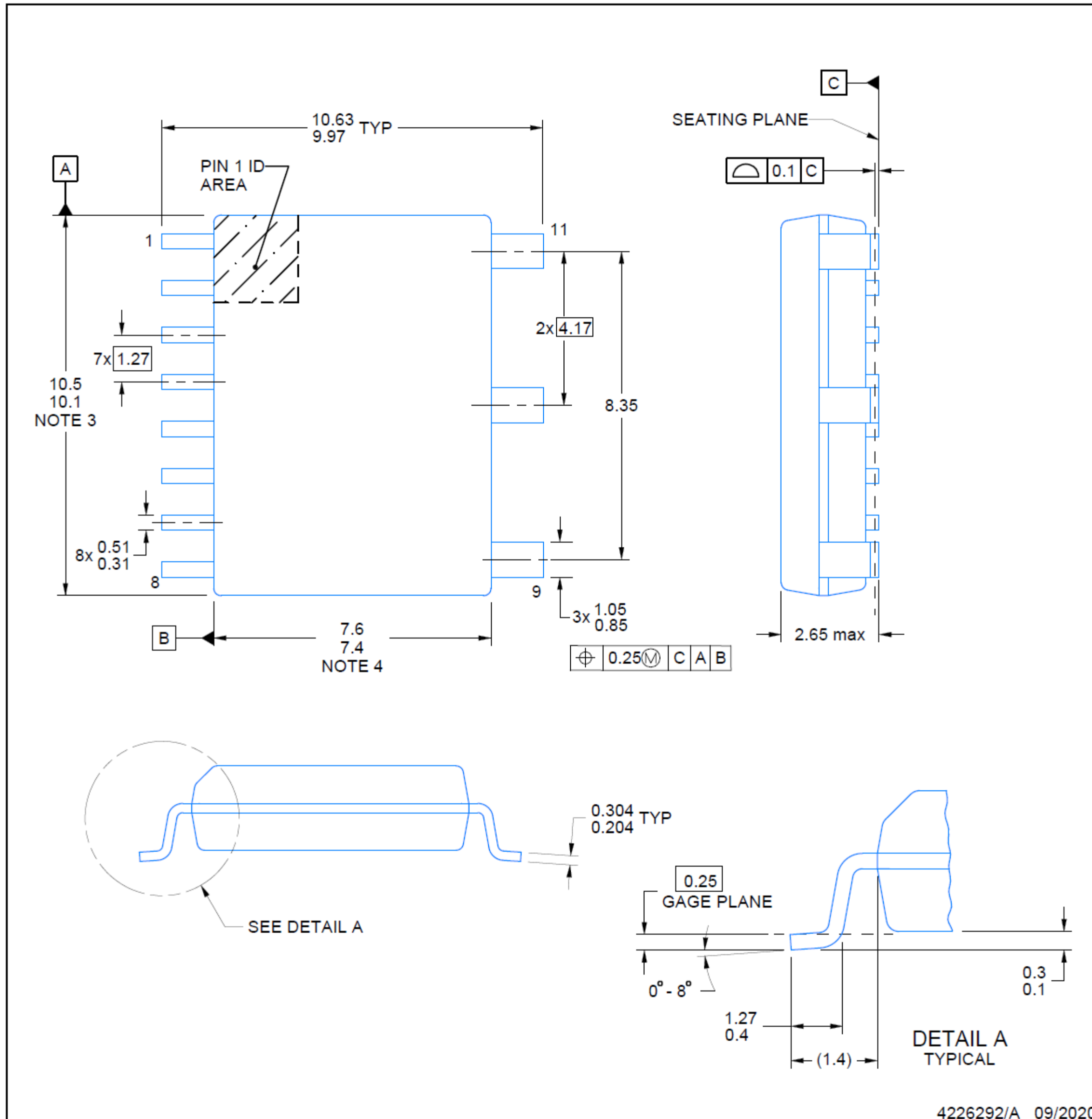
PACKAGE OUTLINE

DWQ0011A

SOIC - 2.65 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

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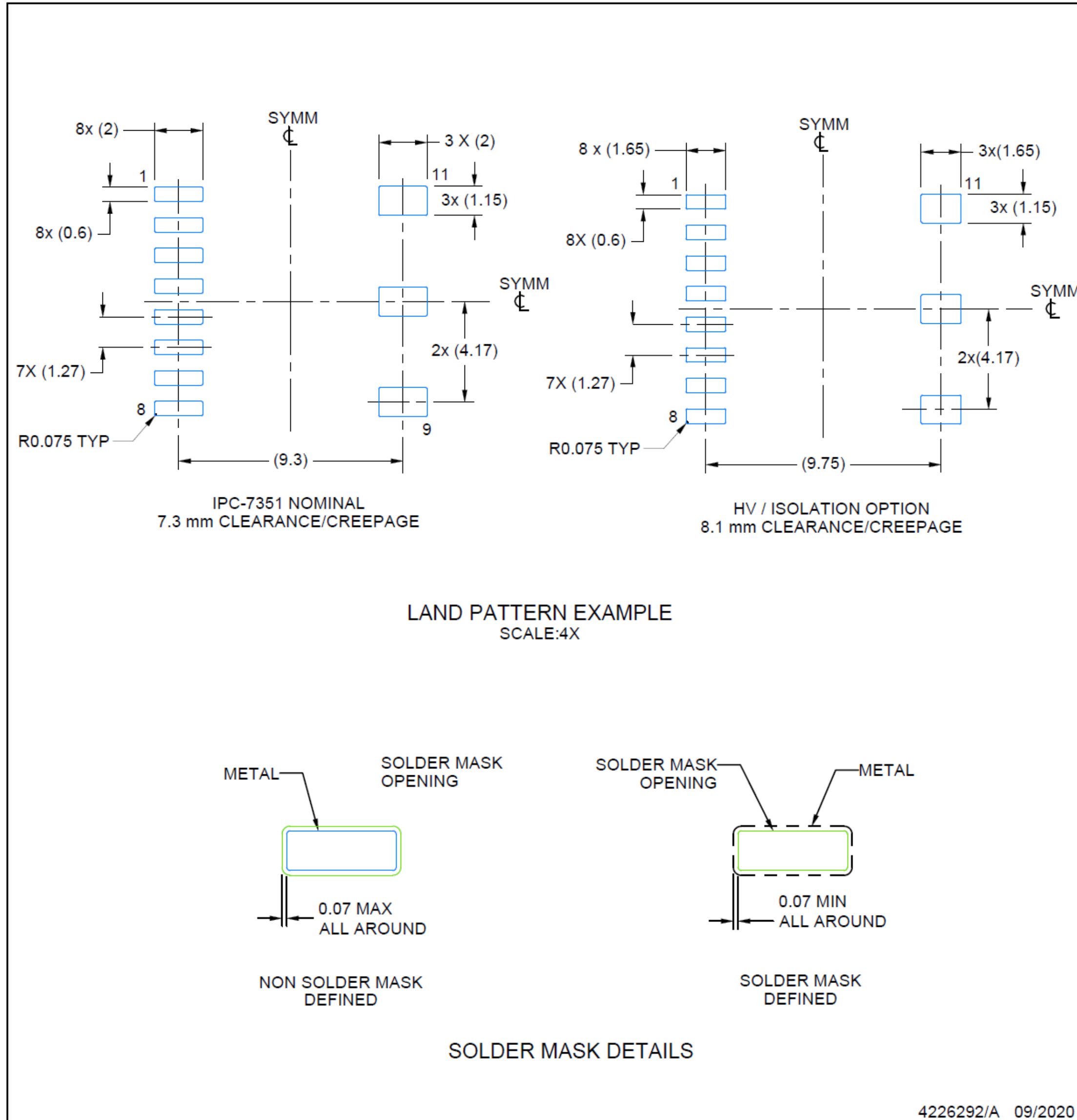
EXAMPLE BOARD LAYOUT

DWQ0011A **SOIC - 2.65 mm max height**

SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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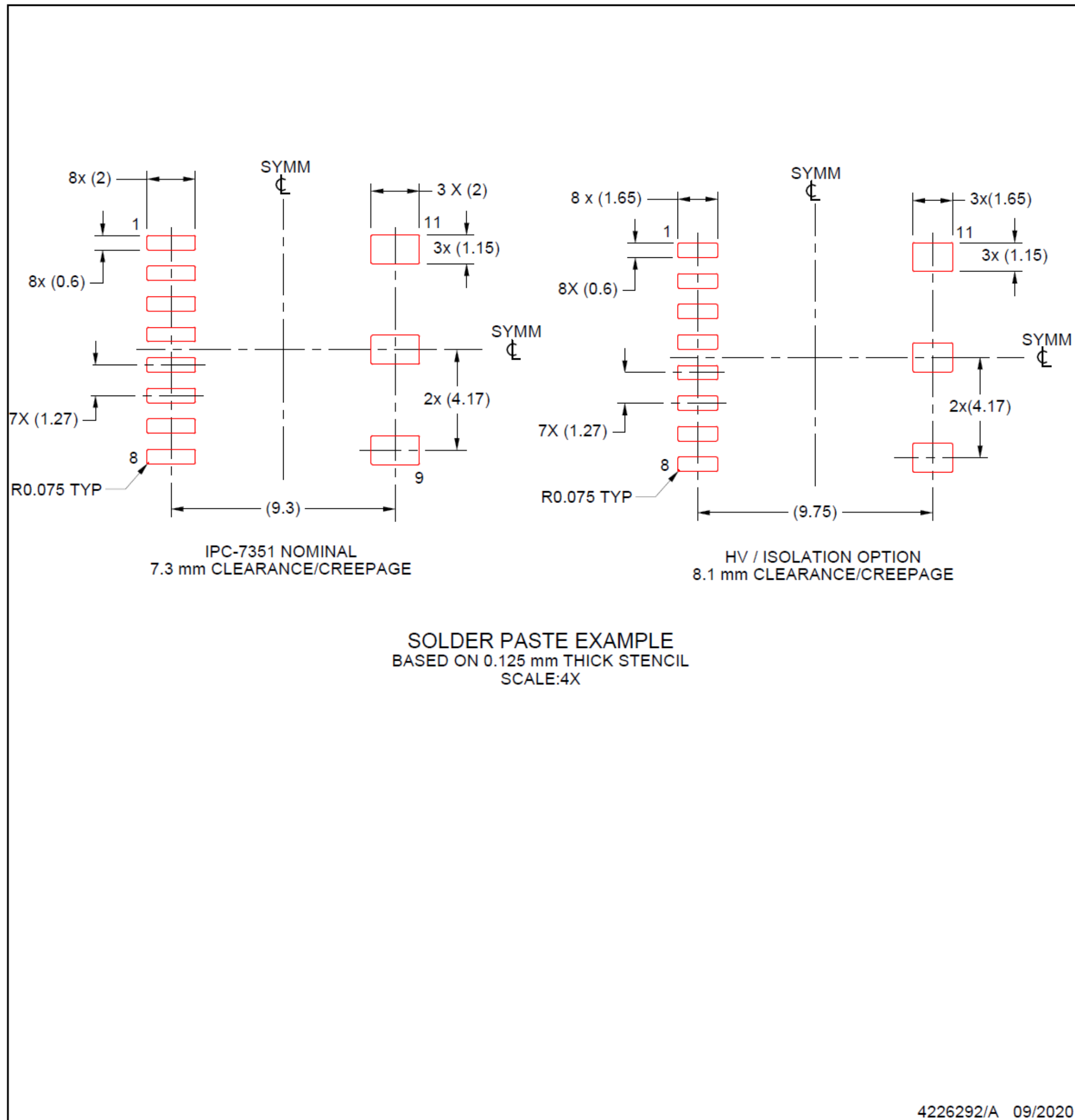
EXAMPLE STENCIL DESIGN

DWQ0011A SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XTPSI2140QDWQRQ1	ACTIVE	SOIC	DWQ	11	1000	TBD	Call TI	Call TI	-40 to 125		Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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