Application Report

Understanding Power Module Operating Limits

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ABSTRACT

Buck power modules offer a high level of integration that simplifies the power supply design process and helps reduce time to market. The benefits of power modules are covered in other TI publications (1, 2). Having the inductor and other passive components integrated translates to smaller solution size, fewer design calculations and components to select and qualify, and predictable efficiency performance. However, all buck regulators have limits, and the fixed inductor contributes to setting the allowed operating boundaries of a buck power module. This application report will discuss the driving factors behind a module's operating limits, to help engineers select and configure power modules most effectively in their designs. The TPSM5D1806 dual 6-A output buck power module is used as an example for the discussions in this application report.

Table of Contents

List of Figures

List of Tables

Trademarks

1 Introduction

Open any power module data sheet and its front page will advertise the module's load current capability and input and output voltage range. A module with selectable or adjustable switching frequency will advertise its frequency options on the data sheet front page as well. In reality, not all input voltage, output voltage, load current, and switching frequency combinations can be achieved due to timing, current, and thermal limitations. One must look further into the datasheet to better comprehend the module's valid operating conditions.

Power module data sheets include tables and graphs that summarize the maximum load current capability for different input and output voltage ranges, and different switching frequencies, if selectable/adjustable. An example of such a table is shown in Table 1-1 for the TPSM5D1806, which is a dual 6-A output buck power module with four selectable switching frequencies: 500kHz, 1MHz, 1.5MHz, and 2MHz. With this table, one can quickly determine the possible switching frequency choices for a desired input to output voltage conversion and max load current requirement, without needing to perform any calculations and analysis by hand or experimentally. Furthermore, module data sheets provide Safe Operating Area (SOA) curves, which show the maximum allowed ambient temperature versus load current as measured on the evaluation board (EVM), as an aid to quantifying the thermal capabilities of the device.

While these data sheet tables and graphs are useful for quick analysis and assessment of the device's capabilities, they may leave an engineer wanting a deeper understanding of how the operating boundaries of the module have been determined. This understanding can aid an engineer in better selecting, comparing, and configuring power modules for their designs.

Table 1-1. TPSM5D1806 Allowable Switching Frequency

Output Current per Channel	Switching Frequency (kHz)	VIN = 5 V		VIN = 12 V	
		VOUT RANGE		VOUT RANGE	
		MIN	MAX	MIN	MAX
6 A	500	-	-	0.5	0.8
	1000	0.5	0.8	0.7	1.6
	1500	0.5	1.3	1.0	2.4
	2000	0.6	1.8	1.4	3.2
5 A	500	0.5	0.8	0.5	0.9
	1000	0.5	1.8	0.7	2.0
	1500	0.5	3.3	1.0	3.6
	2000	0.6	2.8	1.4	5.5
≤ 4 A	500	0.5	0.9	0.5	0.9
	1000	0.5	3.9	0.7	2.0
	1500	0.5	3.5	1.0	3.6
	2000	0.6	2.8	1.4	5.5

2 Basic Buck Regulator Operation

The fundamental operation of buck regulators is discussed in detail in other application reports (3). While not covered in detail here, an understanding of the basic buck operational waveforms is useful for the discussions in this report. Figure 2-1 shows the basic synchronous buck power stage and the simplified waveforms of the inductor current (i_L) and switching node (v_{SW}) in steady state continuous-conduction mode (CCM) conditions. For simplicity, dead times and resistive components such as MOSFET on-resistances and the inductor DC resistance have not been considered in the analyses and equations in this report.

During the on time, t_{ON}, the high-side (HS) MOSFET is on and the low-side (LS) MOSFET is off. In this state, a positive voltage V_{IN}-V_{OUT} exists across the inductor, which causes the inductor current to ramp up. During the off-time, t_{OFF}, the HS MOSFET is off and LS MOSFET is on. With the switching node at ground, the voltage across the inductor is -V_{OUT}, which causes the inductor current to ramp back down. The switching period, t_{SW}, is the sum of t_{ON} and t_{OFF} and is the inverse of the switching frequency, F_{SW}. The duty cycle, D, can be defined as D = t_{ON} / t_{SW}. In a real buck regulator, the on and off times are dynamically set by the buck's control loop circuitry, which then generates signals to the gate drivers that turn the power MOSFETs on and off.

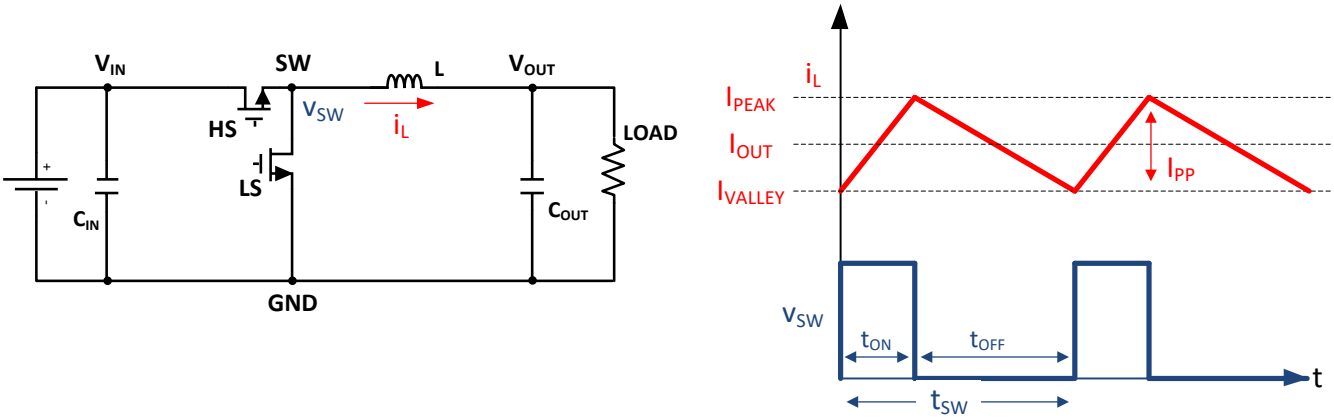


Figure 2-1. Basic synchronous buck regulator and waveforms

3 Impact of Minimum On-Time and Minimum Off-Time

Buck regulators have a minimum on-time and minimum off-time (4) that are the result of gate drive circuitry limitations, control and drive circuit delays, and intentional blanking times. For example, for peak current mode devices with HS MOSFET current sensing, there is a surge in current flowing in the HS FET during its turn-on transition to provide the charge for the LS FET body diode reverse recovery. An initial blanking time in the current sense circuit at the FET turn-on ensures a clean representation of the current is used by the control loop and protection circuitry.

A regulator's minimum on-time and minimum off-time set maximum limits to the allowed switching frequency as defined by Equation 1 and Equation 2 (ignoring resistive voltage drops):

$$F_{SWmax,ton} = \frac{D}{t_{ONmin}} = \frac{V_{OUT}}{V_{IN}\ t_{ONmin}} \quad (1)$$

$$F_{SWmax,toff} = \frac{1-D}{t_{OFFmin}} = \frac{1-\frac{V_{OUT}}{V_{IN}}}{t_{OFFmin}} \quad (2)$$

The TPSM5D1806 has a typical minimum on-time, t_{ONmin}, of 30 ns and minimum off-time, t_{OFFmin}, of 150 ns. Adding some design margin to typical values is recommended, so values of t_{ONmin} of 50 ns and t_{OFFmin} of 200 ns are more conservative numbers used for analysis. Taking an example condition of V_{IN} = 12 V and V_{OUT} = 1 V, the maximum theoretical frequency allowed due to minimum on-time is 1.67 MHz, and maximum theoretical frequency due to minimum off-time is 4.58 MHz. While the minimum off-time is not imposing a limit in this example, the minimum on-time does prohibit the use of the 2-MHz switching frequency option.

When selecting a frequency option for a device with fixed discrete frequency options such as the TPSM5D1806, it is recommended to consider the frequency tolerance as well. The frequency tolerance of the internal oscillator is ±10%, which implies that a device set to 1.5 MHz may have an actual frequency of up to 1.65 MHz, which is close to the 1.67-MHz limit calculated due to min on-time in the previous example. Frequency synchronization to an external clock with tighter accuracy can reduce the required design margins to avoid minimum on- and off-time violations. If the input supply has a wide tolerance or is not well regulated, the maximum and minimum input voltages should be considered when analyzing the maximum allowed frequencies due to minimum on-time and off-time, respectively.

The maximum frequency equations can also be rearranged as Equation 3 and Equation 4 to define the minimum output voltage allowed due to minimum on-time and the maximum output voltage due to minimum off-time at a given frequency and input voltage. The output voltage range due to timing limitations can then be plotted as shown in Figure 3-1 for the TPSM5D1806 at an input voltage of 12 V. The min and max are clamped to the specified output voltage range of the device of 0.5 V to 5.5 V. This figure then makes it easy to read the output voltage range at a given frequency; for example, at 1-MHz switching frequency, the theoretical output voltage range considering only minimum on- and off-times and the basic voltage range limits is 0.7 V to 5.5 V.

$$V_{OUT,min} = F_{SW}\, V_{IN}\, t_{ONmin} \tag{3}$$

$$V_{OUT,max} = (1 - F_{SW}\, t_{OFFmin})\, V_{IN} \tag{4}$$

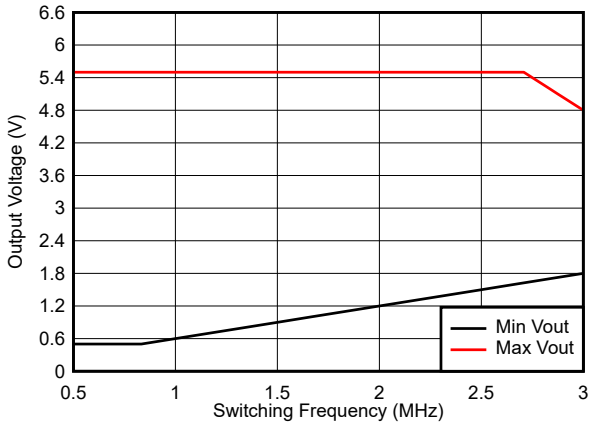


Figure 3-1. TPSM5D1806 Output Voltage Range Due to Minimum On- and Off-Time Only (V_{IN} = 12 V)

4 Impact of Current Limits

Every practical voltage regulator requires current limits to protect its components such as power MOSFETs, inductor, and wiring, which all have inherent maximum current ratings (5).

To the first order, inductor ripple, I_{PP}, and peak inductor or HS FET current, I_{PEAK}, are given by Equation 5 and Equation 6. A HS overcurrent limit typically acts to shut off the buck HS FET when the sensed FET or inductor current hits the current limit value.

$$I_{PP} = \frac{V_{IN} - V_{OUT}}{L} t_{ON} = \frac{V_{IN} - V_{OUT}}{L} \frac{D}{F_{SW}} = \frac{V_{IN} - V_{OUT}}{L} \frac{V_{OUT}}{V_{IN}\, F_{SW}} \tag{5}$$

$$I_{PEAK} = I_{OUT} + \frac{I_{PP}}{2} \tag{6}$$

Given a HS overcurrent limit, $I_{HS,OC}$, the maximum allowed load current is given by Equation 7. In a buck power module where the inductor is fixed, the free variables that influence ripple current are input voltage, output voltage, and switching frequency. For duty cycles below 50%, increasing V_{OUT} or increasing V_{IN} will increase I_{PP} and reduce the maximum allowed load current before hitting the current limit. Operating at a higher switching

frequency may be the only means to reduce inductor ripple current to lower the peak current for a fixed input and output voltage requirement.

$$I_{OUTmax} = I_{HS,OC} - \frac{I_{PP}}{2} \quad (7)$$

The TPSM5D1806 is a dual 6-A output power module which uses integrated 470-nH inductors. Figure 4-1 plots the maximum load current versus output voltage for the four selectable frequency settings of the device assuming an input voltage of 12 V and nominal 470-nH inductor. In a real device, there is a delay from the instant the overcurrent threshold is reached to the time the HS FET is actually turned off, which increases the effective current limit and maximum load current allowed. This delay is factored into the maximum load current curves. In addition, the load current curves are clamped to the maximum specified current of 6 A per channel.

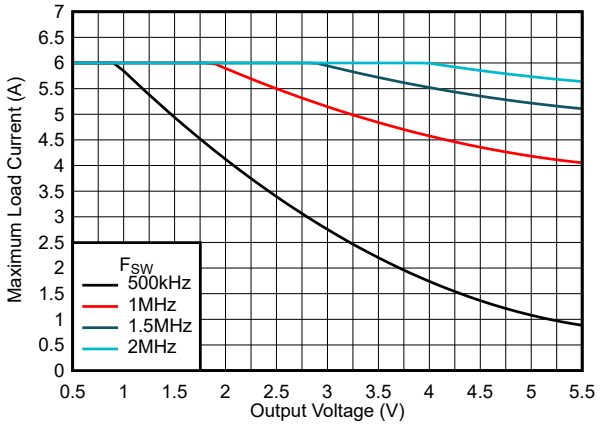


Figure 4-1. Ideal Maximum Load Current Due to HS Current Limit Only (V_{IN} = 12 V, L = 470 nH)

There are additional factors that impact maximum load current due to current limits. Real inductors will have a tolerance around their nominal inductance values, as well as saturation effects that reduce the effective inductance with applied current. Reducing the 470-nH nominal value by 30% to 325 nH to account for these non-idealities results in higher ripple currents and lowers the maximum load current as shown in Figure 4-2. In addition, considering the tolerance on the internal oscillator, the switching frequency may be lower by 10% which further increases the ripple current and lowers the maximum load current as shown in Figure 4-3.

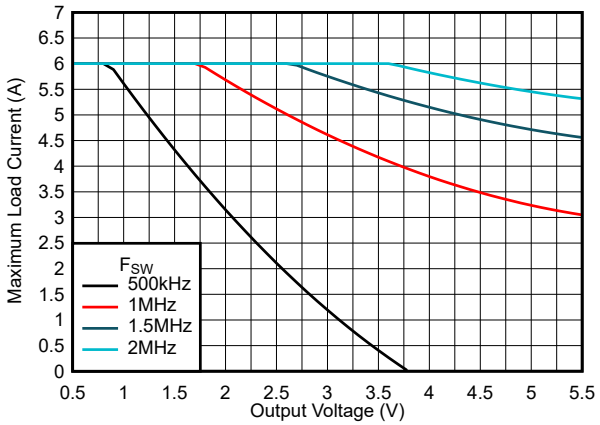


Figure 4-2. Maximum Load Current Due to HS Current Limit Only (V_{IN} = 12 V, L = 325 nH (70% of Nominal))

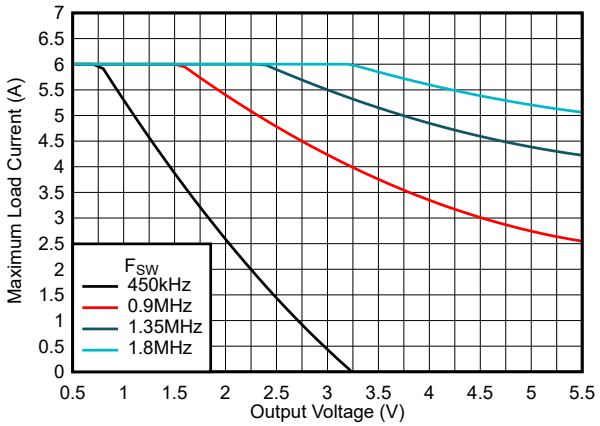


Figure 4-3. Maximum Load Current Due to HS Current Limit Only (V_{IN} = 12 V, L = 325 nH, -10% F_{SW})

Most modern synchronous buck converters and modules also have a negative current limit or sinking current limit, $I_{SINK,OC}$. Under no load conditions, the inductor valley current will go negative for devices such as the TPSM5D1806 that operate in forced continuous-conduction mode (FCCM). If too low a switching frequency is used, the steady state inductor current ripple at no load could be large enough that the valley current could exceed the sinking current limit. Thus, a minimum switching frequency is imposed by the sinking current limit. The margin from the sinking current limit is given by Equation 8 and plotted in Figure 4-4 for V_{IN} = 12 V. For a target output voltage, the switching frequency must be selected where there is positive margin from the sinking current limit.

$$I_{SINK,MARGIN} = I_{SINK,OC} - \frac{I_{PP}}{2} \tag{8}$$

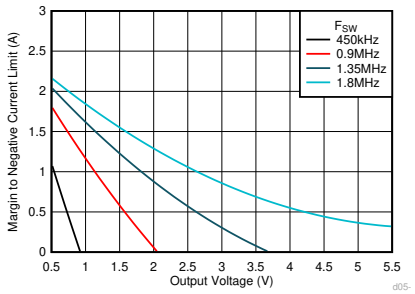


Figure 4-4. Negative Current Limit Margin (V_{IN} = 12 V)

The tradeoff of going to higher switching frequency to avoid current limit violations is typically lower efficiency. The TPSM5D1806 data sheet shows the efficiency curves for 12-V input and 1.8-V output at multiple switching frequencies. The 1.8-V efficiency curves for 1 MHz and 1.5 MHz differ at load currents below 3 A, with the 1.5-MHz curve showing lower efficiency owing to higher switching or AC losses than at 1-MHz.

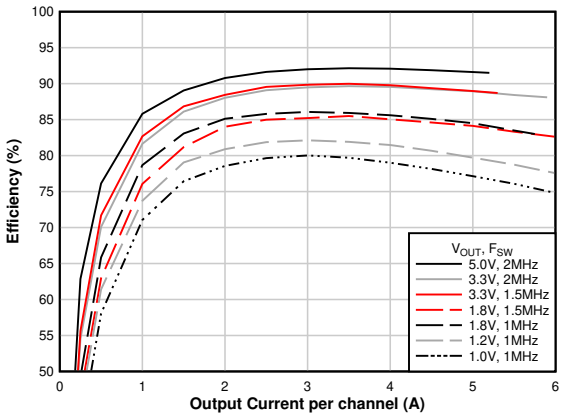


Figure 4-5. TPSM5D1806 Efficiency vs Output Current (V_{IN} = 12 V)

5 TPSM5D1806 Dual-Output Frequency Considerations

The frequency limitations due to minimum on-time, minimum off-time, and current limits all contribute to the operating boundaries summarized in Table 1-1. The same information is also displayed in graph form for Vin = 12 V in Figure 5-1.

The two channels of the TPSM5D1806 operate at the same selected frequency and 180° out of phase from one another in both dual-output and dual-phase operating modes. In dual-output mode, it is necessary to choose a common frequency at which the voltage and load current requirements of the two outputs can be simultaneously met.

Using Figure 5-1, the valid switching frequency options can be determined by finding the frequency curve(s) under which the two outputs' voltage / current points reside. For example, for an application with V_{IN} = 12 V and outputs of 1.8V at 6 A and 3.3V at 5A, either the 1.5-MHz or 2-MHz frequency settings can be used. As the figure also shows, not all combinations of output voltages and load currents may be combined in one TPSM5D1806. For example, there is no valid frequency to support V_{IN} = 12V and outputs of 0.9 V at 6 A and 3.3 V at 6 A within one TPSM5D1806. While the 2-MHz setting would support the 3.3 V rail, the 0.9-V rail would violate minimum on-time with V_{IN} = 12 V. Thus, some consideration has to be made when architecting the power tree for best utilization of the dual-output module channels.

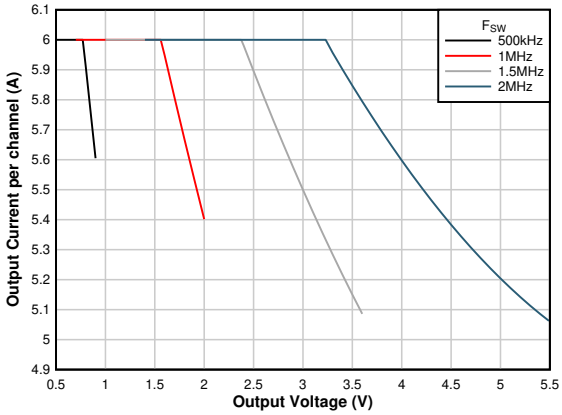


Figure 5-1. TPSM5D1806 Maximum Output Current (V_{IN} = 12 V)

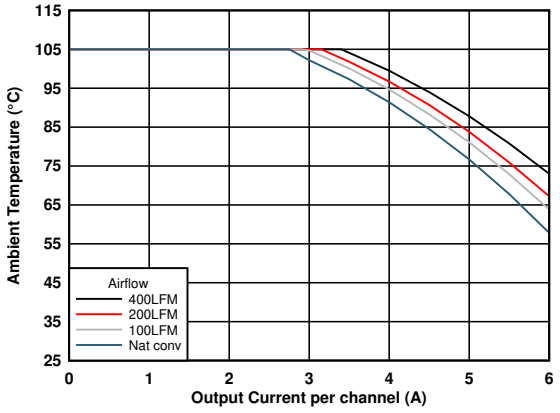
6 Thermal Performance

In addition to the timing and current limits, thermal performance is another key factor to consider for safe module operation. A buck power module integrates the main power dissipating elements in a switch mode power supply – the power switches and magnetics – all into one package.

TI power module datasheets provide Safe Operating Area (SOA) curves such as shown in Figure 6-1. These curves show the maximum allowed ambient temperature versus load current, as an aid to quantifying the thermal capabilities of a given device. Module SOA measurements are typically performed on the module EVM. For the TPSM5D1806, it is important to note that the SOA curves are exercising the module with both channels enabled and set to the same output voltage, and both channels loaded (for example, IOUT1 = IOUT2). This means that the SOA curves can also be used to gauge the thermal performance in dual-phase operation where both TPSM5D1806 channels are tied together to deliver up to 12 A of output current. The x-axis of Figure 6-1 can simply be doubled to get the effective SOA chart for the equivalent dual-phase condition.

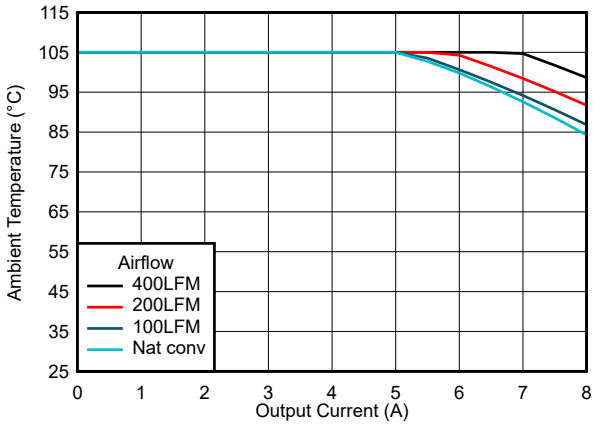
One might assume that the bigger the module, the more output power and current it can deliver due to thermal limitations. That may not always be the case, and it is worthwhile to look at different modules' SOA curves to compare their current derating versus ambient temperature. For example, Figure 6-1 indicates that the TPSM5D1806 in dual-phase configuration can deliver up to 8-A (4-A per channel) with V_{IN} = 12 V and V_{OUT} = 1.8 V at ambient temperatures of up to 90°C with no airflow. Meanwhile, Figure 6-2 indicates that the larger single-output TPSM84824 can deliver 8-A at only up to 85°C for the same condition. The TPSM5D1806 comes in a 5.5 x 8 x 1.8 mm (79.2 mm^3) QFN package, which is smaller than the TPSM84824 which comes in a 7.5 x 7.5 x 5.3 mm (298 mm^3) open frame QFN package.

A caveat to this comparison is that the TPSM84824 SOA measurements were taken on a 4-layer board whereas the TPSM5D1806 SOA was taken on the 6-layer TPSM5D1806EVM. Thermal performance depends on the PCB layout, so the data sheet SOA curves should not be interpreted to represent the module's thermal capability in any and every layout; it is only meant as a guideline of what performance is possible with a layout and stackup similar to the EVM. Estimating that the TPSM84824 dissipates ~1.9W at this condition and would run ~2°C/W cooler on a 6-layer board versus a 4-layer board (6), the estimated max ambient temperature allowed for the TPSM84824 can be adjusted to approximately 89°C. Even after this adjustment, the smaller TPSM5D1806 offers comparable output capability despite its smaller package.



F_{SW} = 1.5 MHz, Dual 1.8-V Outputs, IOUT1 = IOUT2

Figure 6-1. TPSM5D1806 Thermal Safe Operating Area (V_{IN} = 12 V, V_{OUT} = 1.8 V)



F_{SW} = 600 kHz, V_{OUT} = 1.8 V

Figure 6-2. TPSM84824 Thermal Safe Operating Area (V_{IN} = 12 V, V_{OUT} = 1.8 V)

7 Summary

Buck power modules provide many benefits to system engineers, from small solution size to faster time to market. TI power modules are designed to be versatile and cover a wide application space, however, all power modules have operational limits. This application report has highlighted the timing, current limit, and thermal considerations that typically set boundaries to the valid operating area of a module. With this knowledge, a system engineer can better make the design tradeoffs when selecting, comparing, and designing with buck power modules.

8 References

The following materials are available on TI.com:

1. Texas Instruments, Bang for your Buck - An Intro to Buck Converter vs. Buck Power Module Comparison, application report.
2. Texas Instruments, Real Benefits of Using a Power Module vs. Discrete, training.
3. Texas Instruments, Understanding Buck Power Stages in Switchmode Power Supplies, application report.
4. Texas Instruments, Introduction to Buck Converters: Minimum On-time and Minimum Off-time Operation, training.
5. Texas Instruments, Know Your Limits, application report.
6. Texas Instruments, Practical Thermal Design With DC/DC Power Modules, application report.

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