User's Guide

TPSM8286xAA0SEVM Evaluation Module

TEXAS INSTRUMENTS

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1 TPSM8286xAA0SEVM Evaluation Modules

The TPSM8286xAA0SEVM facilitates the evaluation of the TPSM82864AA0SRDJR and TPSM82866AA0SRDJR 4-A and 6-A pin-to-pin compatible step-down power modules with DCS-Control in a 3.5-mm × 4-mm x 1.4-mm overmolded QFN package. The EVMs provide a 1.2-V output voltage with 1% accuracy for input voltages from 2.4 V to 5.5 V. The TPSM82864AA0SRDJR and TPSM82866AA0SRDJR are high-efficiency, small, and ultra-thin solutions for the following:

- Point-of-load (POL) power in applications such as the core supply for FPGAs, CPUs, and ASICs
- Optical modules
- Medical imaging
- Industrial transport
- Solid state drives (SSDs)
- Other space-limited applications

2 Introduction

The TPSM82864AA0SRDJR and TPSM82864AA0SRDJR are synchronous, step-down converter power modules in a small 3.5-mm × 4-mm overmolded QFN package with 1.4-mm height. The two devices in this family support 4-A or 6-A output currents.

2.1 Performance Specification

Table 2-1 provides a summary of the TPSM8286xAA0SEVM performance specifications.

Table 2-1. Performance Specification Summary

SPECIFICATION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage		2.4	5	5.5	V
Output voltage setpoint			1.2		V
Output current	TPSM82864AA0SEVM (BSR182-002)	0		4	A
	TPSM82866AA0SEVM (BSR182-001)	0		6	A

2.2 Modifications

The printed-circuit board (PCB) for this EVM is designed to accommodate some modifications by the user. Additional input and output capacitors or a feedforward capacitor can be added. Also, the MODE setting and output voltage setting configuration can be changed. Finally, the loop response can be measured.

2.2.1 Input and Output Capacitors

C9, shown in Figure 7-1, is provided for an additional input capacitor. This capacitor is not required for proper operation, but can be used to reduce the input voltage ripple.

C5, C6, C7, and C8 are provided for additional output capacitors. These capacitors are not required for proper operation but can be used to reduce the output voltage ripple and to improve the load transient response. The total output capacitance must remain within the recommended range in the data sheet for proper operation.

2.2.2 Feedforward Capacitor

C4 is provided as an optional feedforward capacitor (C_{FF}).

2.2.3 VSET/MODE Resistor

R4 selects the MODE setting (PSM or FPWM) and output voltage setting configuration. When using the VSET configuration for setting the output voltage, short R1 and remove R2. See the *TPSM8286x 4-A and 6-A High Efficiency Step-Down Converter QFN Power Module Data Sheet* for details of the various settings.

2.2.4 Loop Response Measurement

The loop response can be measured with simple changes to the circuitry. First, install a 10-Ω resistor across the pads of R6 on the back of the PCB. The pads are spaced to allow installation of an 0603-sized resistor. Next, cut the short section of trace on the top layer between the via near R1 and the V_{OUT} plane. Figure 2-1 shows this

change. With these changes, an AC signal (10-mV, peak-to-peak amplitude recommended) can be injected into the control loop across the added 10-Ω resistor. Figure 5-2 shows the results of this test.

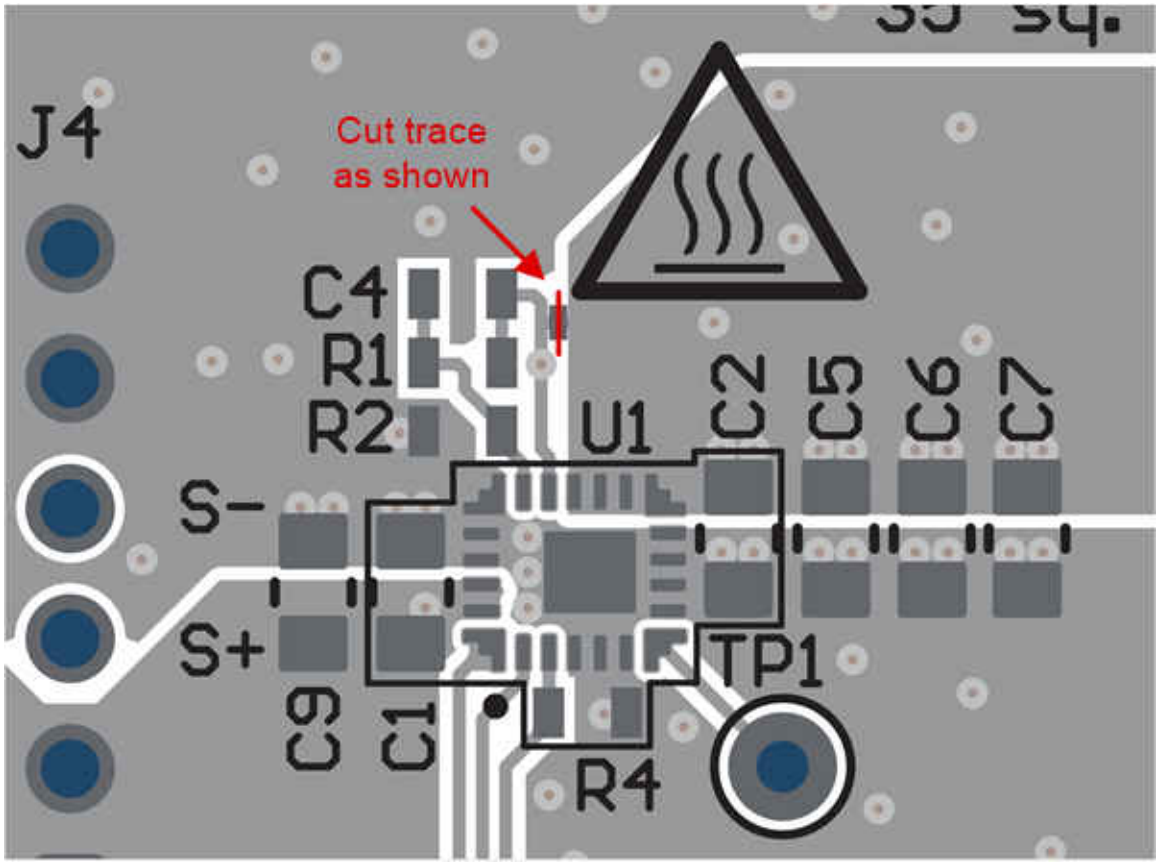

Figure 2-1. Loop Response Measurement Modification

3 Setup

This section describes how to properly use the TPSM8286xAA0SEVM.

3.1 Setup

To operate the EVM, set jumper JP1 between ON and EN to turn on the device as shown in Section 3.2. Connect the input supply to J1 and connect the load to J2.

3.2 Input/Output Connector and Jumper Descriptions

J1 – VIN/GND	Input and return connections from the input supply for the EVM. This connector supports currents over 3 A and accepts up to 16 AWG wire.
J2 – VOUT/GND	Input and return connections from the EVM to the load. This connector supports currents over 3 A and accepts up to 16 AWG wire.
J3 – PG/GND	The PG output appears on pin 2 of this header with ground on pin 1.
J4, Pin 1 and 2 – VIN	Positive input connection from the input supply for the EVM Do not use for currents above 3 A.
J4, Pin 3 and 4 – S+/S–	Input voltage sense connections. Measure the input voltage at this point.
J4, Pin 5 and 6 – GND	Input return connection from the input supply for the EVM. Do not use for currents above 3 A.
J5, Pin 1 and 2 – VOUT	Output voltage connection Do not use for currents above 3 A.
J5, Pin 3 and 4 – S+/S–	Output voltage sense connections. Measure the output voltage at this point.
J5, Pin 5 and 6 – GND	Output return connection Do not use for currents above 3 A.
JP1 – EN	EN pin input jumper. Place the supplied jumper across ON and EN to turn on the module. Place the jumper across OFF and EN to turn off the module.
JP2 – PG Pullup Voltage	PG pin pullup voltage jumper. Place the supplied jumper on JP2 to connect the PG pin pullup resistor to VOUT. Alternatively, the jumper can be removed and a different voltage can be supplied on pin 1 to pull up the PG pin to a different level. This externally applied voltage must remain below 6 V.
JP3 – VSET/MODE	VSET/MODE pin input jumper. Place the supplied jumper across PWM and VSET/MODE to operate the IC in Forced PWM mode. Place the jumper across PFM/PWM and VSET/MODE to operate the IC in Auto PFM/PWM mode. Remove the jumper to operate the IC with a fixed output voltage, which is set by R4. For the fixed output voltage configuration, R4 needs to be installed, R2 removed, and R1 shorted.

4 Safety Instructions

WARNING

Hot surface. Contact may cause burns. Do not touch.

WARNING

High currents may be present on the input and output. Use connectors J1 and J2 if the current exceeds 3 A.

5 Test Results

The TPSM8286xAA0SEVM was used to take all the data in the *TPSM8286x 4-A and 6-A High Efficiency Step-Down Converter QFN Power Module Data Sheet*. See the device data sheet for the performance of this EVM.

Figure 5-1 shows the thermal performance of the EVM. Figure 5-2 shows the loop response measurement.

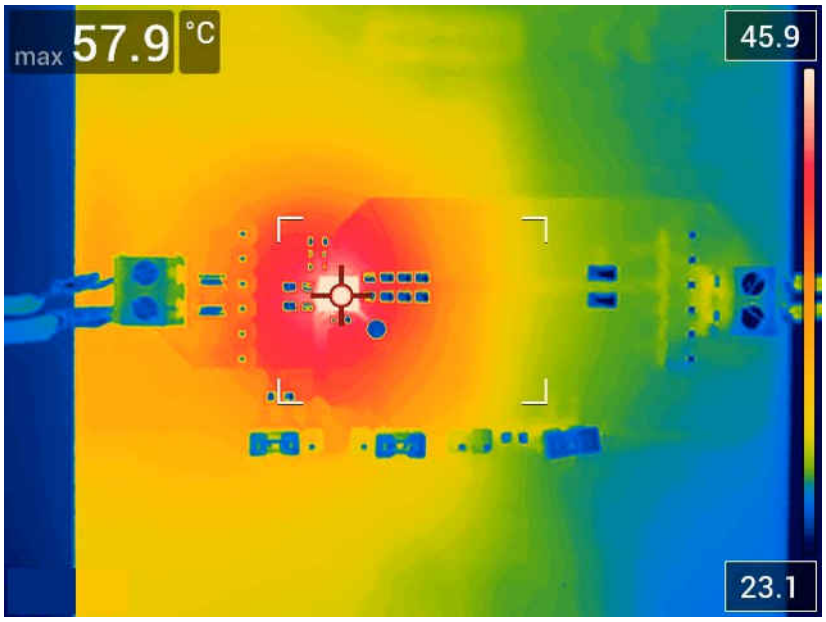

Figure 5-1. Thermal Performance (V_{IN} = 5 V, V_{OUT} = 1.2 V, I_{OUT} = 6 A)

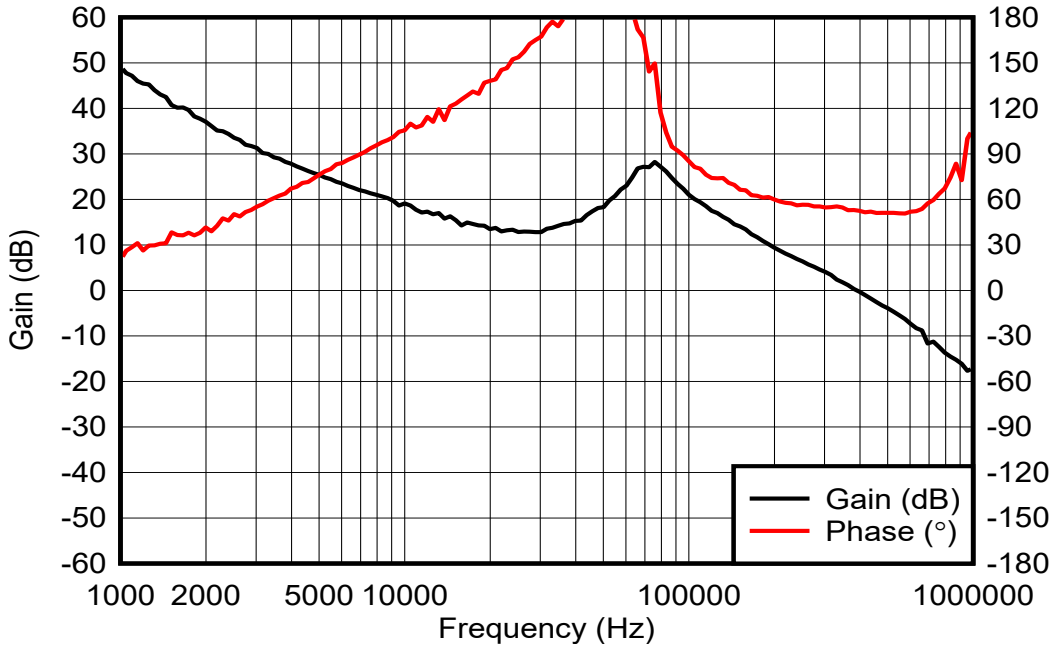

Figure 5-2. Loop Response Measurement (V_{IN} = 5 V, V_{OUT} = 1.2 V, I_{OUT} = 6 A)

6 Board Layout

This section provides the TPSM8286xAA0SEVM board layout and illustrations in Figure 6-1 through Figure 6-6. The Gerbers are available on the TPSM82866AA0SEVM tool folder. All four layers use 2-ounce copper.

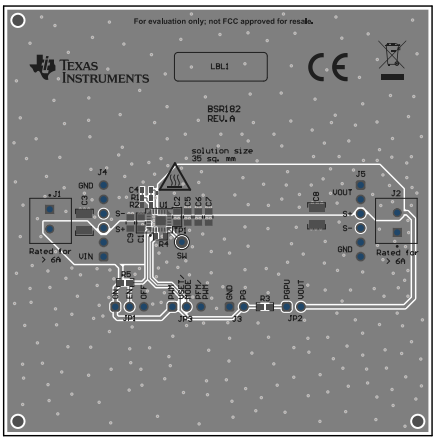

Figure 6-1. Top Assembly

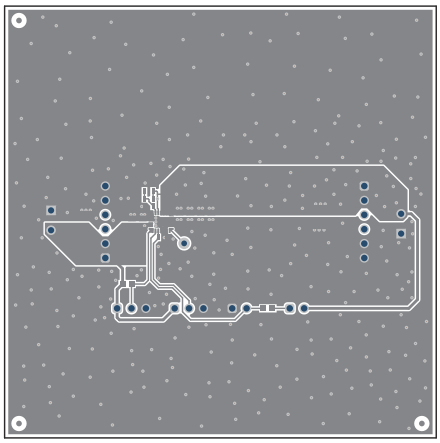

Figure 6-2. Top Layer

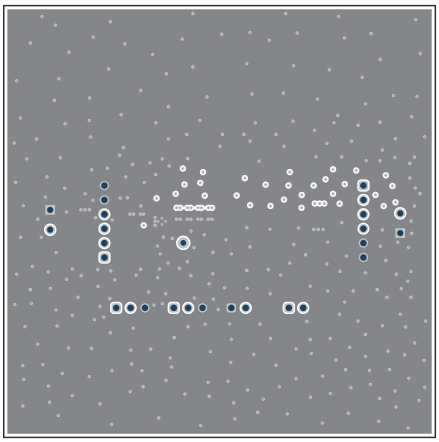

Figure 6-3. Internal Layer 1

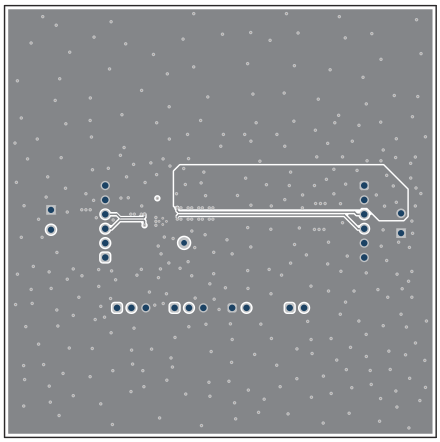

Figure 6-4. Internal Layer 2

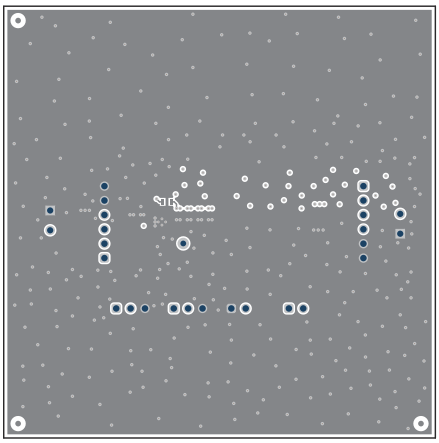

Figure 6-5. Bottom Layer

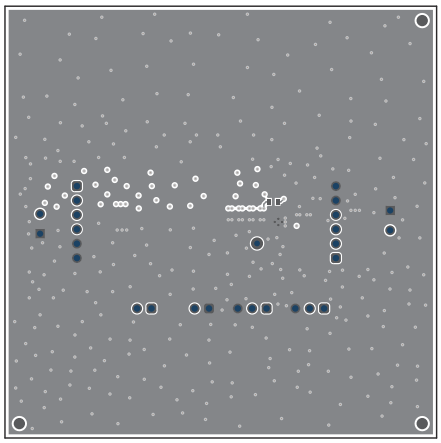

Figure 6-6. Bottom Layer (Mirrored)

7 Schematic and Bill of Materials

This section provides the TPSM8286xAA0SEVM schematic and bill of materials (BOM).

7.1 Schematic

Figure 7-1 illustrates the EVM schematic. The TPSM82864AA0SEVM uses the TPSM82864AA0SRDJR IC and the TPSM82866AA0SEVM uses the TPSM82866AA0SRDJR IC.

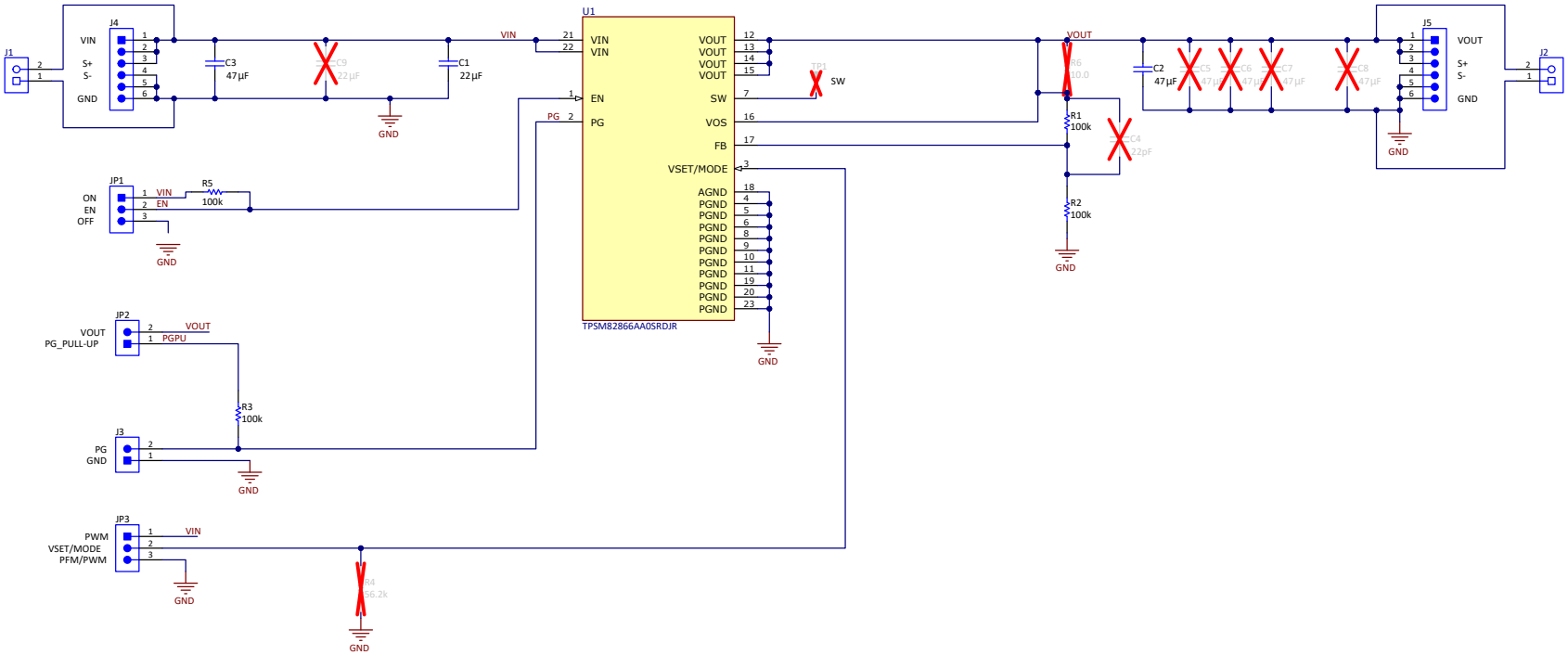

Figure 7-1. TPSM8286xAA0SEVM Schematic

7.2 Bill of Materials

Table 7-1 lists the BOM for this EVM.

Table 7-1. TPSM8286xAA0SEVM Bill of Materials

COUNT		DESIGNATOR	VALUE	DESCRIPTION	SIZE	PART NUMBER	MANUFACTURER
-001	-002						
1	1	C1	22 µF	CAP, CERM, 6.3 V, ±20%, X7R	0805	GRM21BZ70J226ME44L	Murata
1	1	C2	47 µF	CAP, CERM, 6.3 V, ±20%, X6S	0805	JMK212BC6476MG-T	Taiyo Yuden
1	1	C3	47 µF	CAP, CERM, 10 V, ±20%, X7R	1210	LMK325B7476MM-PR	Taiyo Yuden
4	4	R1, R2, R3, R5	100 kΩ	RES, 100 kΩ, 1%, 0.1 W	0603	Std	Std
1	0	U1			3.5 × 4 mm	TPSM82866AA0SRDJR	Texas Instruments
0	1	U1			3.5 × 4 mm	TPSM82864AA0SRDJR	Texas Instruments

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