

# Minimizing TRF7964A and TRF7970A Current Use During Power-Down Mode

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MCU Safety and Security Applications

## ABSTRACT

NFC/RFID applications that are battery powered, such as digital door locks or portable terminals, need to conserve as much power as possible in sleep mode to extend battery life. Because the TRF7964A or TRF7970A NFC/RFID transceiver generally spends a majority of its time in power-down mode in these applications, optimizing current consumption while in this mode is very important.

This application report provides recommendations on circuit and firmware design to reduce current consumption in power-down mode for the TRF7970A and TRF7964A devices. Various designs are considered, and they are analyzed based on their current consumption. This application report is particularly targeted for dual-voltage systems that are powered by battery and where in power-down mode EN2 is needed to be high.

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## 1 Introduction

The key points that are addressed in this application report focus on obtaining the best power performance. The examples included in this report use the MSP430F2370 and the TRF7964A. There should not be any significant changes for the TRF7970A.

The bus communication between the MCU and the TRF7964A or TRF7970A is SPI with Slave Select (SS) in this document. The parallel bus interface is not analyzed.

## 2 Current Design Analysis

The [TRF7970A EVM](#) has the I/O\_1 and I/O\_2 pins pulled high with a 10-k $\Omega$  resistor on each pin, selecting the SPI with SS mode (along with I/O\_0 being connected to ground (GND) These pullups are sourced from the VDD\_X supply. VDD\_X supply is not powered when EN = 0. Thus, these two I/O pins slowly turn off as the VDD\_X power decays. Refer to the TRF7970A EVM schematic in [Section 5](#) for details.

When putting the TRF7964A or TRF7970A into power-down mode, as long as Slave Select (SS) and MOSI are driven low immediately, the resulting configuration is current efficient while in sleep mode (the MSP430™ MCU and the TRF7964A or TRF7970A devices consume less than 1  $\mu$ A).

However, there are systems where the MCU and TRF7964A or TRF7970A are supplied by different voltage sources. For example, in a battery-powered system, the TRF7964A or TRF7970A may be powered by 3.3 V and the MCU by 2.8 V. This configuration requires a different design for the system to operate with low power, because the lower power rail would always be on, even when EN = 0.

## 3 Low-Voltage MCU System

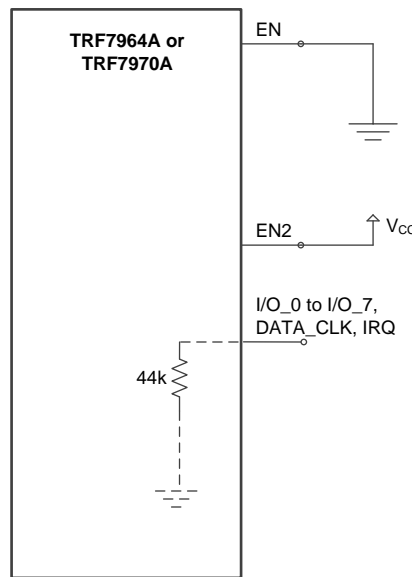
When the MCU is running at a different voltage than the TRF7964A or TRF7970A, generally this means that VDD\_X must be decoupled from the VDD\_I/O pin. This is necessary because VDD\_X sources up to 3.4 V when EN = 1. Because the MCU in this example is a low-voltage powered one, (in this case 2.8 V), this can exceed the absolute maximum voltage allowed by the MCU on the GPIOs that are being driven by the TRF7964A or TRF7970A device (MISO, IRQ).

This VDD\_X voltage can be changed to a compatible voltage for the MCU by configuring the Regulator and I/O Control Register (TRF7964A or TRF7970A register 0x08). However, during the initial configuration, the MCU is exposed to the higher voltage. If the MCU can tolerate the higher voltage, then the current EVM design can be used with its low sleep currents, in this multiple power source scenario.

### 3.1 Pulldown Resistors

44-k $\Omega$  pulldowns on the TRF7964A or TRF7970A I/O pins are activated in two modes:

1. When EN = 0 and EN2 = 1. This mode is mainly used to continue to output a clock from the TRF7964A or TRF7970A for running an MCU when TRF7964A or TRF7970A operation is not needed.
2. When EN2 = 0 and there is a transition of EN = 1 to EN = 0. These pulldown resistors are activated until the VDD\_A rail falls below approximately 1 V. This transition time is 0.8 to 0.9 seconds. After this time, the pulldown resistors are deactivated and the I/Os are high-impedance. I/O\_0 to I/O\_7, DATA\_CLK, and IRQ are high-impedance after the VDD\_A rail has discharged.



**Figure 1. TRF7964A or TRF7970A I/O Impedance During EN = 0**

### 3.2 Possible Nonideal Multiple Power Source Design

Figure 2 shows a design that draws extra current when in power-down mode (PDM) as compared to the previous example. The reason is that the TRF7964A or TRF7970A I/Os are pulled down by 44-k $\Omega$  resistors internally when the device enters PDM (EN = 0, EN2 = 1) see Figure 1). Because I/O\_1 and I/O\_2 are connected to a constantly driven power rail in this example, there is current drawn from the power-rail through these pulldown resistors.

Therefore, it is important to make sure that these I/Os are high-impedance or are driven to ground to achieve the lowest current consumption possible.

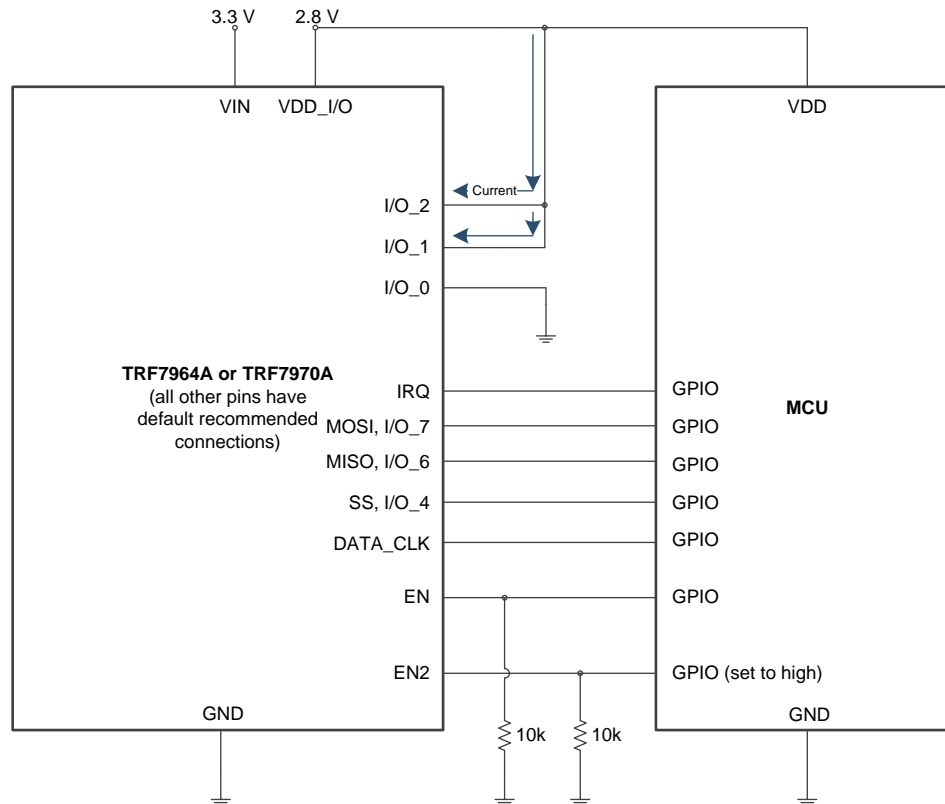


Figure 2. TRF7964A or TRF7970A I/O\_1 and I/O\_2 Connected to a Power Supply

### 3.3 Slave Select (SS) Pulled-Up Design

When slave select (SS) is pulled high (see Figure 3), there is a certain disadvantage. With SS pulled high, when EN = 0 and EN2 = 1, there is current through the SS pullup through the internal pulldowns on the TRF7964A or TRF7970A.

As long as the EN and EN2 pins are pulled low, the SS pullup should not be required. If SS is high when EN goes high, the TRF7964A or TRF7970A can power up safely.

If the SS pullup design is used, it is recommended to have the MCU drive the SS line low, instead of to high impedance, to prevent extra current being lost (see Figure 4).

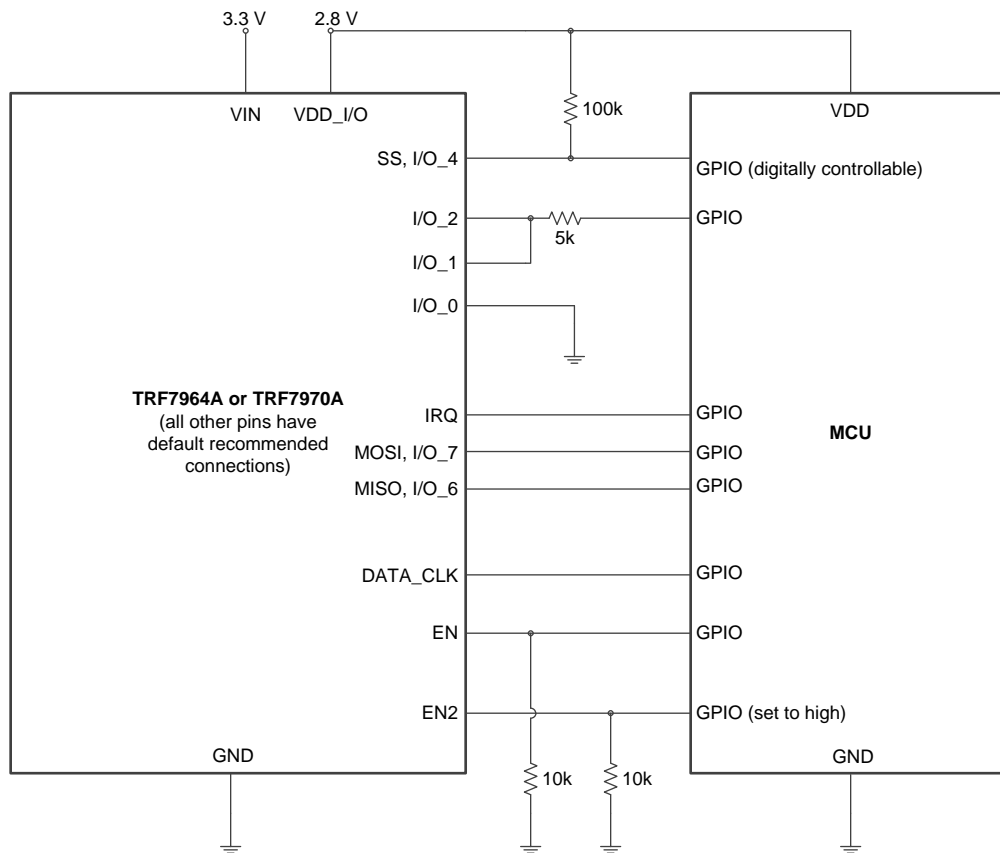
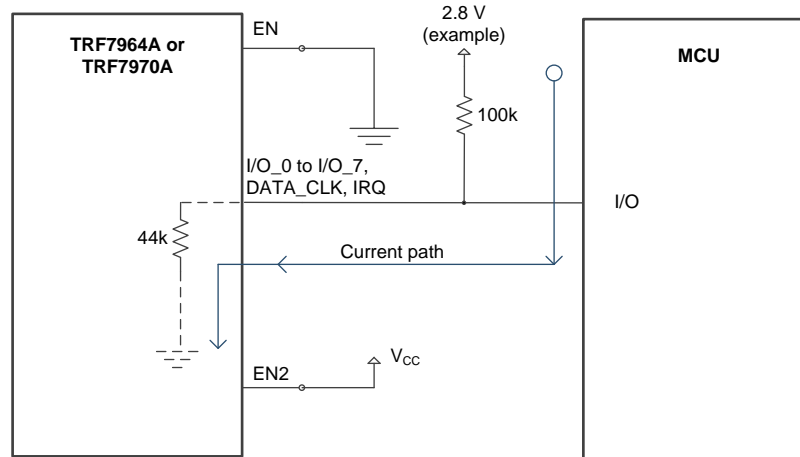


Figure 3. Slave Select Pulled High



**Figure 4. Example Case of Nondigital Voltage on MCU I/O**

### 3.4 TRF7964A or TRF7970A Sharing the SPI Bus

There are some considerations needed if it is desired for the TRF7964A or TRF7970A to share a SPI bus.

1. EN = 0 and EN2 = 1: In this mode, the pulldown resistor is continually active. Therefore, some power is lost on the SPI bus.
2. EN = 0 and EN2 = 0: In this mode, the pulldown resistors are active for almost a second. Waiting until the pulldown resistors are deactivated is generally not a viable option when the time is approximately a second, so this mode is very similar to the first one.

It is possible for the TRF7964A or TRF7970A to share the SPI bus with another device. The TRF7964A or TRF7970A must be disabled (EN = 0) when the communication with the other device occurs. Because each of the I/O lines on the TRF7964A or TRF7970A is pulled low when EN = Low, the system incurs extra current on every high level of the MOSI, MISO, and DATA\_CLK signals. The current loss per pin is:

$$\text{Current Loss} = \text{MCU Voltage} / 44 \text{ k}\Omega$$

$$\text{For example: } 2.8 \text{ V} / 44 \text{ k}\Omega = 64 \mu\text{A}$$

This is for a high level on a single line. When the SPI signal is low, no extra current is consumed.

### 3.5 Recommended Multiple Power Source Design

In [Figure 5](#), VDD\_I/O can be powered constantly with no extra current loss in total power-down mode.

The reason it is recommended to have the I/O pins connected to an MCU is that they can be set low when the TRF7964A or TRF7970A EN = Low. This conserves current.

Also having control over EN2 is essential to a proper power up (for the TRF7964A or TRF7970A). See the [TRF7964A data sheet](#) or the [TRF7970A data sheet](#) for more information.

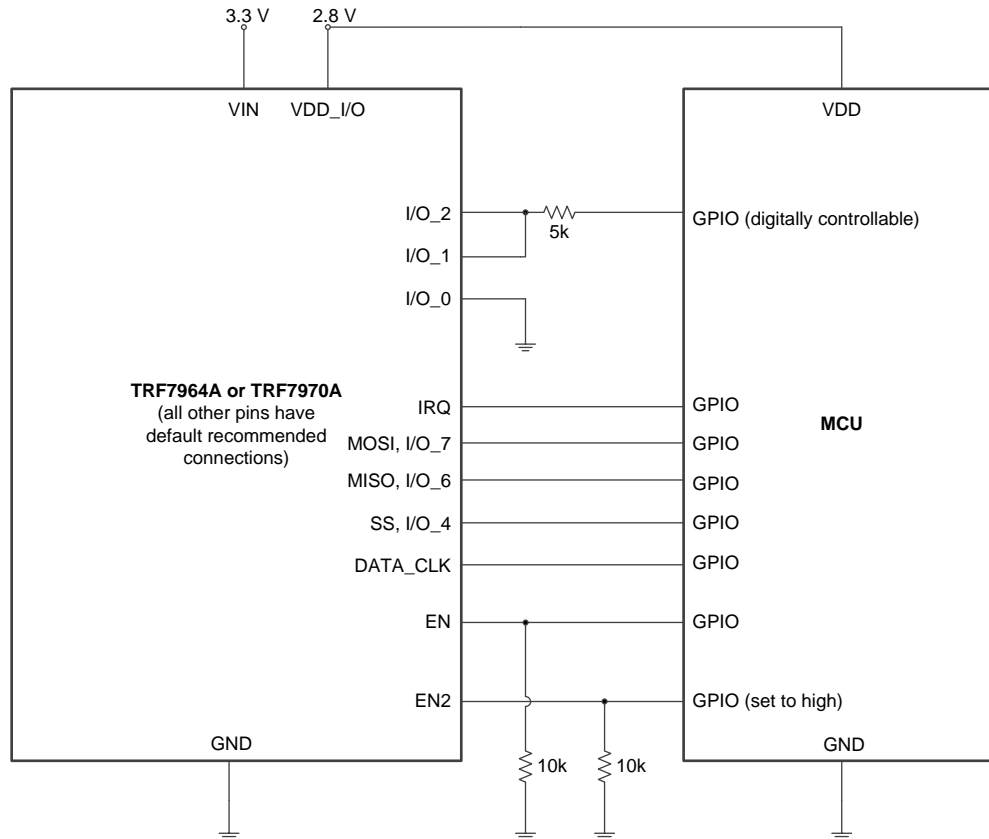


Figure 5. Recommended Design

### 3.6 Recommended Voltage Levels in Power-Down Mode (EN = Low and EN2 = High)

Table 1 shows the recommended settings for the TRF7964A or TRF7970A I/O bus.

**Table 1. Suggested States of TRF7964A or TRF7970A I/O Bus During Power-Down Mode**

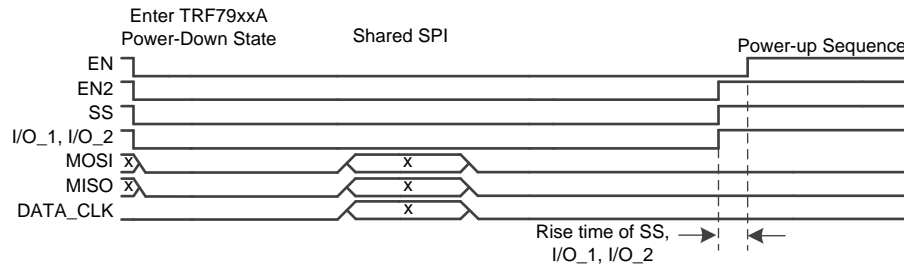
I/O Pin	State	Notes
MISO, MOSI (I/O_6, I/O_7)	Low or Hi-Z <sup>(1)</sup>	
DATA_CLK	Low or Hi-Z <sup>(1)</sup>	
SS (I/O_4)	Low or Hi-Z <sup>(1)</sup>	Hi-Z may draw extra current with a pullup resistor
I/O_0, I/O_1, I/O_2	Low or Hi-Z <sup>(1)</sup>	

<sup>(1)</sup> There are no current differences between having the I/O bus driven low or set to high-impedance, except in the case with SS pulled high.

### 3.7 Timings Section

Bus sharing during TRF7964A or TRF7970A power-down state causes a slight increase in current due to the 44-kΩ pulldown resistors active on the bus.

For the power-up sequence, SS must be high before the EN signal is set high (see Figure 6). When EN2 is high and EN0 is low, the pulldown resistors are activated. However, in the same case, when EN2 is low, the pulldown resistors are active for approximately one second, until the voltage decays on VDD\_A. During this time, current is drawn from any high-level signals on I/O\_0 to I/O 7, DATA\_CLK, and IRQ.



**Figure 6. Sleep and Wake Timings**

### 3.8 Power Measurements

Table 2 summarizes an example case in which the TRF7964A or TRF7970A is powered by 3.3 V and the MCU is powered by 2.8 V. The pullup that is used in this example is 100 kΩ.

In Table 2, the state and current measurements are after EN and EN2 are low.

**Table 2. System Current Consumption**

VDD_I/O During Power Down (V)	SS Pullup	SS Drive	MOSI, MISO, DATA_CLK	I/O_0, I/O_1, I/O_2	TRF7964A or TRF7970A 3.3-V Rail Current (μA)	MSP430 MCU 2.8-V Rail Current (μA)	Additional Information
2.8	No pullup	Low	Low	All Low	<1	<1	Section 3.5
Hi-Z	No pullup	Low	Low	All Low	<1	<1	Section 3.5
2.8	100 kΩ to 2.8 V	Low	Low	All Low	<1	29	Section 3.3
2.8	100 kΩ to 2.8 V	Hi-Z	Low	All Low	<1	26 <sup>(1)</sup>	Figure 4
2.8	100 kΩ to 2.8 V	High	Low	I/O_1 and I/O_2 pulled high by 10 kΩ to 2.8 V	<1	166	Section 3.2 (partially)

<sup>(1)</sup> Care must be taken before deciding to set this pin to Hi-Z when an SS pullup is used, because an intermediate external voltage level that can cause extra current leakage by the input circuitry (see Figure 4).



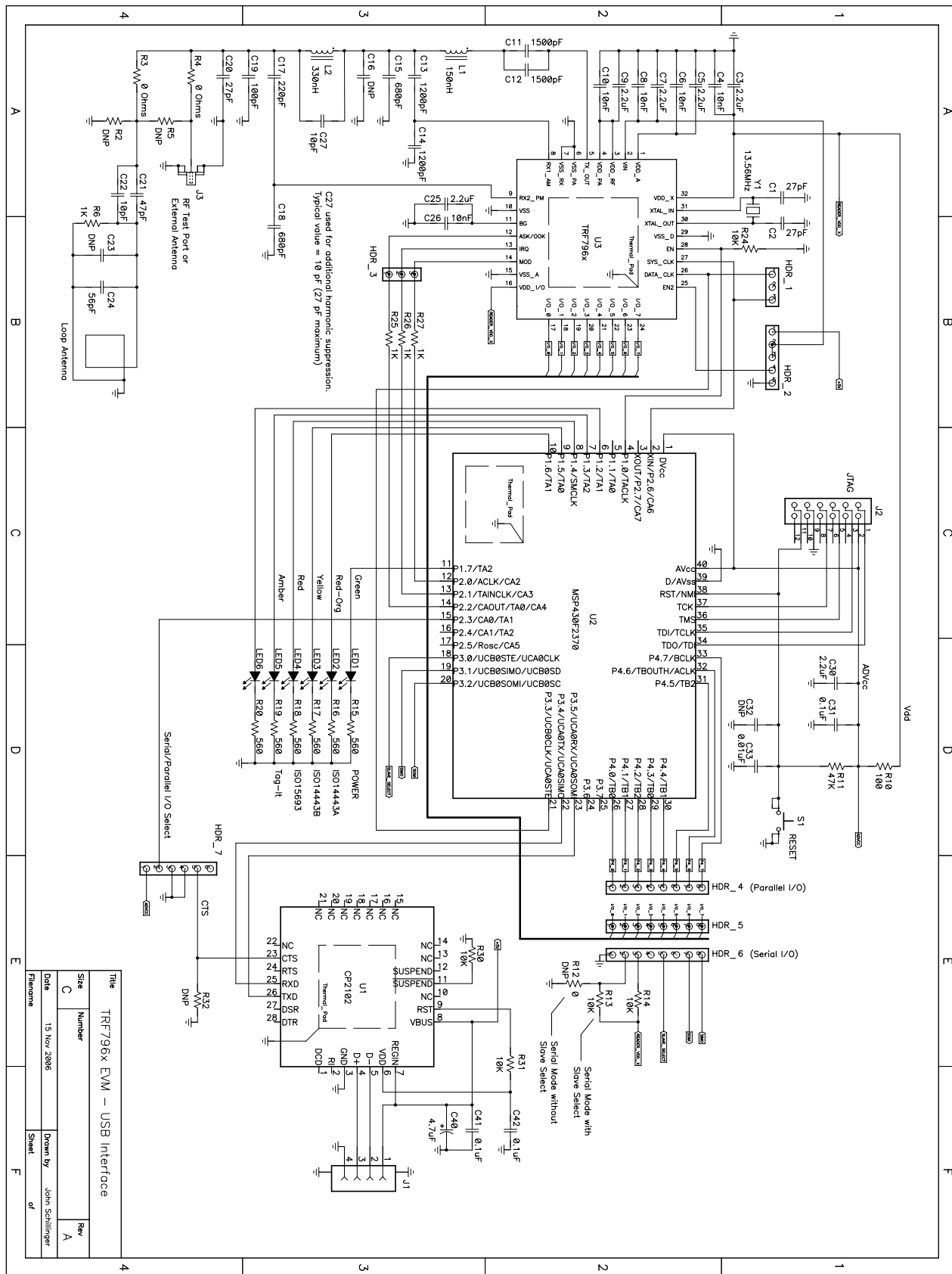
#### 4 Conclusion

This application report describes the key features that are important to minimize TRF7964A or TRF7970A current consumption in power-down mode.

Without careful attention to the design, power could be lost in power-down mode when designing with the TRF7964A or TRF7970A. With these simple considerations, this problem can be fixed.

#### 5 Schematics

[Figure 7](#) shows the reference to use to analyze the current setup. This schematic is nearly the same as the TRF7970A EVM.



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Figure 7. Schematic

## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from August 14, 2015 to June 28, 2017</b>	<b>Page</b>
• Changed the title of this application report (changed "TRF797xx" to "TRF7970A and TRF7964A") .....	1
• Throughout document, removed references to TRF79xx devices other than TRF7970A and TRF7964A (this document applies to only these two devices) .....	1
• Changed references as TRF79xxA to TRF7964A or TRF7970A through the document. ....	2
• Added <a href="#">Section 3.1, Pulldown Resistors</a> .....	3
• Updated <a href="#">Figure 2, TRF7964A or TRF7970A I/O_1 and I/O_2 Connected to a Power Supply</a> .....	4
• Updated <a href="#">Figure 3, Slave Select Pulled High</a> .....	5
• Updated <a href="#">Figure 4, Example Case of Nondigital Voltage on MCU I/O</a> .....	6
• Updated <a href="#">Section 3.4, TRF7964A or TRF7970A Sharing the SPI Bus</a> .....	6
• Updated <a href="#">Figure 5, Recommended Design</a> .....	7
• Updated <a href="#">Figure 6, Sleep and Wake Timings</a> .....	8

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