Application Report
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TRF7970A Firmware Design Hints

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ABSTRACT

This application report is a reference for the firmware developer using TRF7970A in conjunction with a microcontroller (for example, an MSP430™ MCU or ARM®-based MCU).

Contents

List of Figures

List of Tables

TRF7960, TRF7961, TRF7960A, TRF7970A Firmware Hints

Table 1 lists the firmware design hints that are described in this application report.

Table 1. Firmware Hints Reference

Item		TRF7970A	TRF7960A	TRF7960	TRF7961
1	ISO15693 only - Direct command (0x14) 'Transmit next slot'			✓	✓
2	Missing IRQ	✓	✓	✓	✓
3	Lost IRQ	✓	✓	✓	✓
4	Wrong data due to "overshoots"			✓	
5	ISO14443A decoder			✓	
6	Tags that do not follow the ISO14443A Layer 4 framing			✓	
7	SPI with SS (see Section 7.5)		✓	✓	✓

1 ISO15693 Only – Direct Command (0x14) EOF/TX Next Slot

Description

Sending of 'Transmit next slot' direct command (0x14) can happen only once (ISO15693).

Workaround

Before sending the 'Transmit next slot' direct command, the 'Reset' direct command must be send. This is only used in ISO15693 Inventory command (with 16 time slots). ISO 15693 'Write Single Block' and 'Lock Block' commands are affected also if the 'Option' bit is set.

2 Missing IRQ

Description

The device does not send (on pin 13) any interrupt requests on certain condition. The chip can go to a state in which the sending of additional interrupts during RX or TX is stopped. This happens when the Stop condition is exactly aligned with the byte boundary on TX data.

Workaround

The loading and reading of the FIFO should be coded in such a way, that the Stop condition does not fall directly on the TX byte boundary.

3 Lost IRQ

Description

Lost IRQ if the end of RX IRQ occurs at the same time that the IRQ register is being read (also see Section 6).

Workaround

Add additional checks to retrieve the RX data in case the IRQ is suppressed by a coinciding read operation.

4 Wrong Data Due to Overshoots

Description

The ISO14443A 106-kbps decoder gives wrong data in certain condition. When the analog front end filter overshoots, the digitizer might produce a rising edge on the subcarrier data. If this occurs within a small time-window the decoder will produce false data. This happens extremely rarely and is dependent on the antenna/filter characteristics.

Workaround

Switch to PM channel or adjust gain to avoid overshoots in the analog filter.

5 ISO14443A Decoder

Description

ISO14443A subcarrier decoded incorrectly – "reading holes".

Workaround

Adjust gain setting of main RX channel; repeat reading until correct data results. (This might require additional time.)

6 Tags That Do Not Follow ISO14443A Layer 4 Framing

Description

When a transmit frame starts with the code 0x93, 0x95 or 0x97, the reply will not be correctly framed. This happens because the TRF796x devices have an automatic anticollision broken byte framing system that is activated with the 0x93, 0x95 or 0x97 code.

Workaround

Use TRF7960 "Direct Mode".

7 TRF7960, TRF7961, TRF7960A, TRF7970A SPI With SS Special Handling

7.1 SPI With SS Pin Only – No High Impedance

Description

Serial interface with SS pin only - interface does not go to high impedance when SS is high. It is not possible to multiplex the serial port interface lines.

Workaround

An external 3-state buffer must be used if the chip is connected to a serial bus and the interface lines must be multiplexed.

7.2 SPI With SS Pin Only – Direct Commands

Description

Serial interface with SS pin only - the direct commands are not executed if they are the last operation in the SPI communication. In the SPI interface with SS pin the Stop condition clock pulse is missing (compared to the parallel interface and SPI without SS pin). Some operations are relying on this clock and they do not work as expected.

Workaround

If a direct command is the last operation in the SPI communication, the SS pins goes high. An additional clock pulse must be sent after this happens.

7.3 SPI With SS Pin Only – IRQ Status Bit

Description

Serial interface with SS pin only - IRQ status bits are not cleared after the IRQ Status register (0x0C) is read.

Workaround

A dummy read must be made after reading the 'IRQ status' register (0x0C). This can be done in noncontinuous or continuous mode. In continuous mode only 8 clock pulses are needed. In noncontinuous mode 16 clock pulses are needed: 8 for address and 8 for data.

7.4 SPI With SS Pin Only – No TX if Single Bit in FIFO

Description

Serial interface with SS pin only - the chip does not start with transmission if only 1 byte is loaded to the FIFO.

Workaround

The microcontroller has to load an additional byte to the FIFO. The chip will transmit only 1 byte on the TX if the "Number of complete bytes" in the registers 0x1D and 0x1E is 1.

7.5 SPI With SS Pin Only – Clock Polarity Change

Description

DATA_CLK clock polarity needs to be switched when FIFO read operation (single or continues) is executed. During SPI data transmission MOSI line is valid on rising edge; MISO line is valid on falling edge of data clock signal.

NOTE: Not needed for the TRF7970A

Workaround

Firmware must switch clock polarity between FIFO Write and Read.

7.6 SPI With SS Pin Only – IRQ Status Register Reset

Description

The IRQ Status Register (0x0C) is not automatically cleared after reading.

Workaround

Dummy register read is required to clear the content of the IRQ Status Register and drive the IRQ line to low.

7.7 SPI With SS Pin Only – Single Byte Direct Commands

Description

All single byte direct commands need an additional CLK cycle to work.

Workaround

All direct Command functions need to have an additional DATA_CLK cycle before Slave Select l line goes high.

7.8 SPI With SS Pin Only – Some Registers Do Not Take Default Values

Description

Some of the registers do not take the default values when the appropriate protocol is chosen in the ISO Control Register.

Workaround

Manually program the default settings into the TRF796x during initialization.

8 TRF7970A MIFARE™ Compatibility

For communication with MIFARE tags special procedures have to be used. This is because the MIFARE protocol encrypts parity bits and the CRC bytes.

Transmit

For transmitting data from the TRF7970A to a MIFARE tag Special Direct Mode must be used.

When in Special Direct Mode the TRF7970A sends a data clock to the MCU on I/O_5 (pin 22) and the Microcontroller controls the TRF7970A through I/O_2 (TX enable) and I/O_3 (data).

Detailed procedure is described below.

Receive

The TRF7970A can receive MIFARE coded data in two ways.

- By using Direct Mode 1 where the decoded data and bit clock are available directly on I/O_6 and I/O_5 pins. Detailed procedure is described below.
- By using normal receive through FIFO. In this case bit 7 in register 0x01 must be set to a 1 to disable CRC checking and bit 5 in register 0x10 must be set to a 1 to disable parity checking. The 2 bytes CRC are stored in the FIFO, the parity bits are discarded.

To enable receiving 4-bit long packets bit 2 in register 0x10 must be set to a 1 and bit 7 in register 0x01 must be set to a 1 to disable CRC checking.

8.1 TX in Special Direct Mode, RX in Direct Mode 1

Procedure

1. Set TX_Data (I/O_3) low (required for sending correct SOF when entering SDM)
2. Write register 0x0D with 0x3E (Disable No Response IRQ)
3. Write register 0x01 with 0x08 (ISO14443A at 106 kbps)
4. Write register 0x00 with 0x21 (enable TX/RX)
5. Send command 0x16 to disable decoders (for TRF7970A, command is 0x96)
6. Read register 0x0C (to clear IRQ)
7. Write register 0x10 with 0x08 (enable Special Direct Mode)
8. Write register 0x00 with 0x61 (enter Special Direct Mode)
9. Send 8 clock cycles to enter Special Direct Mode, with no stop condition (SS pin stays low)
10. I/O_2 goes high and enables TX, bit clock on I/O_5, data sampled on I/O_3 falling edge
11. I/O_2 goes low and disables TX
12. Stop condition issued on SPI (SS line brought high)
13. Reply from tag received in Direct Mode 1.

8.2 Screen Shots

NOTE: In Figure 1, Special Direct Mode is called Direct Mode 2.

Table 2 shows the signals for Figure 1.

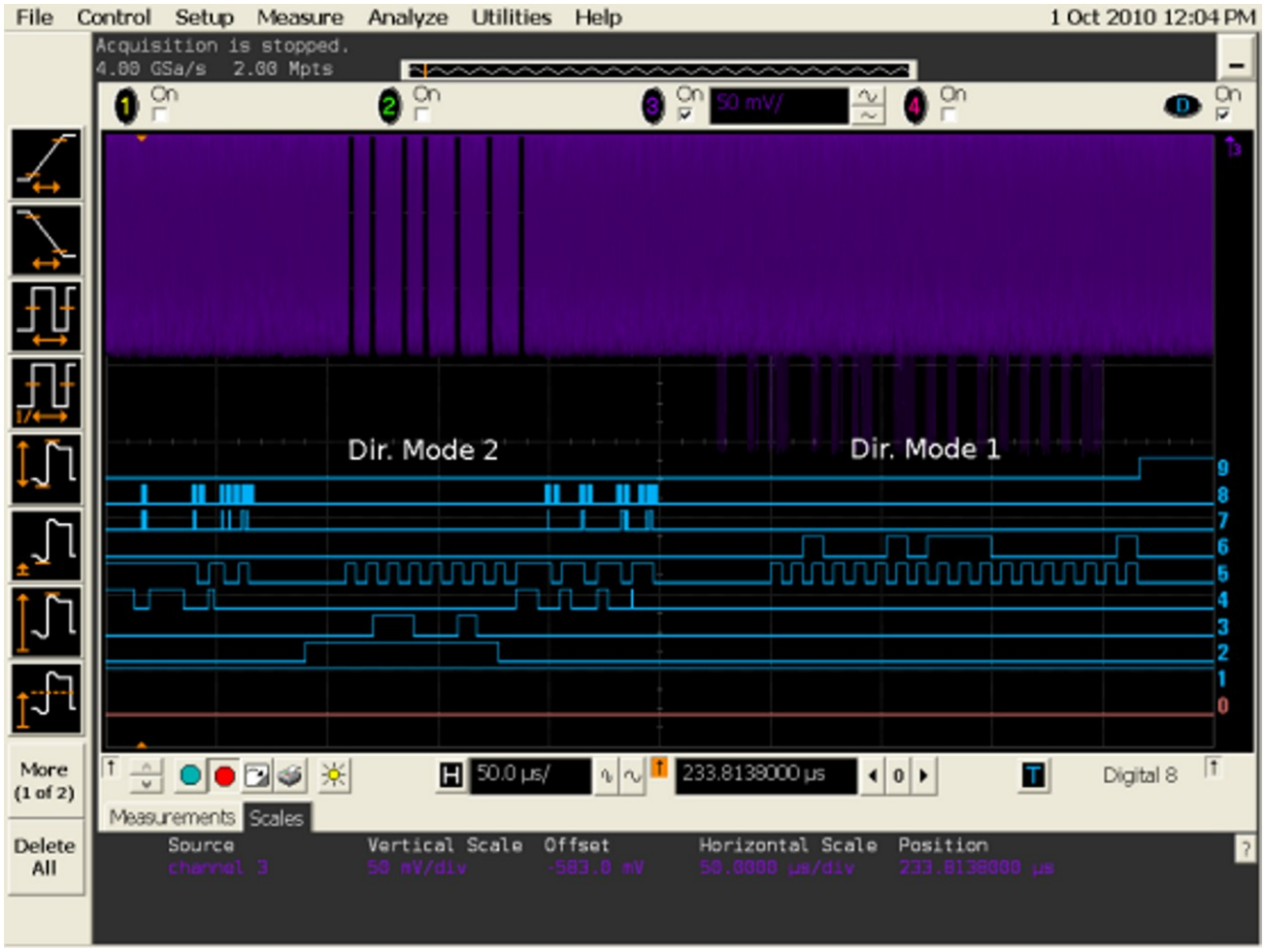

Figure 1. Special Direct Mode (TX REQ1, 0x26, LSB First), RX Reply From Tag)

Table 2. Entering Special Direct Mode (Signals)

Test Point	Signals
Channel 1 (Oscilloscope)	RF Field
D9	IRQ
D8	DATA_CLK
D7	I/O_7 (MOSI)
D6	I/O_6 (MISO)
D5	I/O_5 (bit clock)
D4	I/O_4 (slave select, SS)
D3	I/O_3 (TX data)
D2	I/O_2 (TX enable)
D1	I/O_1
D0	I/O_0

Table 3 shows the steps for Figure 2.

Table 3. Entering Special Direct Mode (Steps)

Step Number	Instruction
1	Read register 0x0C (to clear IRQ if necessary)
2	Write register 0x10 with 0x08 (enable Special Direct Mode)
3	Write register 0x00 with 0x61 (enter Direct Mode)
4	Send 8 clock cycles to enter Direct Mode, with no stop condition (SS pin stays low for duration of Special Direct Mode)

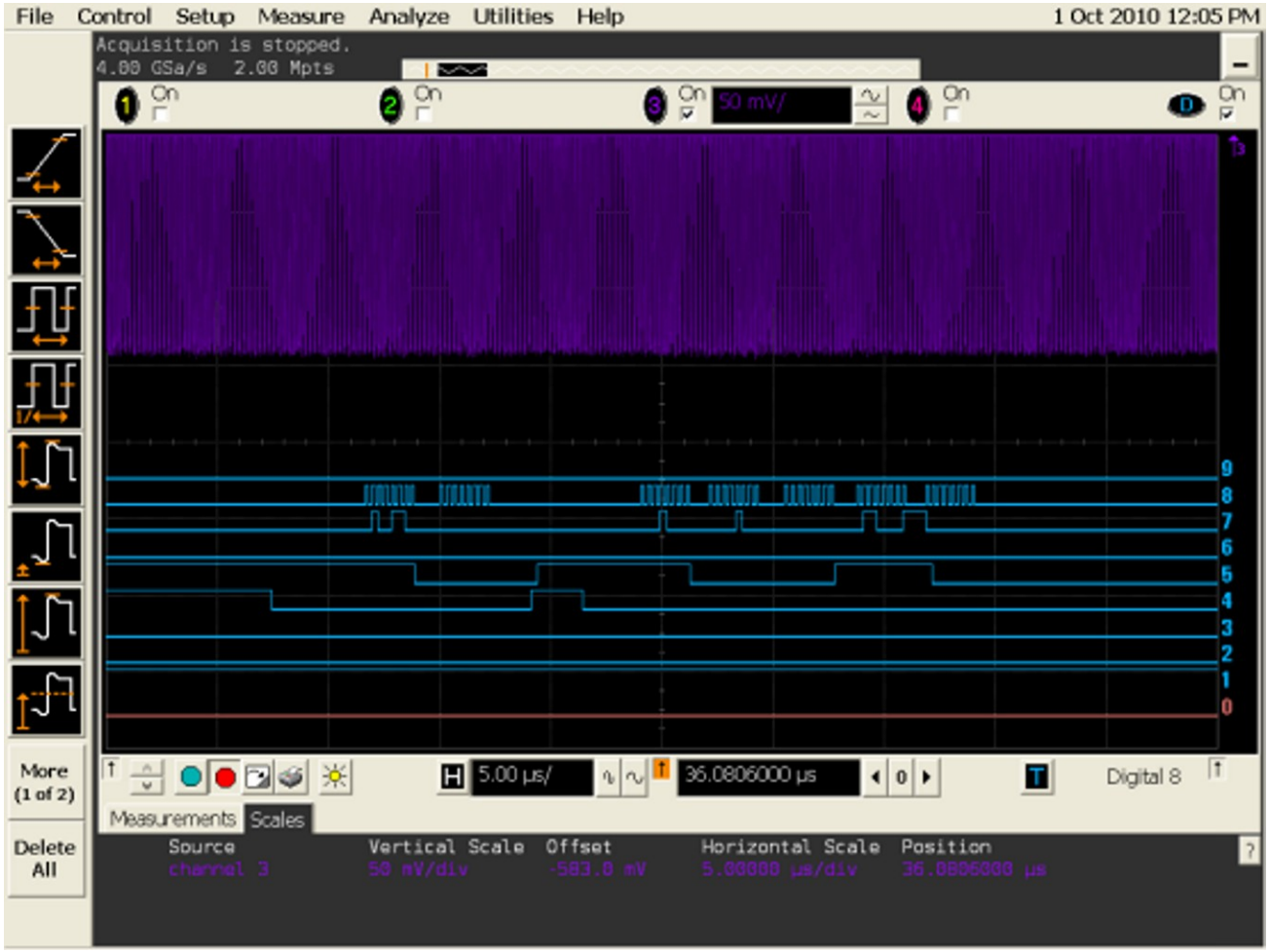

Figure 2. Entering Special Direct Mode

Table 4 shows the steps for Figure 3.

Table 4. TX Part (Steps Detail)

Step Number	Instruction
1	I/0_2 goes high, enabling TX, bit clock on I/O_5, data on I/O_3 sampled on falling edge
2	I/O_2 goes low, disabling TX
3	Stop Condition (SS line brought high)

Figure 3. TX Part (Detail)

Table 5 shows the steps for Figure 4.

Table 5. End of TX (Steps Detail)

Step Number	Instruction
1	Write register 0x10 with 0x00 (disables Special Direct Mode)
2	Read register 0x0C (clearing any IRQ)

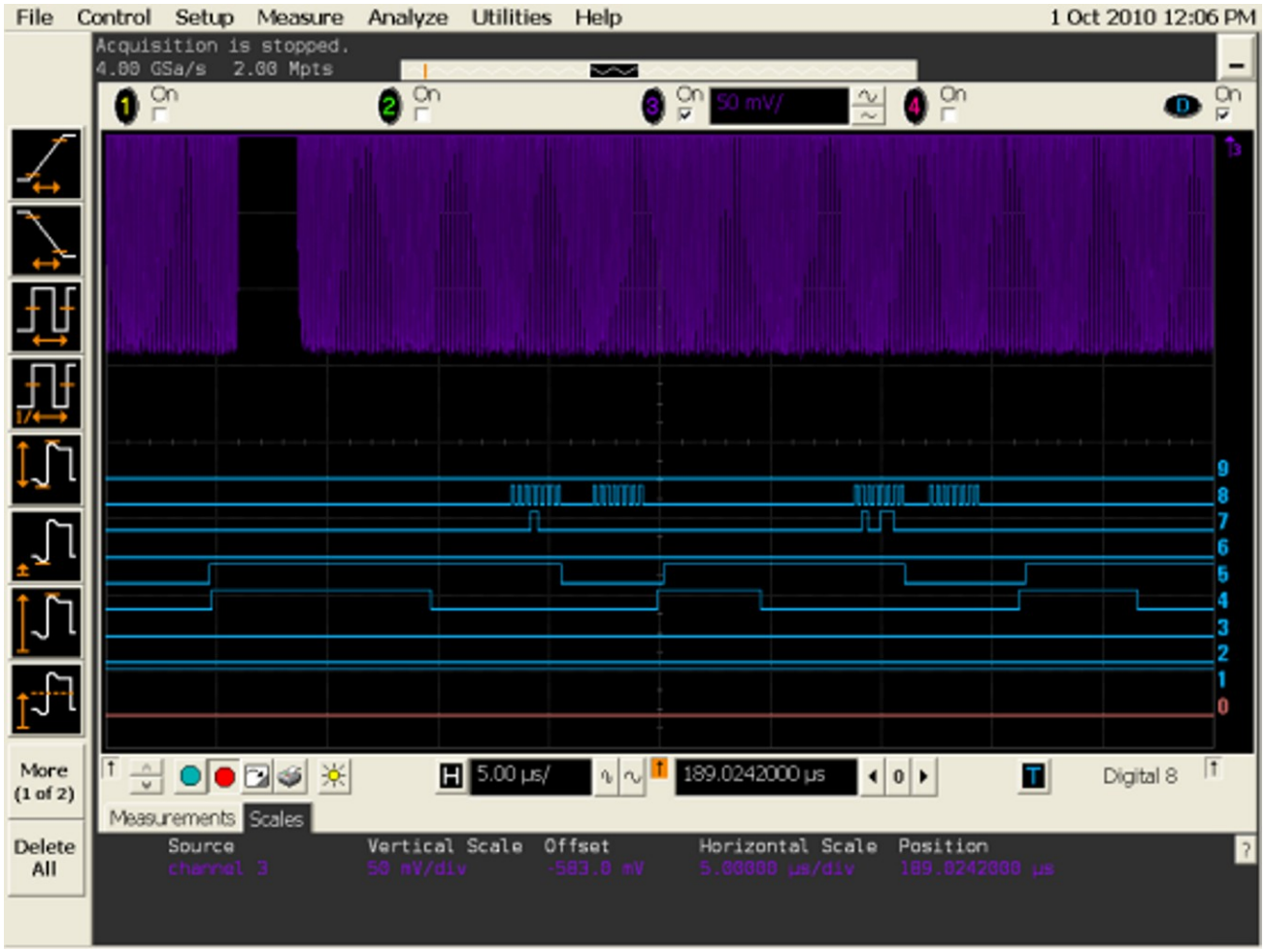

Figure 4. End of TX (Detail)

Table 6 shows the steps for Figure 5.

Table 6. RX Part (Entering Direct Mode 1 Detail Steps)

Step Number	Instruction
1	Read register 0x0C (to clear IRQ if necessary)
2	Write register 0x01 with 0x48 (enable Direct Mode 1)
3	Write register 0x00 with 0x61 (enter Direct Mode)
4	Send 8 clock cycles to enter Direct Mode, with no stop condition (SS pin stays low for duration of Direct Mode 1)

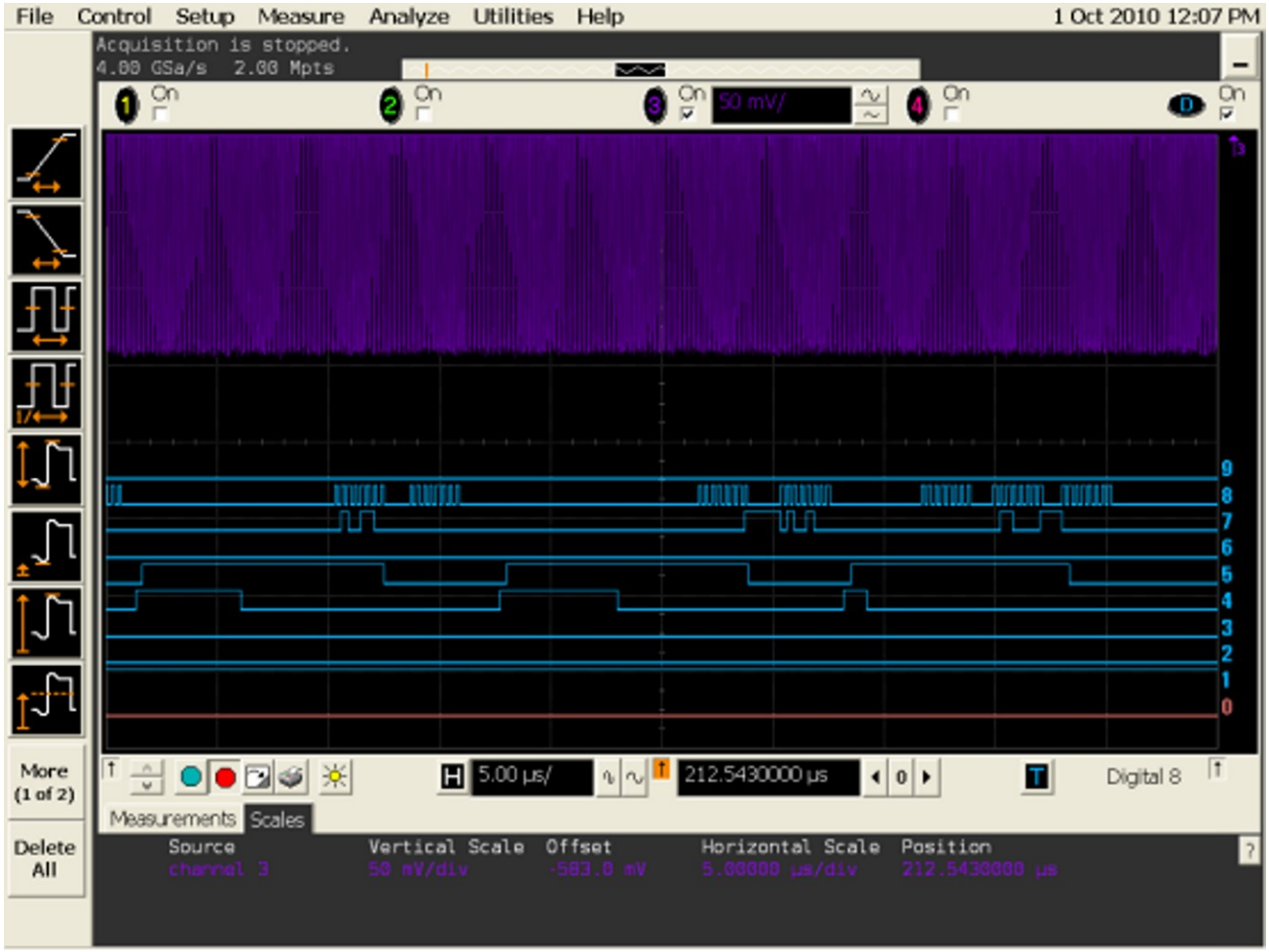

Figure 5. RX Part (Entering Direct Mode 1 Detail)

Table 7 shows the steps for Figure 6.

Table 7. RX Part (Receiving Tag Reply Steps Detail)

Step Number	Instruction
1	Receiving tag reply in Direct Mode 1
2	IRQ goes high at end of RX

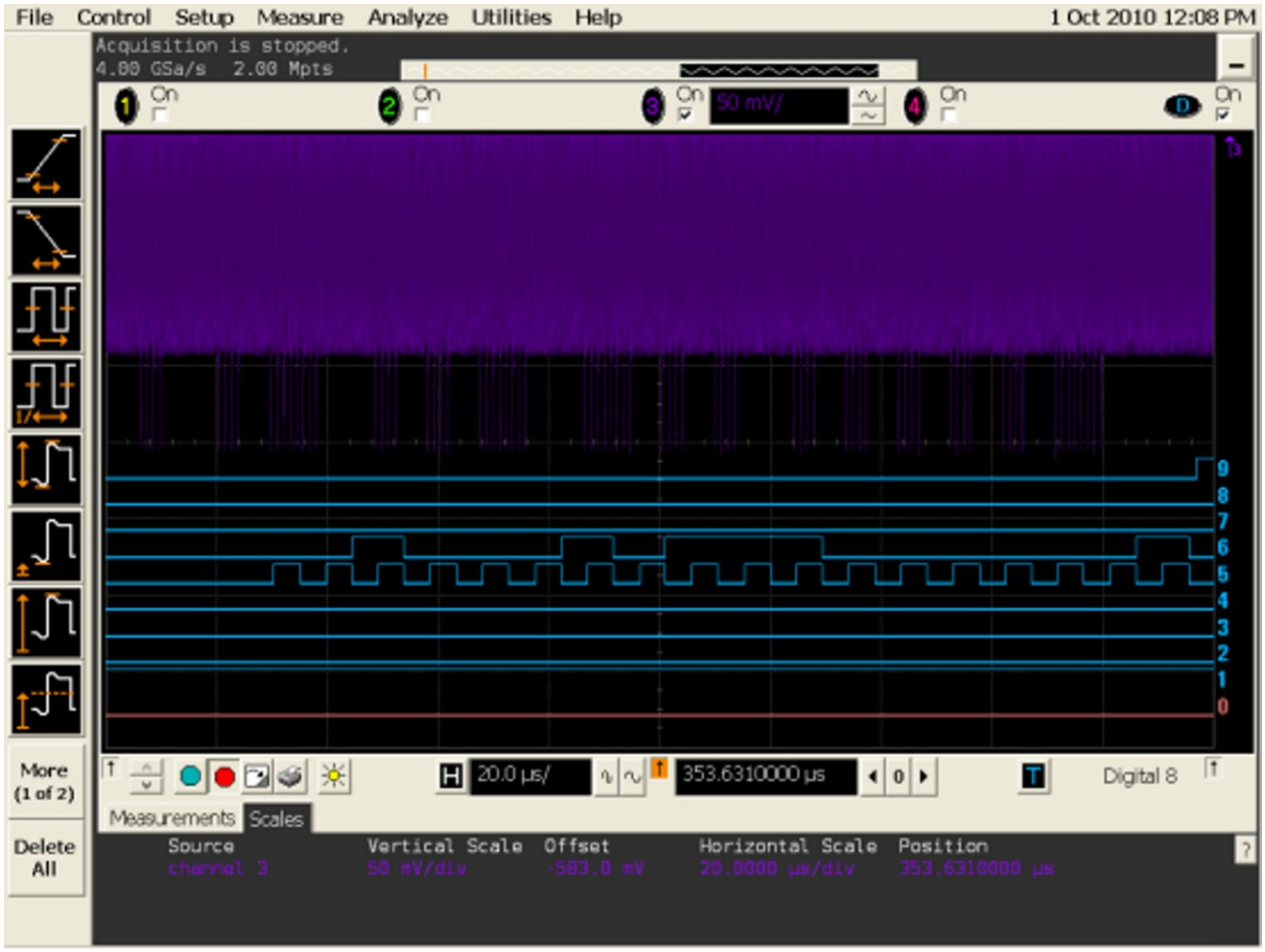

Figure 6. RX Part (Detail)

Table 8. Known Limitations With Specific Tags

Tag	Tag Type	Problem	Workaround
T1	MIFARE Ultralight	The 4-bit ACK and NAK reply can not be decoded with the integrated decoder/framer system. The 4-bit ACK is not according the standard ISO 14443A, so the internal data framing reports an error and needs to be by-passed.	Direct mode
T2	MIFARE classic (standard)	The parity check fails with the encrypted frames as the MIFARE® standard encrypts also the parity bit.	Direct mode
T3	Tags that do not follow the ISO14443A Layer 4 framing	When a transmit frame starts with the code 0x93, 0x95 or 0x97, the reply will not be correctly framed. This happens because the TRF796x devices have an automatic ANTICOLLISION broken byte framer that is activated with the 0x93, 0x95 or 0x97 code.	Direct mode
T4	Cryptographic cards (for example, JCOP™ and DESFire™)	Using a cryptographic card (JCOP or DESFire) at close proximity (<1 cm) can cause a wrong collision error detection.	The reason is the 'calculation noise' emitted by the card, which can be suppressed if the gain is drastically reduced. Use additional gain reduction enabled by test register.
T5	ISO 15693 cards requiring a slot delimiter (EOF)	There are ISO15693 cads on the market requiring a slot delimiter (EOF).	A dedicated MCU timer must be used to generate the 37.76-µs timing grid.

Table 9. TRF7960A Special Functions Register 0x10

Bit	Bit Name	Function	Comment
B7		Reserved	Reserved
B6		Reserved	Reserved
B5		Reserved	Reserved
B4	next_slot_37us	Sets the time grid for next slot command in ISO15693	0 = 18.88 µs 1 = 37.77 µ s
B3		Reserved	Reserved
B2	4_bit_RX	Enable 4-bit replay (ACK, NACK) used by some cards; for example, MIFARE Ultralight	0 = normal receive 1 = 4-bit receive
B1	14_anticoll	Disable anticollision frames for ISO14443A (this bit should be set to 1 after anticollision is finished)	0 = Anticollision framing (0x93, 0x95, 0x97) 1 = Normal framing (no broken bytes)
B0	col_7_6	Selects the number of subcarrier pulses that trigger a collision error in ISO14443A at 106 kbps	0 = 7 subcarrier pulses 1 = 6 subcarrier pulses

Table 10. TRF7970A Special Functions Register 0x10

Bit	Bit Name	Function	Comment
B7		Reserved	Reserved
B6		Reserved	Reserved
B5	par43	Disables parity checking for ISO14443A	
B4	next_slot_37us	Sets the time grid for next slot command in ISO15693	0 = 18.88 µs 1 = 37.77 µs
B3	dir_mode2	Bit stream transmit for MIFARE at 106 kbps	Enables direct mode for transmitting ISO14443A data, bypassing the FIFO and feeding the data bit stream directly onto the encoder.
B2	4_bit_RX	Enable 4-bit replay (ACK, NACK) used by some cards (for example, MIFARE Ultralight)	0 = normal receive 1 = 4-bit receive
B1	14_anticoll	Disable anticollision frames for ISO14443A (this bit should be set to 1 after anticollision is finished)	0 = Anticollision framing (0x93, 0x95, 0x97) 1 = Normal framing (no broken bytes)
B0	col_7_6	Selects the number of subcarrier pulses that trigger collision error in ISO14443A at 106 kbps	0 = 7 subcarrier pulses 1 = 6 subcarrier pulses

Table 11. TRF7970A Special Functions Register 0x11

Bit	Bit Name	Function	Comment
B7		Reserved	Reserved
B6		Reserved	Reserved
B5		Reserved	Reserved
B4		Reserved	Reserved
B3		Reserved	Reserved
B2		Reserved	Reserved
B1		Reserved	Reserved
B0	irg_srx	Copy of the RX start signal (Bit 6) of the IRQ Status Register (0x0C)	Signals the RX SOF was received and the RX is in progress. IRQ when RX is completed.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from August 4, 2011 to June 30, 2016	Page
• Added steps 1 and 2 in Section 8.1, *TX in Special Direct Mode, RX in Direct Mode 1*	5

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