TS5A23167 0.9-Ω dual SPST analog switch 5-V, 3.3-V 2-channel analog switch

1 Features

- Isolation in Powered-Off Mode, $V_+ = 0$
- Low ON-State Resistance (0.9 Ω)
- Control Inputs Are 5.5-V Tolerant
- Low Charge Injection
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model(A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data Acquisition Systems
- Communication Circuits
- Modems
- Hard Drives
- Computer Peripherals
- Wireless Terminals and Peripherals

3 Description

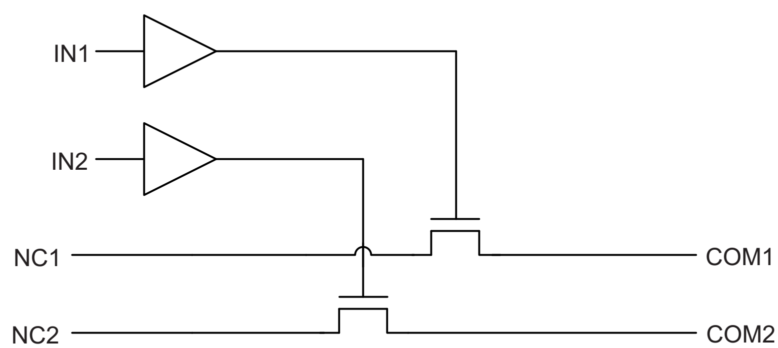
The TS5A23167 is a dual single-pole single-throw (SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A23167	VSSOP (8)	2.30 mm × 2.00 mm
	DSBGA (8)	1.25 mm × 2.25mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

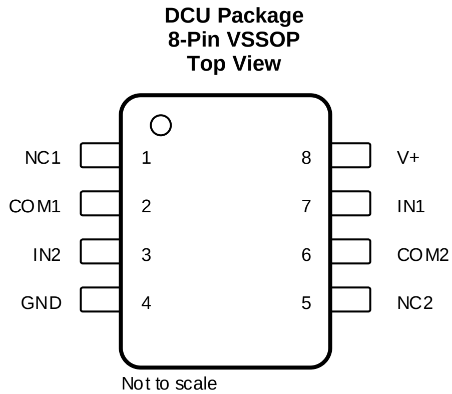
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

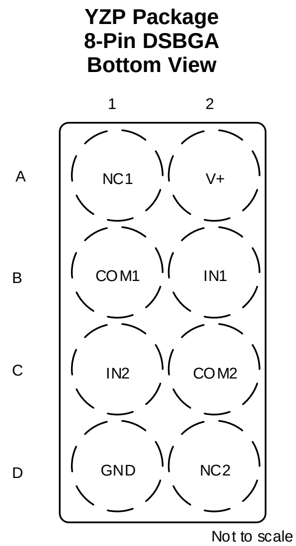
Changes from Revision B (January 2019) to Revision C	Page
• Changed pins NO1 and NO2 To: NC1 and NC2 in the *Simplified Schematic*	1
• Changed pins NO1 and NO2 To: NC1 and NC2 in the *Functional Block Diagram*	19
• Changed L From: Off To: On in Table 1	19
• Changed H From: On To: Off in Table 1	19

Changes from Revision A (September 2012) to Revision B	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Changed the DSBGA package pin numbers	3

Changes from Original (May 2005) to Revision A	Page
• Updated package options information	1

5 Pin Configuration and Functions





Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DCU NO.	DSBGA NO.		
NC1	1	A1	I/O	Normally closed
COM1	2	B1	I/O	Common
IN2	3	C1	GND	Digital control pin to connect COM to NC
GND	4	D1	I	Digital ground
NC2	5	D2	I	Normally closed
COM2	6	C2	I/O	Common
IN1	7	B2	I/O	Digital control pin to connect COM to NC
V+	8	A2	PWR	Power Supply

6 Specifications

6.1 Absolute Maximum Ratings[1] [2]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range[3]		–0.5	6.5	V
V_{NC} V_{COM}	Analog voltage range[3] [4] [5]		–0.5	$V_+ + 0.5$	V
I_K	Analog port diode current	V_{NC}, $V_{COM} < 0$	–50		mA
I_{NC} I_{COM}	On-state switch current	V_{NC}, V_{COM} = 0 to V_+	–200	200	mA
	On-state peak switch current[6]		–400	400	
V_I	Digital input voltage range[3] [4]		–0.5	6.5	V
I_{IK}	Digital clamp current	$V_I < 0$	–50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		–100	100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1-ms duration < 10% duty cycle.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	+2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	+1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage	0	V_+	V
V_+	Supply voltage	1.65	5.5	V
V_I	Control Input Voltage	0	5.5	V
T_A	Operating free-air temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC[1]		TS5A23166		UNIT
		DCU (VSSOP)	YZP (DSBGA)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	212.2	98.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.6	1.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91.7	26.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.1	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	91.1	26.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics for 5-V Supply(1)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NC}					0		V_+	V
Peak ON resistance	r_{peak}	$0 \le V_{NC} \le V_+$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	4.5 V		0.9	1.1	Ω
				Full				1.2	
ON-state resistance	r_{on}	V_{NC} = 2.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	4.5 V		0.75	0.9	Ω
				Full				1	
ON-state resistance match between channels	Δr_{on}	V_{NC} = 2.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	4.5 V		0.04	0.1	Ω
				Full				0.1	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NC} \le V_+$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	4.5 V		0.2		Ω
		V_{NC} = 1 V, 1.5 V, 2.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C			0.15	0.25	
				Full				0.25	
NC OFF leakage current	$I_{NC(OFF)}$	V_{NC} = 1 V, V_{COM} = 4.5 V, or V_{NC} = 4.5 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	5.5 V	0 V	4	20	nA
				Full		–150		150	
	$I_{NC(PWROFF)}$	V_{NC} = 0 to 5.5 V, V_{COM} = 5.5 V to 0,	Switch OFF, See Figure 14	25°C	0 V	–10	0.2	10	µA
				Full		–50		50	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NC} = 4.5 V, or V_{COM} = 4.5 V, V_{NC} = 1 V,	Switch OFF, See Figure 14	25°C	5.5 V	0 V	4	20	nA
				Full		–150		150	
	$I_{COM(PWROFF)}$	V_{COM} = 0 to 5.5 V, V_{NC} = 5.5 V to 0,	Switch OFF, See Figure 14	25°C	0 V	–10	0.2	10	µA
				Full		–50		50	
NC ON leakage current	$I_{NC(ON)}$	V_{NC} = 1 V, V_{COM} = Open, or V_{NC} = 4.5 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	5.5 V	–5	0.4	5	nA
				Full		–50		50	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NC} = Open, or V_{COM} = 4.5 V, V_{NC} = Open,	Switch ON, See Figure 15	25°C	5.5 V	–5	0.4	5	nA
				Full		–50		50	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		2.4		5.5	V
Input logic low	V_{IL}			Full		0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	5.5 V	–2	0.3	2	nA
				Full		–20		20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.6 Electrical Characteristics for 5-V Supply[1] (continued)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	5 V	1	4.5	7.5	ns
				Full	4.5 V to 5.5 V	1		9	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	5 V	4.5	8	11	ns
				Full	4.5 V to 5.5 V	3.5		13	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0 ,	C_L = 1 nF, See Figure 21	25°C	5 V		6		pC
NC OFF capacitance	$C_{NC(OFF)}$	V_{NC} = V_+ or GND, Switch OFF,	See Figure 16	25°C	5 V		19		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_+ or GND, Switch OFF,	See Figure 16	25°C	5 V		18		pF
NC ON capacitance	$C_{NC(ON)}$	V_{NC} = V_+ or GND, Switch ON,	See Figure 16	25°C	5 V		35.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	5 V		35.5		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	5 V		2		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	5 V		150		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 19	25°C	5 V		–62		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 20	25°C	5 V		–85		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 22	25°C	5 V		0.005		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	5.5 V		0.01	0.1	μA
				Full				1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

6.7 Electrical Characteristics for 3.3-V Supply(1)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NC}					0		V_+	V
Peak ON resistance	r_{peak}	$0 \le V_{NC} \le V_+$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	3 V		1.3	1.6	Ω
				Full				1.8	
ON-state resistance	r_{on}	V_{NC} = 2 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	3 V		1.1	1.5	Ω
				Full				1.7	
ON-state resistance match between channels	Δr_{on}	V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	3 V		0.04	0.1	Ω
				Full				0.1	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NC} \le V_+$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	3 V		0.3		Ω
		V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C			0.15	0.25	
				Full				0.25	
NC OFF leakage current	$I_{NC(OFF)}$	V_{NC} = 1 V, V_{COM} = 3 V, or V_{NC} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	3.6 V	–5	0.5	5	nA
				Full		–50		50	
	$I_{NC(PWROFF)}$	V_{NC} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,	Switch OFF, See Figure 14	25°C	0 V	–5	0.1	5	µA
				Full		–25		25	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NC} = 3 V, or V_{COM} = 3 V, V_{NC} = 1 V,	Switch OFF, See Figure 14	25°C	3.6 V	–5	0.5	5	nA
				Full		–50		50	
	$I_{COM(PWROFF)}$	V_{COM} = 0 to 3.6 V, V_{NC} = 3.6 V to 0,	Switch OFF, See Figure 14	25°C	0 V	–5	0.1	5	µA
				Full		–25		25	
NC ON leakage current	$I_{NC(ON)}$	V_{NC} = 1 V, V_{COM} = Open, or V_{NC} = 3 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	3.6 V	–2	0.3	2	nA
				Full		–20		20	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NC} = Open, or V_{COM} = 3 V, V_{NC} = Open,	Switch ON, See Figure 15	25°C	3.6 V	–2	0.3	2	nA
				Full		–20		20	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		2		5.5	V
Input logic low	V_{IL}			Full		0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	3.6 V	–2	0.3	2	nA
				Full		–20		20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.8 Electrical Characteristics for 3.3-V Supply(1) (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	C_L = 35 pF, See Figure 17	25°C	3.3 V	1.5	5	9.5	ns
				Full	3 V to 3.6 V	1.0		10	
Turn-off time	t_{OFF}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	C_L = 35 pF, See Figure 17	25°C	3.3 V	4.5	8.5	11	ns
				Full	3 V to 3.6 V	3		12.5	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$,	C_L = 1 nF, See Figure 21	25°C	3.3 V		6		pC
NC OFF capacitance	$C_{NC(OFF)}$	$V_{NC} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		19.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		18.5		pF
NC ON capacitance	$C_{NC(ON)}$	$V_{NC} = V_+$ or GND, Switch ON,	See Figure 16	25°C	3.3 V		36		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	3.3 V		36		pF
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 16	25°C	3.3 V		2		pF
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON,	See Figure 18	25°C	3.3 V		150		MHz
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, f = 1 MHz,	Switch OFF, See Figure 19	25°C	3.3 V		–62		dB
Crosstalk	X_{TALK}	$R_L = 50\ \Omega$, f = 1 MHz,	Switch ON, See Figure 20	25°C	3.3 V		–85		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 22	25°C	3.3 V		0.01		%
Supply									
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	3.6 V		0.001	0.05	µA
				Full				0.3	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

6.9 Electrical Characteristics for 2.5-V Supply(1)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NC}				2.3 V	0		V_+	V
Peak ON resistance	r_{peak}	0 ≤ V_{NC} ≤ V_+, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	2.3 V		1.8	2.4	Ω
				Full				2.6	
ON-state resistance	r_{on}	V_{NC} = 2 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	2.3 V		1.2	2.1	Ω
				Full				2.4	
ON-state resistance match between channels	Δr_{on}	V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	2.3 V		0.04	0.15	Ω
				Full				0.15	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ V_{NC} ≤ V_+, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	2.3 V		0.7		Ω
		V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C			0.4	0.6	
				Full				0.6	
NC OFF leakage current	$I_{NC(OFF)}$	V_{NC} = 1 V, V_{COM} = 3 V, or V_{NC} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	2.7 V	–5	0.3	5	nA
				Full		–50		50	
	$I_{NC(PWROFF)}$	V_{NC} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,	Switch OFF, See Figure 14	25°C	0 V	–2	0.05	2	μA
				Full		–15		15	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NC} = 3 V, or V_{COM} = 3 V, V_{NC} = 1 V,	Switch OFF, See Figure 14	25°C	2.7 V	–5	0.3	5	nA
				Full		–50		50	
	$I_{COM(PWROFF)}$	V_{COM} = 0 to 3.6 V, V_{NC} = 3.6 V to 0,	Switch OFF, See Figure 14	25°C	0 V	–2	0.05	2	μA
				Full		–15		15	
NC ON leakage current	$I_{NC(ON)}$	V_{NC} = 1 V, V_{COM} = Open, or V_{NC} = 3 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	2.7 V	–2	0.3	2	nA
				Full		–20		20	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NC} = Open, or V_{COM} = 3 V, V_{NC} = Open,	Switch ON, See Figure 15	25°C	2.7 V	–2	0.3	2	nA
				Full		–20		20	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		1.8		5.5	V
Input logic low	V_{IL}			Full		0		0.6	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	2.7 V	–2	0.3	2	nA
				Full		–20		20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.10 Electrical Characteristics for 2.5-V Supply[(1)] (continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	C_L = 35 pF, See Figure 17	25°C	2.5 V	2	6	10	ns
				Full	2.3 V to 2.7 V	1		12	
Turn-off time	t_{OFF}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	C_L = 35 pF, See Figure 17	25°C	2.5 V	4.5	8	12.5	ns
				Full	2.3 V to 2.7 V	3		15	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$,	C_L = 1 nF, See Figure 21	25°C	2.5 V		4		pC
NC OFF capacitance	$C_{NC(OFF)}$	$V_{NC} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		19.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		18.5		pF
NC ON capacitance	$C_{NC(ON)}$	$V_{NC} = V_+$ or GND, Switch ON,	See Figure 16	25°C	2.5 V		36.5		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	2.5 V		36.5		pF
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 16	25°C	2.5 V		2		pF
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON,	See Figure 18	25°C	2.5 V		150		MHz
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, f = 1 MHz,	Switch OFF, See Figure 19	25°C	2.5 V		–62		dB
Crosstalk	X_{TALK}	$R_L = 50\ \Omega$, f = 1 MHz,	Switch ON, See Figure 20	25°C	3.3 V		–85		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 22	25°C	2.5 V		0.02		%
Supply									
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	2.7 V		0.001	0.02	µA
				Full				0.25	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

6.11 Electrical Characteristics for 1.8-V Supply(1)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted))

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NC}					0		V_+	V
Peak ON resistance	r_{peak}	$0 \le V_{NC} \le V_+$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	1.65 V		4.2	25	Ω
				Full				30	
ON-state resistance	r_{on}	V_{NC} = 2 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	1.65 V		1.6	3.9	Ω
				Full				4.0	
ON-state resistance match between channels	Δr_{on}	V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	1.65 V		0.04	0.2	Ω
				Full				0.2	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NC} \le V_+$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	1.65 V		2.8		Ω
		V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C			4.1	22	
				Full				27	
NC OFF leakage current	$I_{NC(OFF)}$	V_{NC} = 1 V, V_{COM} = 3 V, or V_{NC} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	1.95 V	–5		5	nA
				Full		–50		50	
	$I_{NC(PWROFF)}$	V_{NC} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,	Switch OFF, See Figure 14	25°C	0 V	–2		2	μA
				Full		–10		10	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NC} = 3 V, or V_{COM} = 3 V, V_{NC} = 1 V,	Switch OFF, See Figure 14	25°C	1.95 V	–5		5	nA
				Full		–50		50	
	$I_{COM(PWROFF)}$	V_{COM} = 0 to 3.6 V, V_{NC} = 3.6 V to 0,	Switch OFF, See Figure 14	25°C	0 V	–2		2	μA
				Full		–10		10	
NC ON leakage current	$I_{NC(ON)}$	V_{NC} = 1 V, V_{COM} = Open, or V_{NC} = 3 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	1.95 V	–2		2	nA
				Full		–20		20	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NC} = Open, or V_{COM} = 3 V, V_{NC} = Open,	Switch ON, See Figure 15	25°C	1.95 V	–2		2	nA
				Full		–20		20	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		1.5		5.5	V
Input logic low	V_{IL}			Full		0		0.6	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	1.95 V	–2	0.3	2	nA
				Full		–20		20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.12 Electrical Characteristics for 1.8-V Supply[1] (continued)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted))

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	C_L = 35 pF, See Figure 17	25°C	1.8 V	3	9	18	ns
				Full	1.65 V to 1.95 V	1		20	
Turn-off time	t_{OFF}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	C_L = 35 pF, See Figure 17	25°C	1.8 V	5	10	15.5	ns
				Full	1.65 V to 1.95 V	4		18.5	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$,	C_L = 1 nF, See Figure 21	25°C	1.8 V		2		pC
NC OFF capacitance	$C_{NC(OFF)}$	$V_{NC} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		19.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		18.5		pF
NC ON capacitance	$C_{NC(ON)}$	$V_{NC} = V_+$ or GND, Switch ON,	See Figure 16	25°C	1.8 V		36.5		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	1.8 V		36.5		pF
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 16	25°C	1.8 V		2		pF
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON,	See Figure 18	25°C	1.8 V		150		MHz
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, f = 1 MHz,	Switch OFF, See Figure 19	25°C	1.8 V		–62		dB
Crosstalk	X_{TALK}	$R_L = 50\ \Omega$, f = 1 MHz,	Switch ON, See Figure 20	25°C	1.8 V		–85		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$, C_L = 50 pF,	f = 20 Hz to 20 kHz See Figure 22	25°C	1.8 V		0.055		%
Supply									
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	1.95 V		0.001	0.01	μA
				Full				0.15	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

6.13 Typical Characteristics

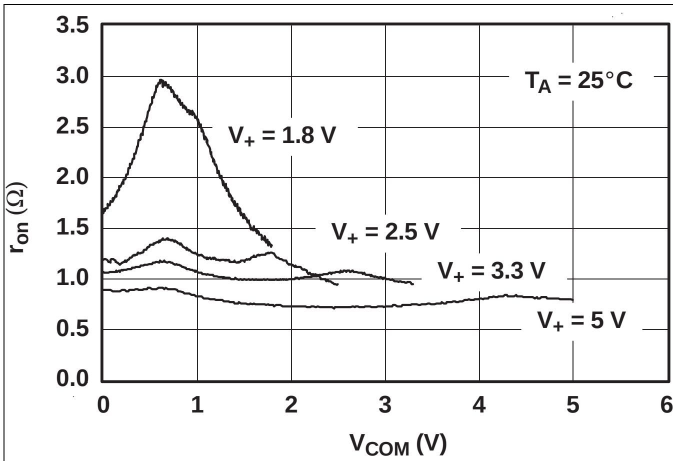


Figure 1. r_{on} vs V_{COM}

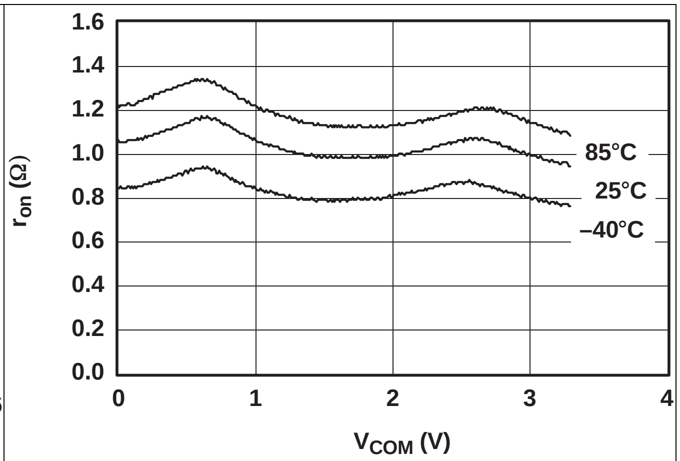


Figure 2. r_{on} vs V_{COM} (V_+ = 3.3 V)

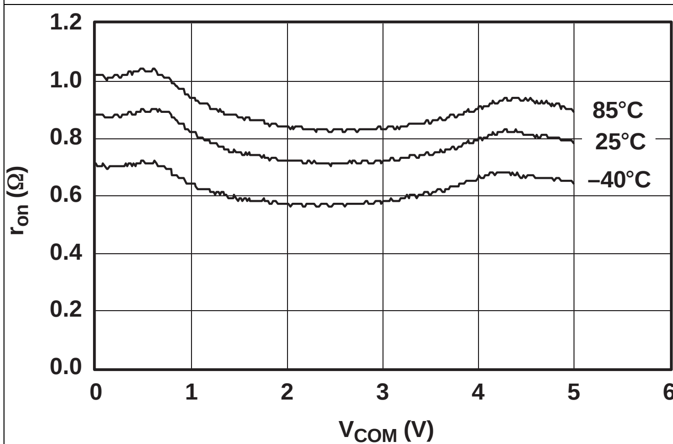


Figure 3. r_{on} vs V_{COM} (V_+ = 5 V)

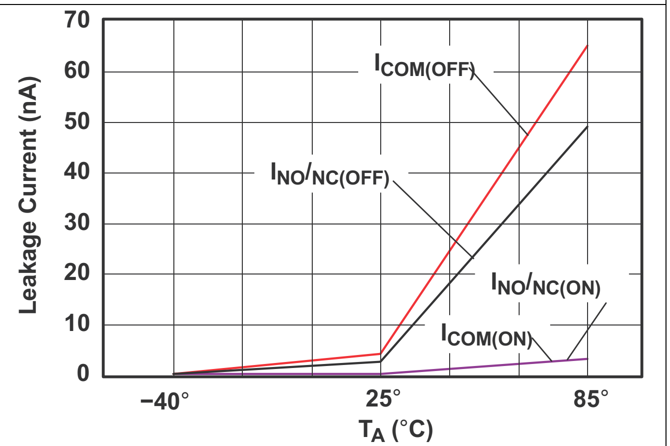


Figure 4. Leakage Current vs Temperature (V_+ = 5.5 V)

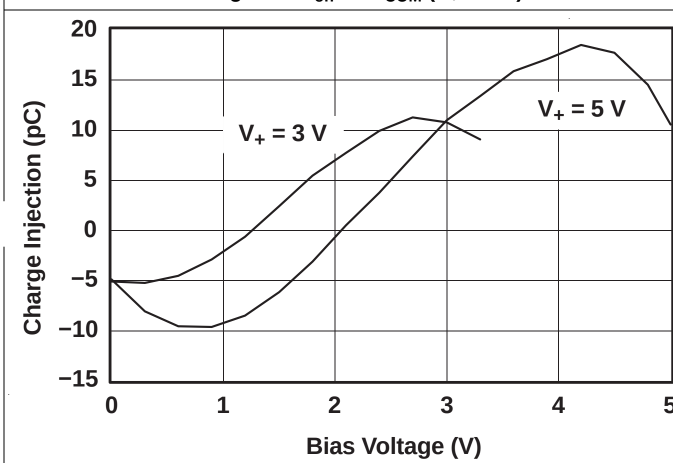


Figure 5. Charge Injection (Q_C) vs V_{COM}

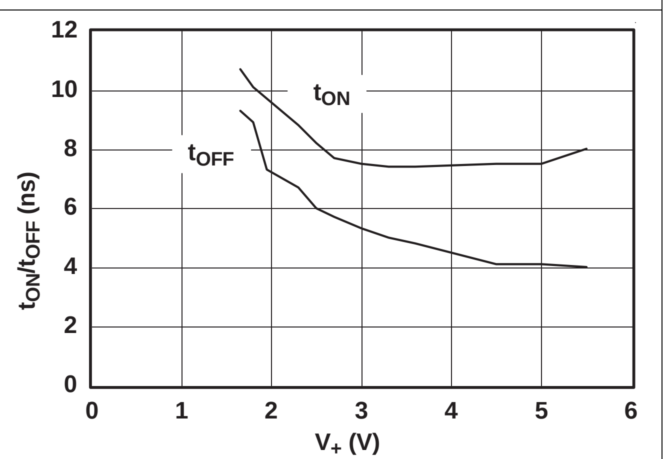


Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

Typical Characteristics (continued)

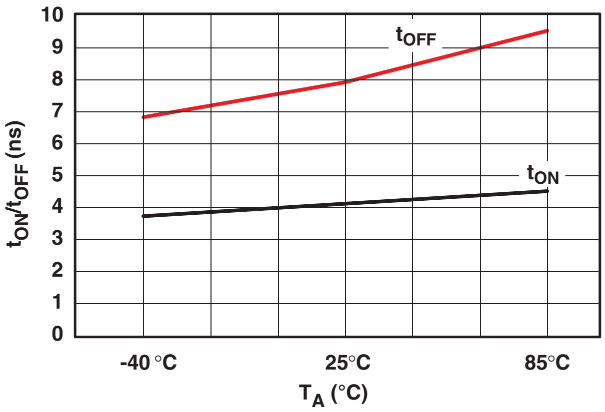


Figure 7. t_{ON} and t_{OFF} vs Temperature (V_+ = 5 V)

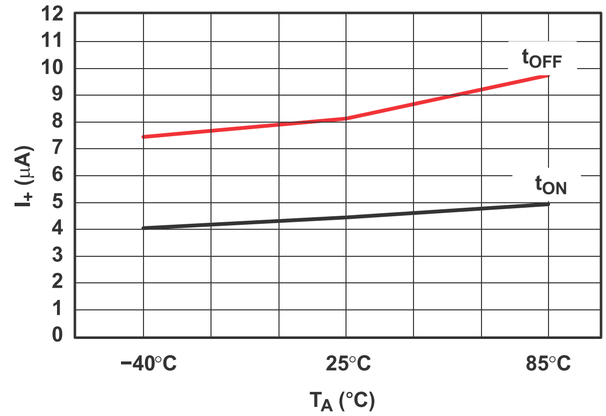


Figure 8. t_{ON} and t_{OFF} vs Temperature (V_+ = 5 V)

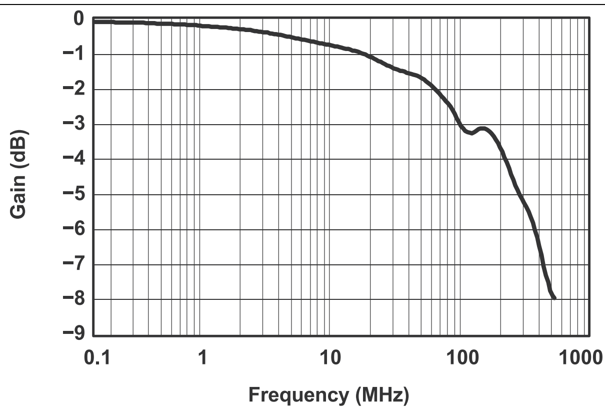


Figure 9. Bandwidth (V_+ = 5 V)

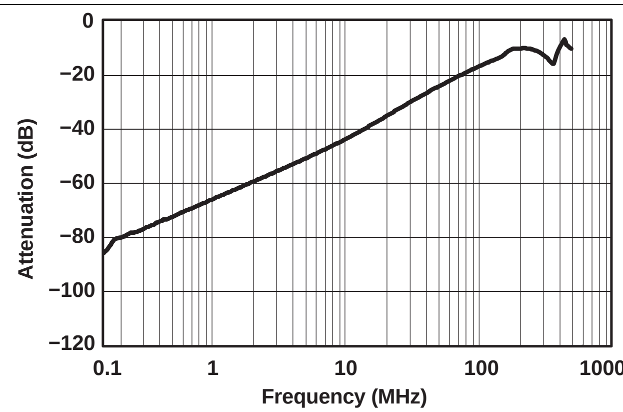


Figure 10. OFF Isolation and Crosstalk (V_+ = 5 V)

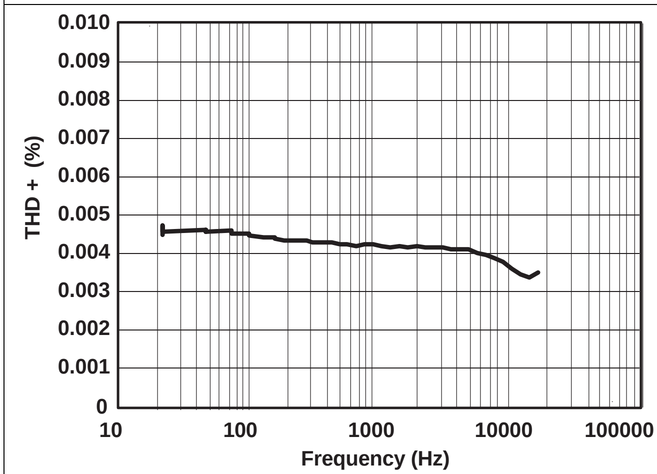


Figure 11. Total Harmonic Distortion vs Frequency

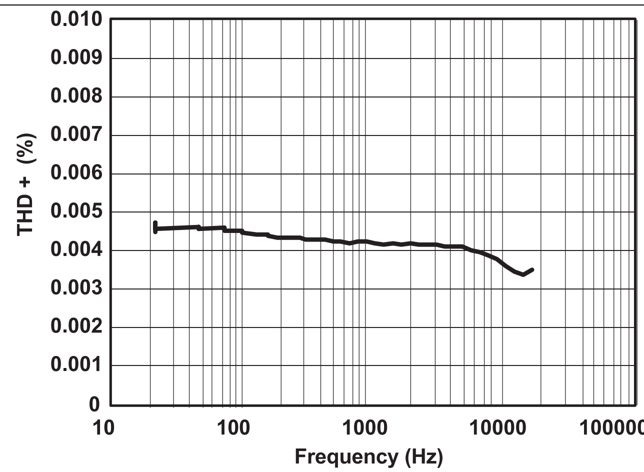


Figure 12. Total Harmonic Distortion vs Frequency (V_+ = 5 V)

Typical Characteristics (continued)

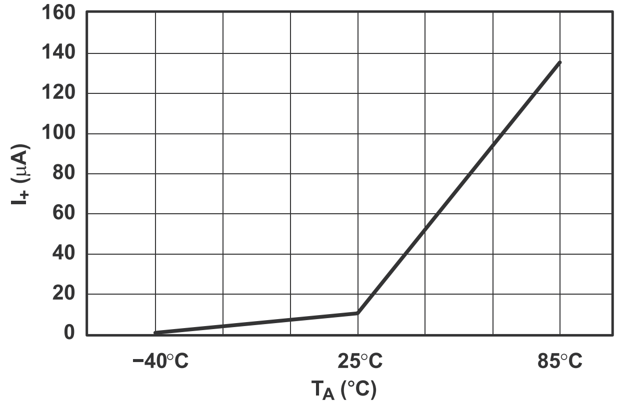


Figure 13. Power-Supply Current vs Temperature (V_+ = 5 V)

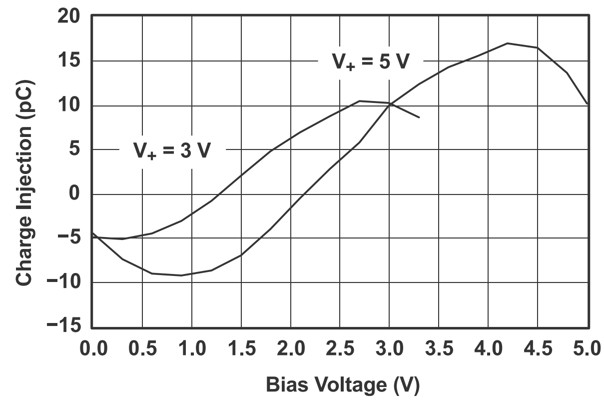


Figure 14. Charge Injection (Q_C) vs V_{COM}

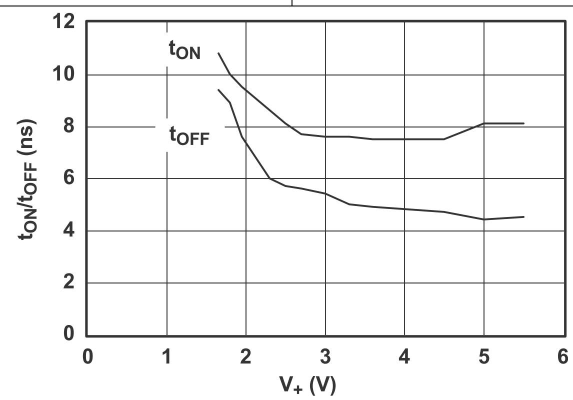


Figure 15. t_{ON} and t_{OFF} vs Supply Voltage

7 Parameter Measurement Information

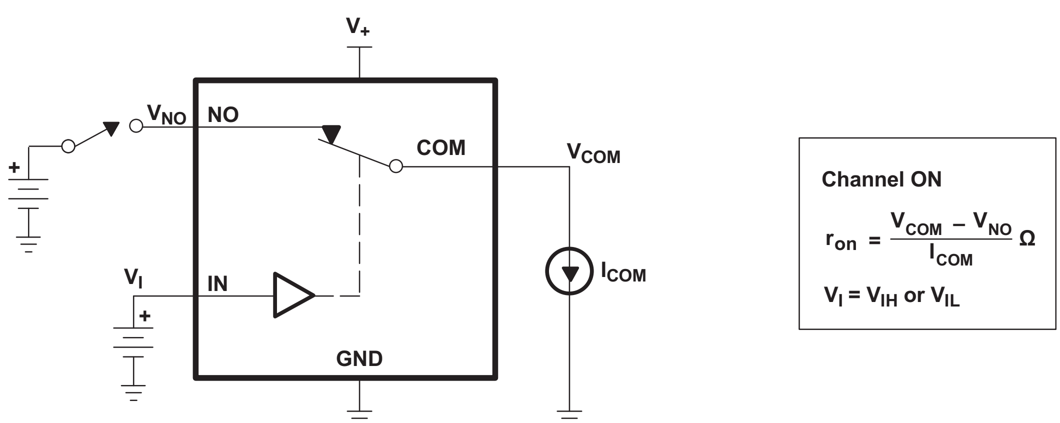


Figure 16. ON-State Resistance (r_{on})

Parameter Measurement Information (continued)

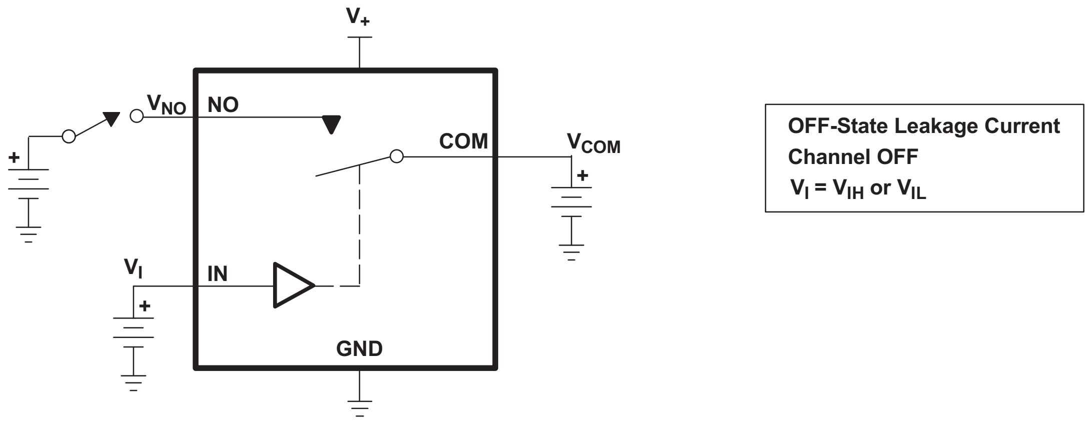


Figure 17. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NC(OFF)}$, $I_{COM(PWROFF)}$, $I_{NC(PWR(FF)}$)

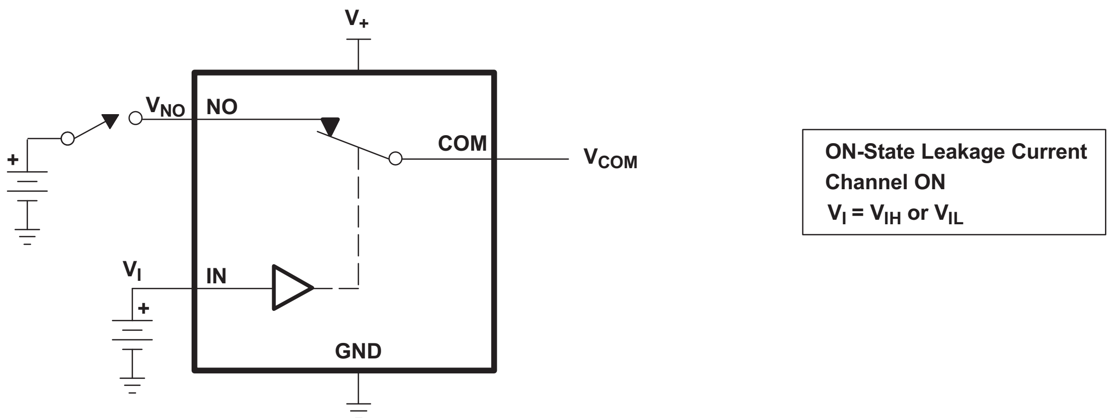


Figure 18. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$)

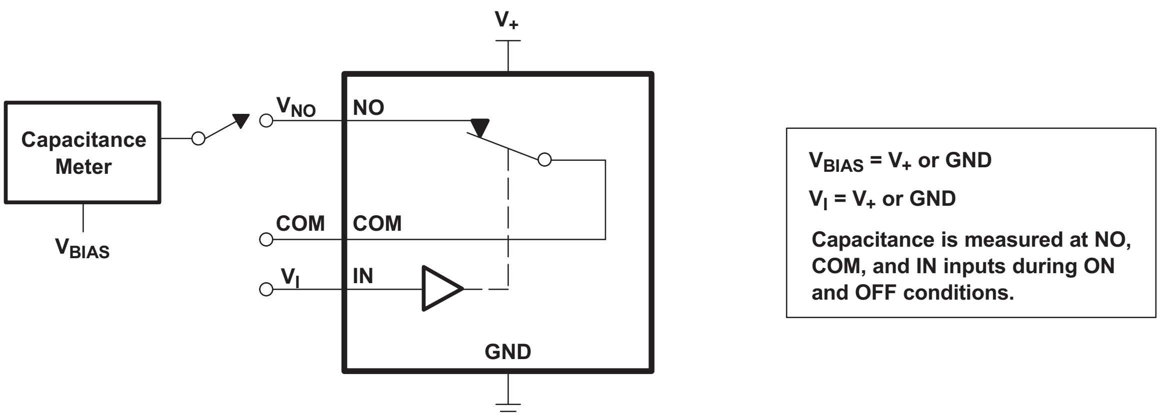
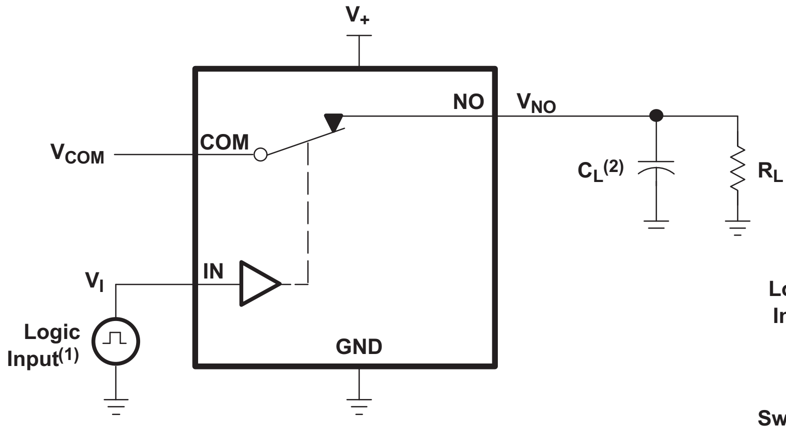
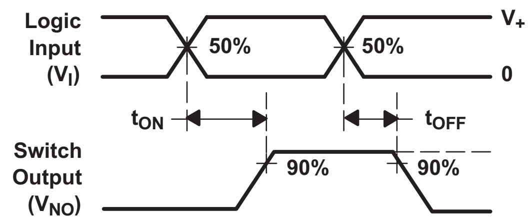


Figure 19. Capacitance (C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NC(ON)}$)

Parameter Measurement Information (continued)



TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_+
t_{OFF}	50 Ω	35 pF	V_+



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 20. Turnon (t_{ON}) and Turnoff Time (t_{OFF})

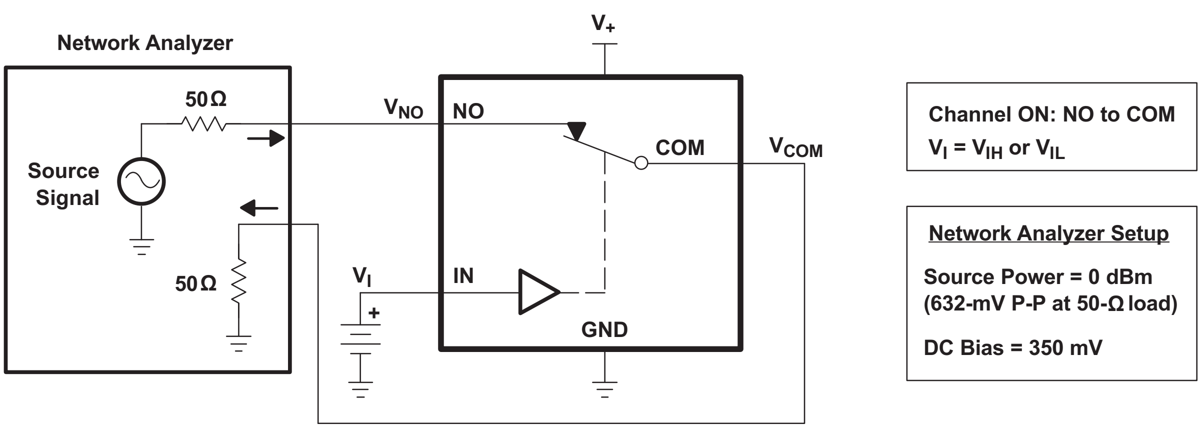


Figure 21. Bandwidth (BW)

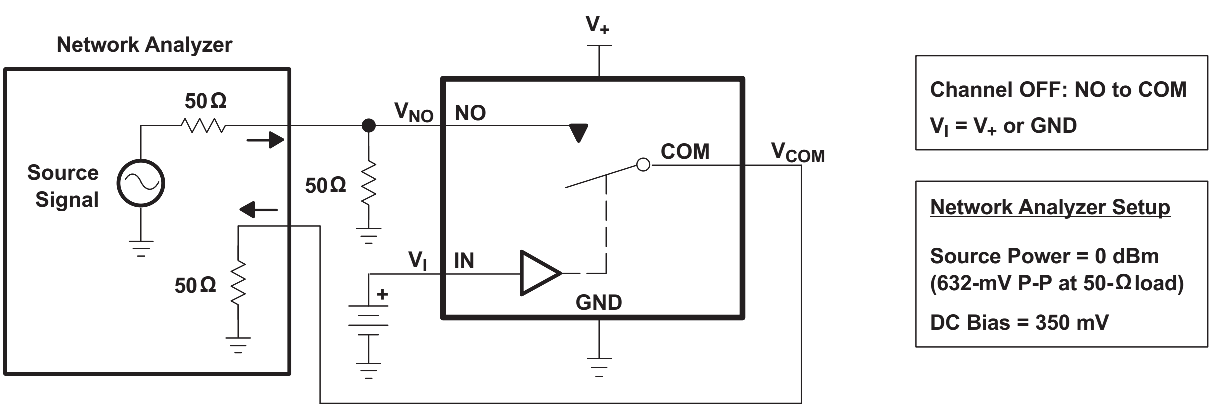


Figure 22. OFF Isolation (O_{ISO})

Parameter Measurement Information (continued)

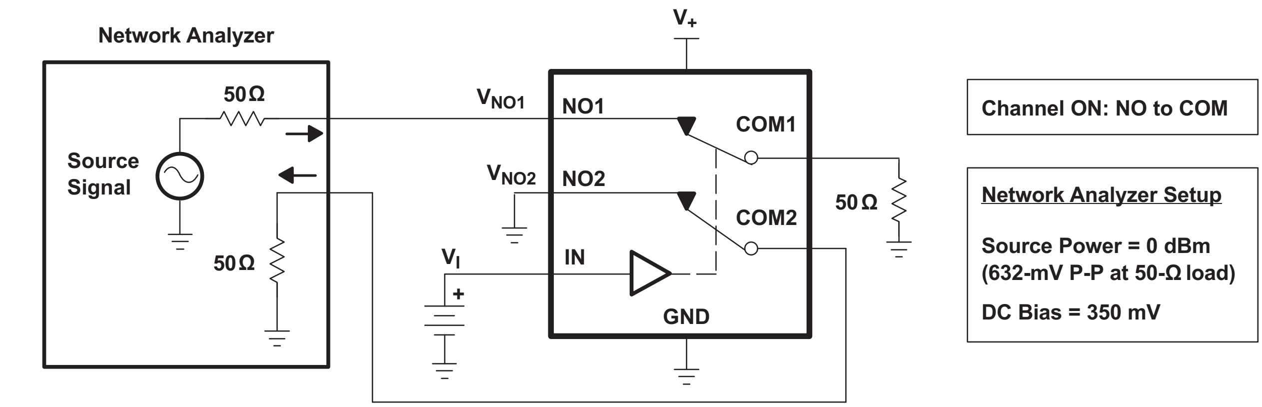
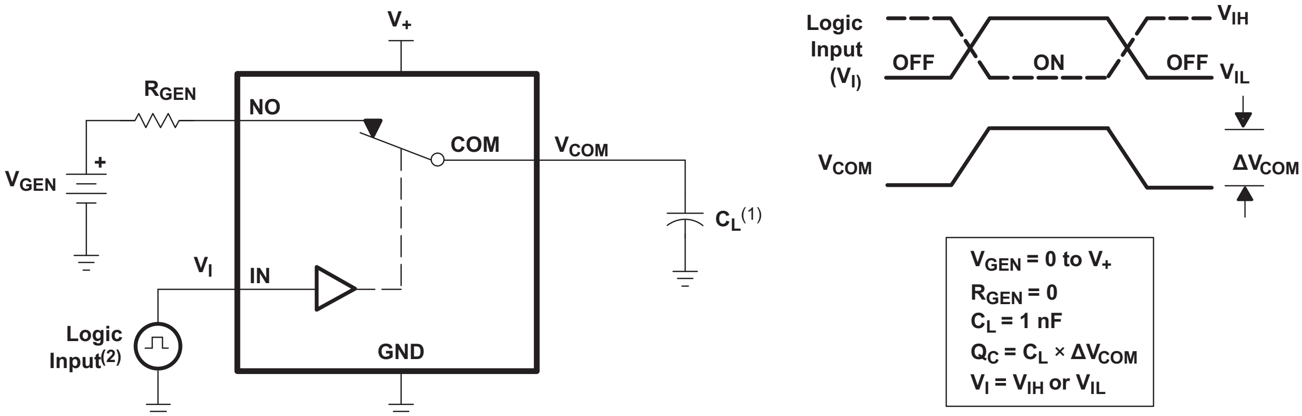


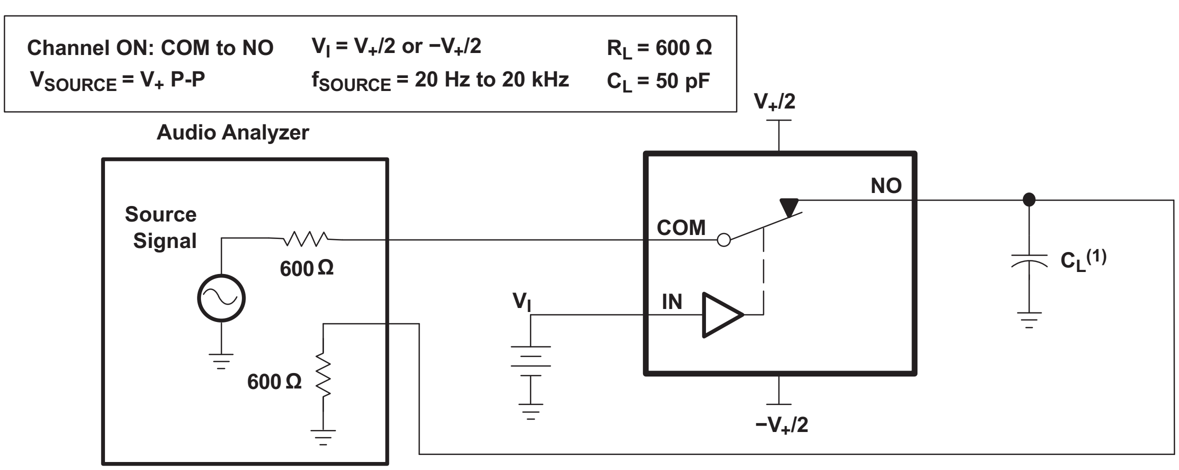
Figure 23. Crosstalk (X_{TALK})



(1) C_L includes probe and jig capacitance.

(2) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

Figure 24. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

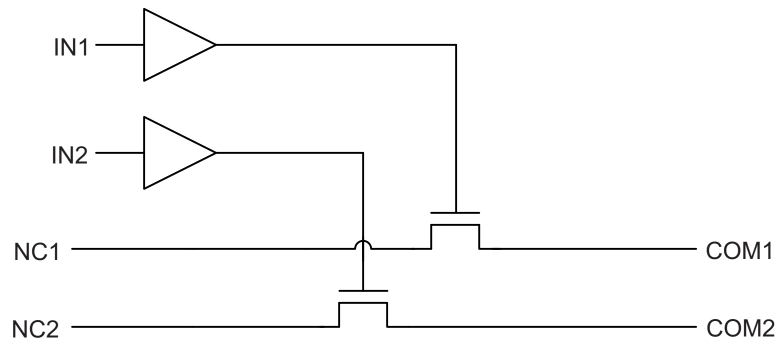
Figure 25. Total Harmonic Distortion (THD)

8 Detailed Description

8.1 Overview

The TS5A23167 is a dual single-pole single-throw (SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications. Table 2 shows the descriptions of each parameter specified in the datasheet.

8.2 Functional Block Diagram



8.3 Feature Description

Tolerant control inputs allow 5-V logic levels to be present on the IN pin at any value of V_{CC}. Low ON-resistance allows minimal signal distortion through device.

8.4 Device Functional Modes

Table 1 shows the functional modes for TS5A23167.

Table 1. Function Table

IN	NC TO COM, COM TO NC
L	ON
H	OFF

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS5A23167 dual SPST analog switch is a basic component that could be used in any electrical system design. One example application is a gain selector, which is described in the *Typical Application* section.

9.2 Typical Application

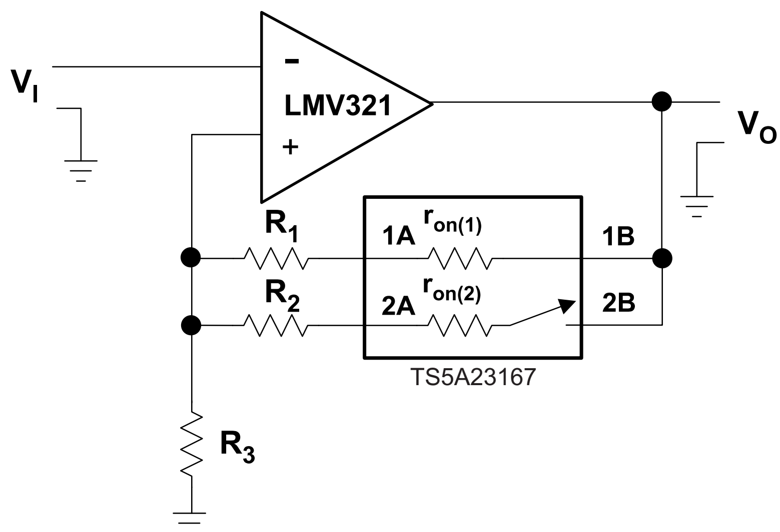


Figure 26. Gain-Control Circuit for OP Amplifier

9.2.1 Design Requirements

By selecting values of R1 and R2, such that Rx >> $r_{on(x)}$, r_{on} of TS5A23167 can be ignored. The gain of op amp can be calculated as follow:

$$Vo / VI = 1 + R|| / R3 \quad (1)$$

$$R|| = (R1+r_{on(1)}) || (R2+r_{on(2)}) \quad (2)$$

9.2.2 Detailed Design Procedure

Place a switch in series with the input of the op amp. Because the op amp input impedance is very large, a switch on $r_{on(1)}$ is irrelevant.

Typical Application (continued)

9.2.3 Application Curve

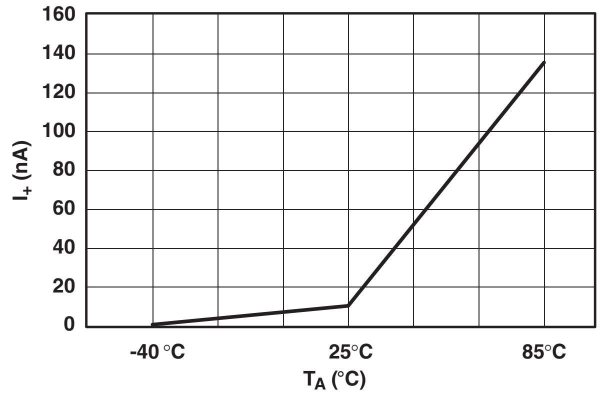


Figure 27. Power-Supply Current vs Temperature (V_+ = 5 V)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-µF or 0.022-µF capacitor is recommended for each V_{CC} because the VCC pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-µF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Figure 28 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

11.2 Layout Example

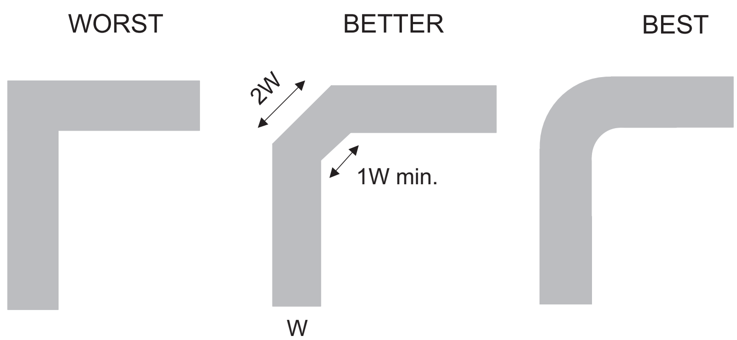


Figure 28. Trace Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

Table 2. Parameter Description

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
r_{on}	Resistance between COM and NC ports when the channel is ON
r_{peak}	Peak on-state resistance over a specified voltage range
$r_{on\Delta}$	Difference of r_{on} between channels in a specific device
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
$I_{NC(PWROFF)}$	Leakage current measured at the NC port during the power-down condition, $V_+ = 0$
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NC) in the OFF state under worst-case input and output conditions
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-down condition, $V_+ = 0$
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NC) in the ON state and the output (NC) open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_I	Voltage at the control input (IN)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NC) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NC) signal when the switch is turning OFF.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance, and ΔV_{COM} is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NC) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC) is ON
C_I	Capacitance of control input (IN)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an adjacent ON channel (NC1 to NC2). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A23167DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(JAPQ, JAPR)	Samples
TS5A23167DCURG4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAPR	Samples
TS5A23167YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	J8N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

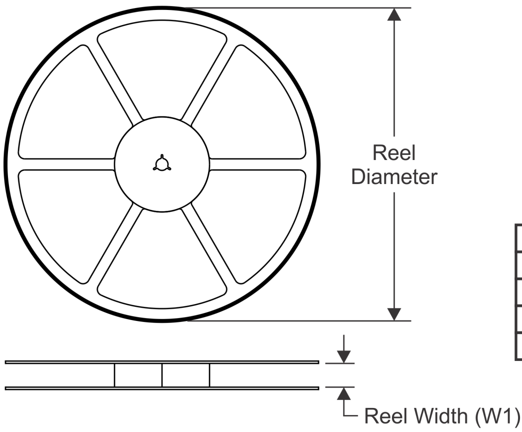
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

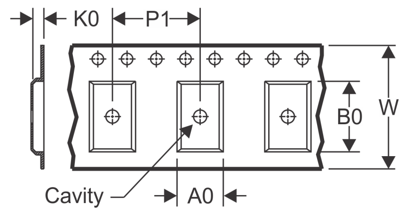
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

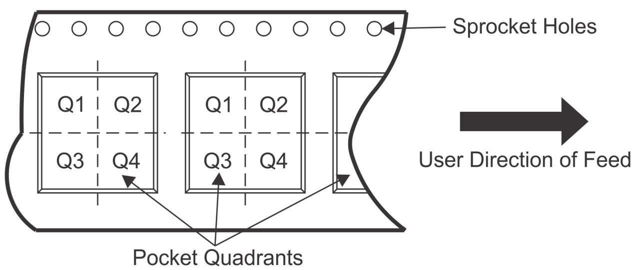


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

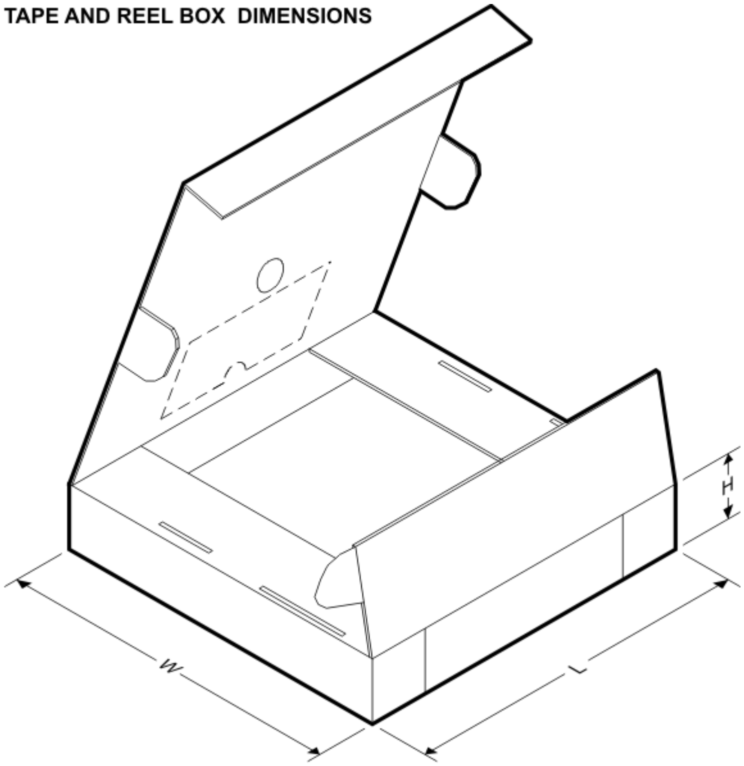
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

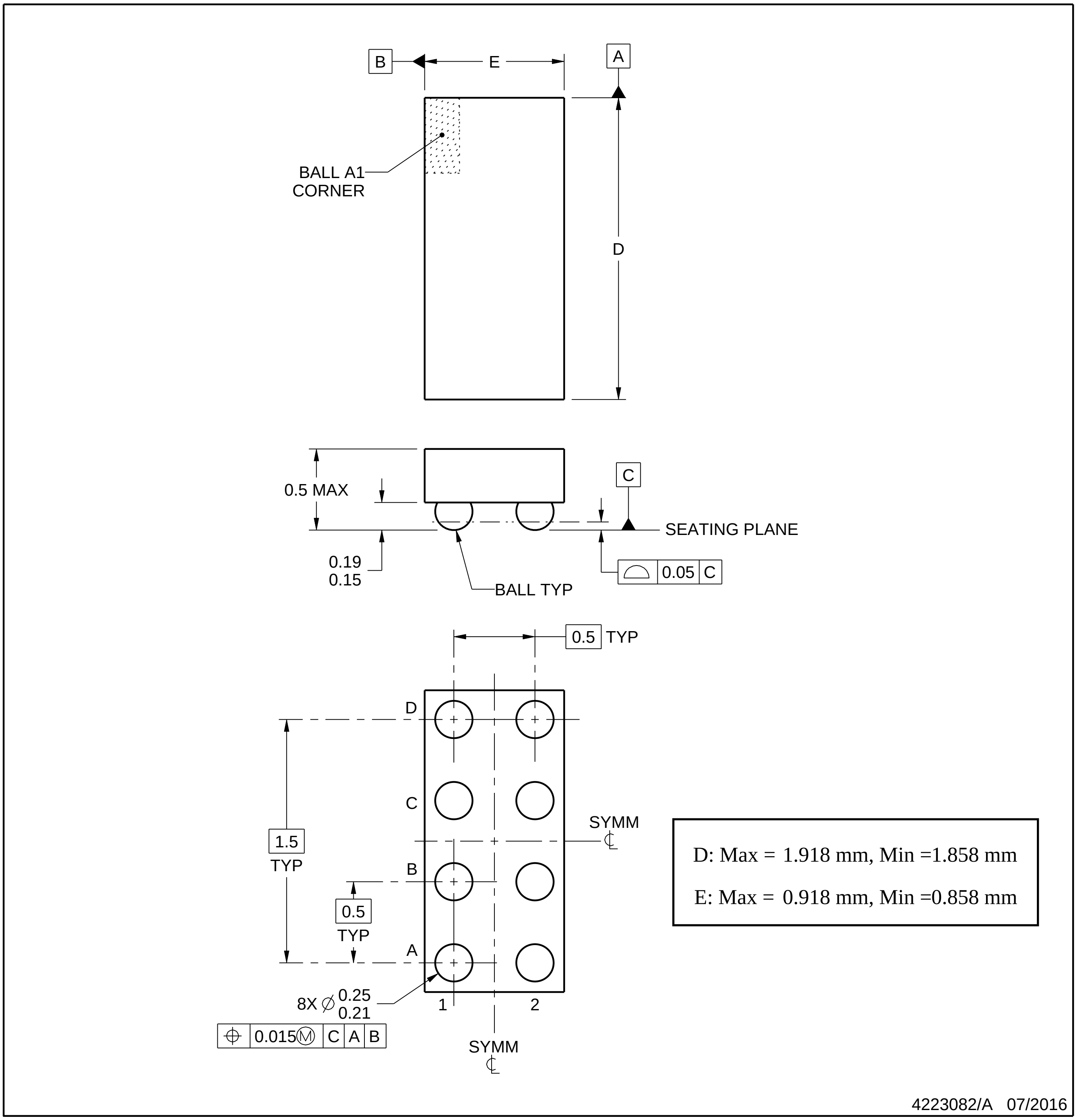
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A23167DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A23167DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A23167YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



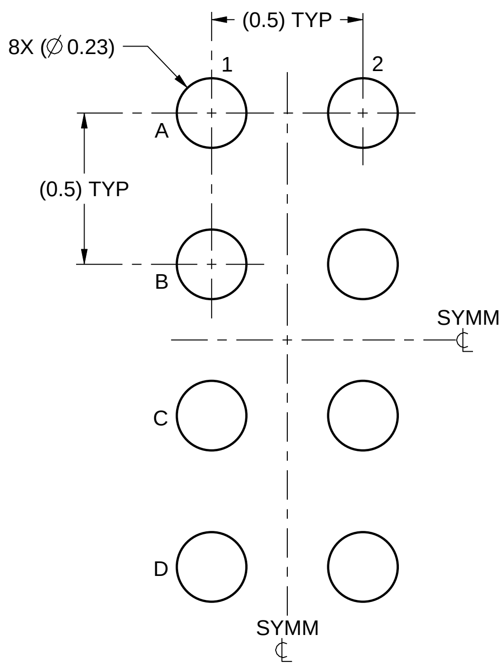
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A23167DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A23167DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A23167YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

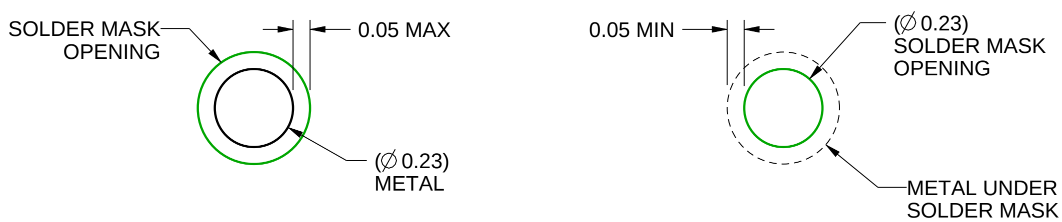


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X



NON-SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

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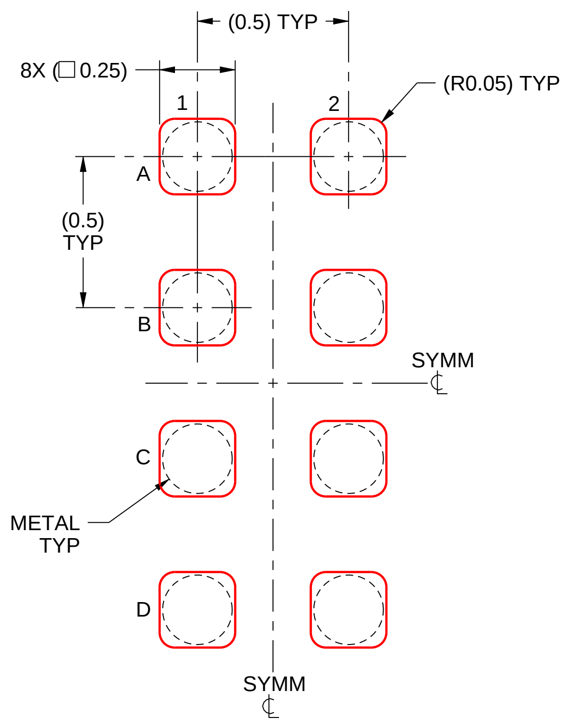
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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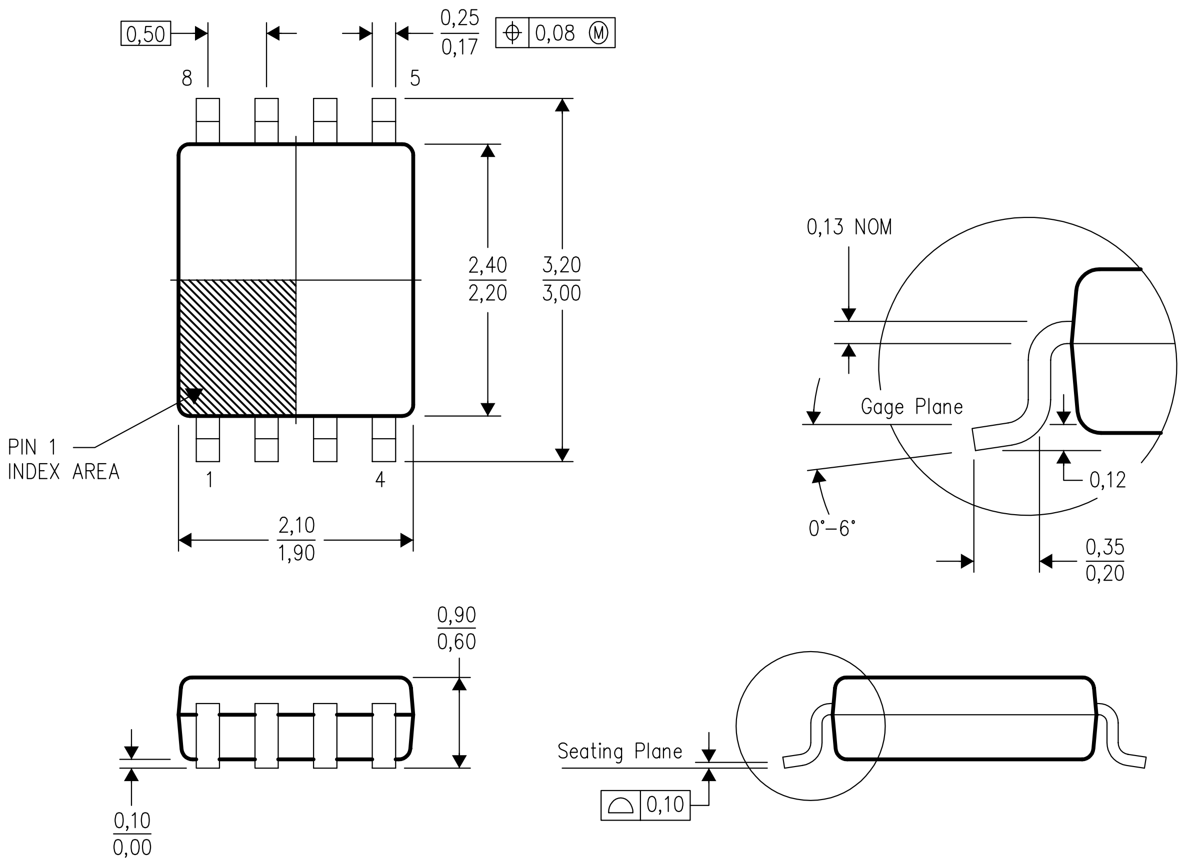
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

DCU (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



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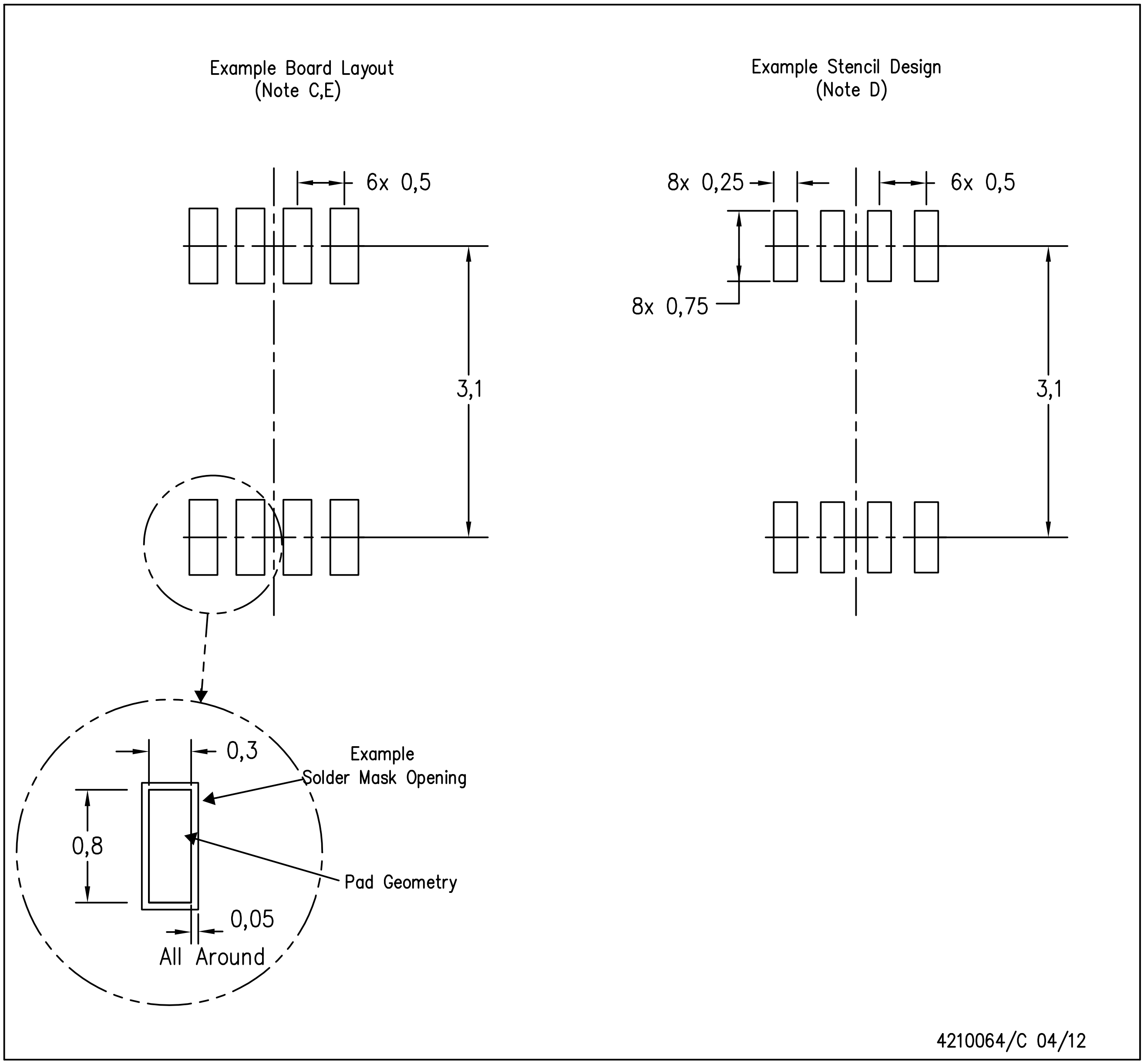
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.