Application Report
SLLA117 - July 2002

MIXED SIGNAL PRODUCTS
TI 1394 PRODUCTS

IEEE 1394 EMI Board Design and Layout Guidelines

Revision 1.1.3

Jose A. Cadena-Hernandez

Burke Henehan

Lee Myers

1 Introduction

Below are suggested EMI guidelines to follow when designing a 1394 board. These guidelines are in addition to the "Recommendations for PHY Layout" application note # SLLA020A. Not all must be followed, but rather they are suggestions. For example if you are designing a board that will go into a desktop PC, then more attention should be paid to keeping RF noise from coupling onto the traces that connect to the 1394 connector, since the 1394 cable is the most likely source for RF noise.

EMI has three elements to it:

- There is a source of energy.
- There is a receptor of this energy.
- There is a coupling path between the source and receptor to transfer the unwanted energy.

The main source of energy in a 1394 design comes from the high clock frequencies. Even though the twisted pairs are higher in frequency than the PHY SCLK (SCLK is the system clock that runs between the PHY and link devices), the signals that run on the twisted pair have less amplitude and are differential signals. The differential mode currents on the twisted pairs will generate magnetic fields that will cancel each other out. Whereas, SCLK has greater amplitude and is not a differential signal. The 1394 cable can behave as a monopole antenna and care should be taken to prevent RF currents from coupling onto the cable.

When designing a 1394 board the signals of most interest are:

a) The PHY-Link interface signals: SCLK has a fundamental of 49.152 MHz, D0-D7, CTL0, CTL1, LREQ - all have a maximum fundamental of 24.576 MHz, the LPS signal has a fundamental of ~1MHz, and the LKON signal has a fundamental of ~6.114 MHz
b) The power Lines going into and out of the cable: The 1394 connector socket pin1 (Bus Power) may be heavily filtered and need only pass low frequency signals of less than ~100 KHz; 1394 socket pin2 (analog ground) must be able to pass an approximately ~5MHz fundamental speed signal current and must be filtered sparingly.
c) The differential twisted pair signals going out on cable: TPA+, TPA-, TPB+, and TPB- all have a fundamental 49.152 MHz at S100 transfers; a fundamental of 98.304 MHz at S200; and a fundamental of 196.608 MHz at S400.
d) The external crystal circuit: 24.576 MHz fundamental.

The remainder of this document is broken up into two parts, Schematic recommendations and Layout recommendations.

2 Schematic recommendations

If galvanic isolation is not implemented, the cable connector sockets should be shorted directly to a small chassis ground plane (GND "strap") that exists immediately underneath the connector sockets. This is to short EMI (and ESD) directly to chassis ground before it gets onto the 1394 cable. This etch plane should be as fat as possible, but all the conductors coming off the connector pins 1 through 6 must have the board signal GND plane run under them (the PHY ground plane). If needed, scoop out the Chassis GND strap etch to allow for the PHY signal ground to extend under the connector pins. Note that the etches coming from pins 1 and 2 (V+ power and V- power) should be fat and via-ed to their respective planes (or fat etches) as soon as possible, respecting the filtering that may be in place between the connector pin and the plane. See Figure 1 below for a schematic example.

To address the PHY clock emissions on the PHY-Link interface, place a ~10 to 130 Ohms resistor in series with the PHY SCLK. Use a trial and error method of looking at the shape of the SCLK waveform on a high-speed oscilloscope and tuning the value of the resistance to minimize waveform distortion. The value on this resistor should be as small as possible to get the desired effect. This resistor should be placed close to the PHY. Series terminate the other PHY link interface signals with 10 to 130 Ohms resistors if needed. The SCLK signal is the most likely source of EMI, but signals immediately adjacent to SCLK are likely to be affected, most notably the LREQ signal, which should also have a series terminating resistance. A typical value of 51 Ohms seems to give good results.

To reduce the number of antennas, fix all DC inputs into PHY by connecting them to a power plane through a 1Kohm resistor or directly to a GND plane. Length of the traces should be kept as short as possible to reduce antenna lengths. This may be done for the: PC0, PC1, PC2, TESTM, SE, SM, /ISO, and PD pins.

Keep the 270 pF capacitor in the TPB termination network close to the PHY and as close as possible to the junction between the termination resistors; keep the 5 KOhm +/- 5% resistor in the TPB termination close to the junction between the termination resistors. On the TPA side termination network place a 270 pF cap as close as possible to the junction between the 56.2 Ohm resistors. Keep the 1 uF cap on the TPBIAS pin close to the junction between the termination resistors, hopefully next to the 270 pF cap. Use fat etches to connect the 1 uF cap to the mid-point of the termination resistors to reduce current noise during speed signaling. Select ceramic caps with a high frequency response.

Use a 10 pf load crystal with its corresponding lower value load capacitors on the PHY oscillator input XI and XO pins. For more details on crystal selection, refer to “Selection and Specification of Crystals for Texas Instruments IEEE 1394 Physical Layers” application note #SLLA051. Power is proportional to the current squared. The current is $I = C*dv/dt$, since dv/dt is a function of the PHY, current is proportional to the capacitive load. Cutting the load to 1/2 will decrease the current by 1/2 and the power to 1/4 the original value. Reducing this power should reduce the power of the emissions.

To keep EMI from getting onto the cable bus power wire (a very large antenna) a ferrite may be placed in series with cable bus power V+ near the 1394 connector pin 1. This ferrite may limit at low frequencies since V+ does not need to pass any high frequency signaling (V- pin 2 must pass speed signal current). The ferrite bead between connector pin 1 and bus power may be valued between 47 and approximately 1000 Ohms at 100 MHz. It should continue being resistive out to approximately 1 GHz. If the low end resistive value is chosen it may also be used for the 1394 connector pin 2 ferrite filter, however the connector pin 1 filter may be much more aggressive (high impedance). See Figure 1 and 2 below for a schematic example.

To keep EMI from getting onto the cable analog ground wire (a very large antenna) place a ferrite in series with the cable bus ground V- near to 1394 connector socket. Note that this ferrite must pass the speed signal current which has a fundamental of up to 5 MHz. The ferrite bead between connector pin 2 and PHY ground may be valued between 10 and 50 Ohms at 100 MHz. It should continue being resistive out to approximately 1 GHz. If the high-end resistive value is chosen it may also be used for the 1394 connector pin 1 ferrite filter. See Figure 1 and 2 below for a schematic example.

If a metal enclosure is not available in the system, to keep EMI from getting onto the cable shield (a very large antenna) a ferrite may be placed in between the connector socket shield (connector pins 7 & 8) and signal ground. This ferrite may limit at low frequencies since the shield does not need to pass any current. The ferrite bead may be valued between 47 and approximately 1000 Ohms at 100 MHz. It should continue being resistive out to approximately 1 GHz. If the low end resistive value is chosen it may also be used for the 1394 connector pin 2 ferrite filter. See Figure 2 below for a schematic example.

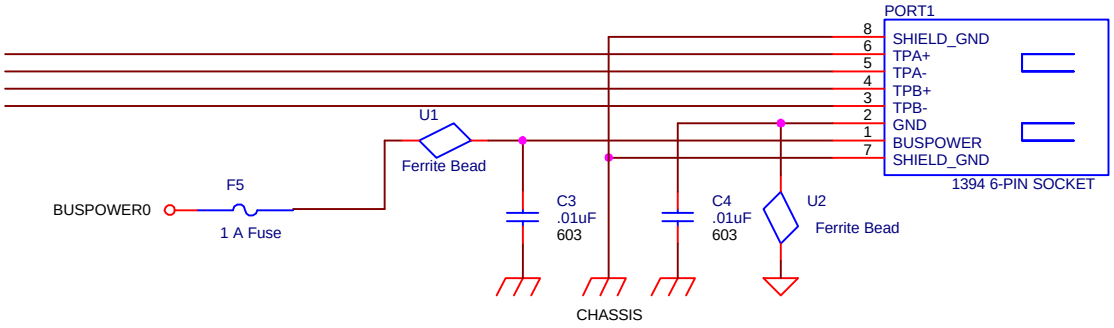


Figure 1. 1394 6-pin Socket Schematic Example when metallic chassis is available.

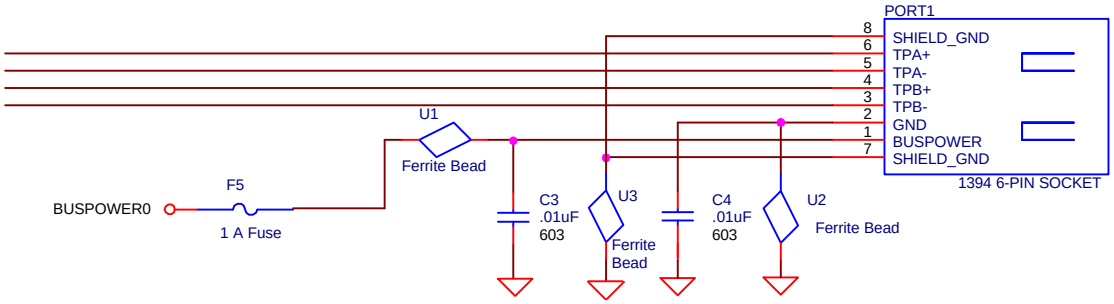


Figure 2. 1394 6-pin Socket Schematic Example when no metallic chassis is available.

When 4-pin connectors are used, to keep EMI from getting onto the cable shield (also PHY ground and a very large antenna) place a ferrite in series with the cable shield pins near to the 1394 connector socket. Note that this ferrite must pass the speed signal current which has a fundamental of up to 5 MHz. The ferrite bead between the 4-pin cable shield and PHY ground may be valued between 10 and 50 Ohms at 100 MHz. It should continue being resistive out to approximately 1 GHz. See Figure 3 below for a schematic example. It is recommended to use the 6-pin connectors whenever possible.

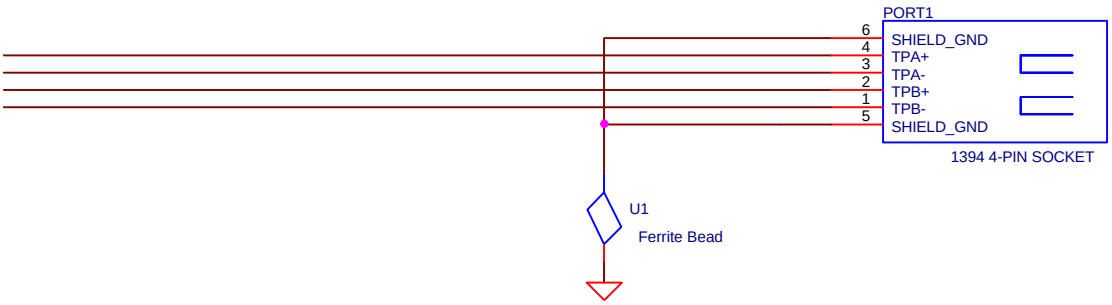
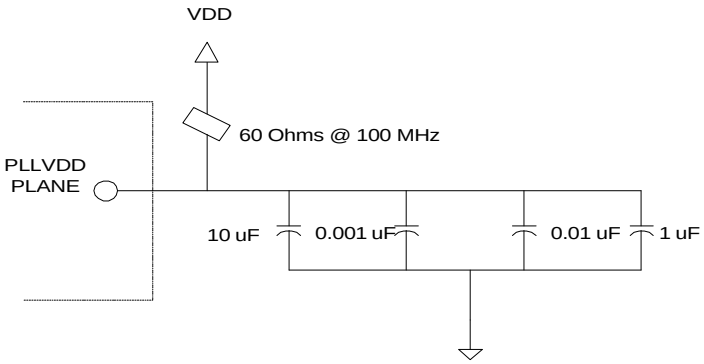


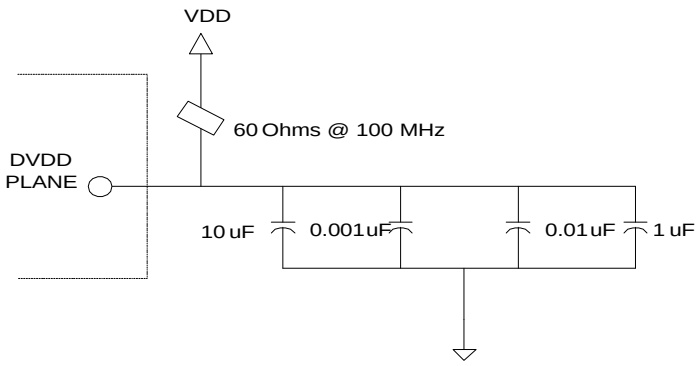
Figure 3. 1394 4-pin Socket Schematic Example.

2.1 PLLVDD and DVDD Filtering

Another means to minimize EMI emissions is to add decoupling capacitors with a ferrite bead at PLLVDD pin and DVDD pins of the chip. This array should be as close as possible to the chip in order to minimize the inductance of the line and minimize noise contributions to the system, a suggested example is shown in Figures 4(a) and 4(b). In the case of DVDD pins, it is recommended to tie them up to a single low impedance point in the board and then adding the decoupling capacitors in addition to the ferrite bead. This array of caps and ferrite bead improve EMI and Jitter performance. Both EMI and Jitter should be taken into account before altering the configuration.



(a)



(b)

Figure 4. Suggested Array at PLLVDD and DVDD in order to minimize EMI.

2.2 ESD/EMI Schematic recommendations

In order to have proper ESD/EMI performance, recommendations listed below should be considered:

1. Use a larger value cap on PHY /RESET to filter more ESD energy (0.33 uF or multiple 0.1 uF caps in parallel). Refer to device datasheet for /RESET timing specifications.
2. Use a 0.01 uF cap on each cable power V+ line to chassis GND near to the 1394 connector pin. See Figure 1 and 2.
3. Use a 0.001 uF cap on each cable power V- line to chassis GND next to the 1394 connector pin. See Figure 1 and 2.
4. Place a 0.01 uF cap on both input and output of each voltage regulator. This is to increase the immunity to ESD and reduce EMI.
5. Use a 10 KOhm resistor to 3.3V and 0.1 uF cap to signal GND on the global /RESET pin on the link layer.

3 Layout recommendations to improve EMI and ESD performance:

Put pads in for all components in prototype boards. When testing prototype boards for EMI and ESD, some of the following components may not be required:

1. The 1394 connector gasket between chassis GND, 1394 connector shield, and metal bracket on PCB board (for example on a PCI add-in card).
2. The ferrite on the cable V- ground pin (socket pin 2).
3. The ferrite on the cable V+ power pin (socket pin 1).

3.1 Board Stackup

Because of the high frequencies associated with 1394, a 1394 board with at least four layers is recommended; two signal layers separated by a ground and power layer (See Figure 5).

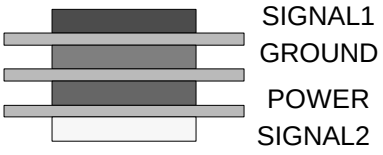


Figure 5. Four-layer board stackup.

The majority of signal traces should be run on a single layer, preferably SIGNAL1. Immediately next to this layer should be the GND plane which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used (see Section 3.3). Minimizing the number of signal vias could reduce EMI due to a reduction in inductance at high frequencies.

3.2 Digital and Analog Partitioning

If separate power planes are used, they must be tied together at one point through a low impedance bridge or preferably through a ferrite bead (See Figure 6). Care must be taken to capacitively de-couple each power rail close to the device.

The analog ground (AGND), digital ground (DGND), and Phase Locked Loop (PLL) ground (PLLGND) must be tied together to the low impedance circuit board ground plane.

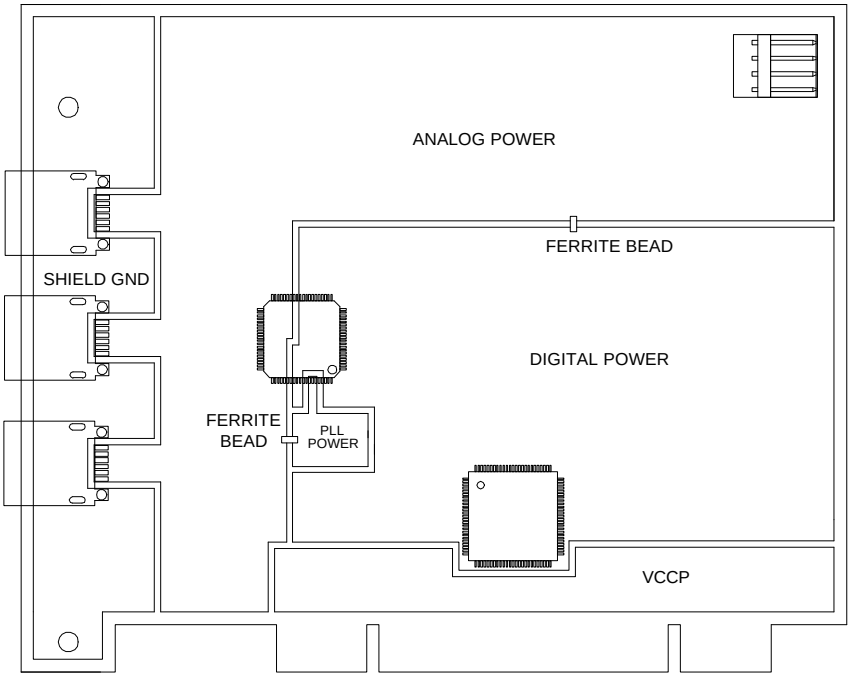


Figure 6. A image plane partition, route signal carefully.

3.3 Image Planes

An image plane is a layer of copper (voltage plane or ground plane), physically adjacent to a signal routing plane. Use of image planes provides a low impedance, shortest possible return path for RF currents. For a 1394 board the best image plane is the ground plane, since on most designs a common ground can be used for both analog and digital circuits. Care should be taken not to route traces such that they cross from one plane to the other, as this can cause a broken RF return path resulting in an EMI radiating loop (See Figure 7). This is important for higher frequency or repetitive signals. Therefore it is best to run all clock signals on the signal plane above a solid ground plane (on a multi-layer board). Avoid crossing the image power or ground plane boundaries with high speed clock signal traces immediately above or below the separated planes. This also holds true for the twisted pair signals (TPA, TPB). Special care should be applied to the LPS and LKON signals as these do not always route easily on a single layer.

Any unused area of the top and bottom signal layers of the PCB can be filled with copper that is connected to the ground plane through vias.

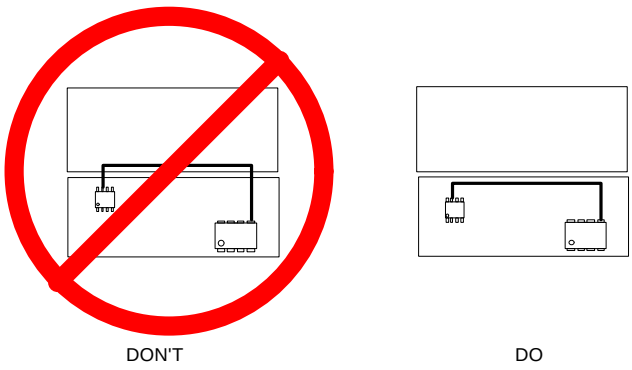


Figure 7. Do not cross image plane boundaries.

Care should also be taken not to overlap planes that do not reference each other. For example do not overlap a digital power plane with an analog power plane as this will produce a capacitance between the overlapping area which could pass RF emissions from one plane to the other. See Figure 8.

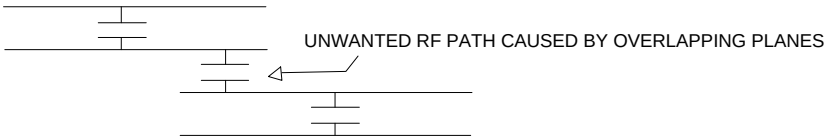


Figure 8. Do not overlap planes.

Avoid image plane violations. Traces that route over a slot in an image plane results in a possible RF return loop. See Figure 9.

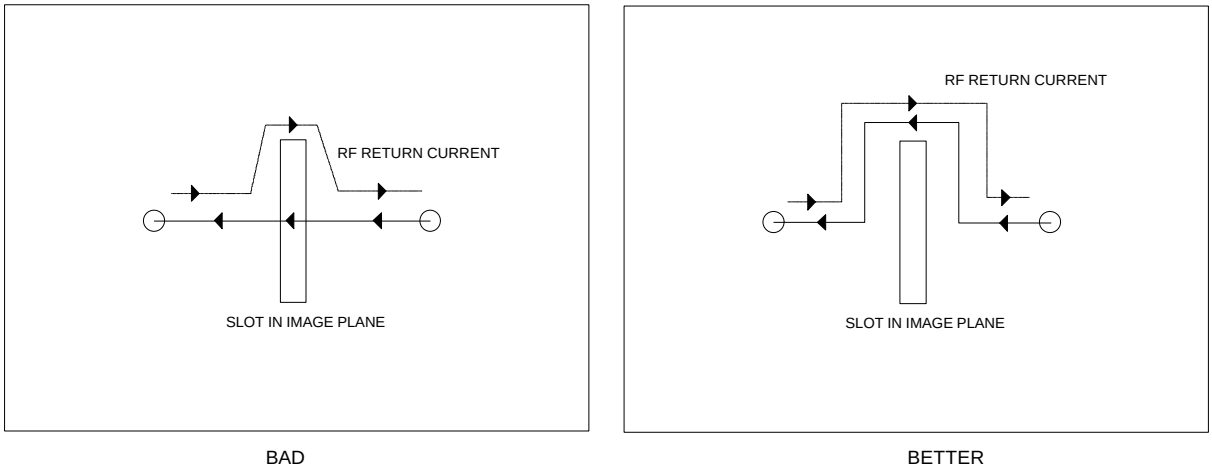


Figure 9. Do not violate image planes

3.4 Parts Placement

Components should be placed on the board such that the traces coming from a component will always be above its corresponding image plane. The PHY should also be placed close to the link to reduce the trace length of the PHY/link interface. For less radiated EMI, place the PHY device as far away from the 1394 connector (termination network should be close to the PHY) as is practical. Balance this against keeping the twisted pair trace lengths short (for signal integrity), keeping the PHY-Link interface traces short (for signal integrity and EMI) and keeping the PHY away from any switching power supply.

3.5 Decoupling Caps

Properly used decoupling caps keep RF energy from being injected into the power planes from high frequency components. Decoupling capacitors also provides a localized source of pulsed DC power for device or components. This reduces peak current surges from propagating across the board. Use 0.1uF and 0.001uF decoupling caps on the PHY and link (For PLLVDD see Section 2.1). Minimize the trace length between the decoupling capacitor and the corresponding power pins on the device. Also minimize the trace length from the capacitor pad to the power or ground plane. See Figure 10.

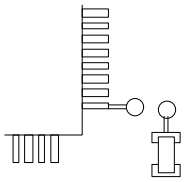


Figure 10. Decoupling Caps.

3.6 3W rule for SCLK

When routing the SCLK trace from the PHY to link, try to use the 3W spacing rule. The distance from the center of the SCLK trace to the center of any adjacent signal trace should be at least three times the width of the SCLK trace. SCLK is a 49.152 MHz clock with a fast rise time. Using the 3W rule will cut down on crosstalk between traces. In general, leave space between each of the traces running from the PHY to link. Avoid using right angles when routing traces to minimize the routing distance and impedance discontinuities.

For further protection from crosstalk, run guard traces beside the SCLK signal from PHY to Link (GND pin to GND pin if possible). This is to lessen clock signal coupling onto the other PHY-Link interface traces near it and thus radiating the clock signal from more antennas. See Figure 11.

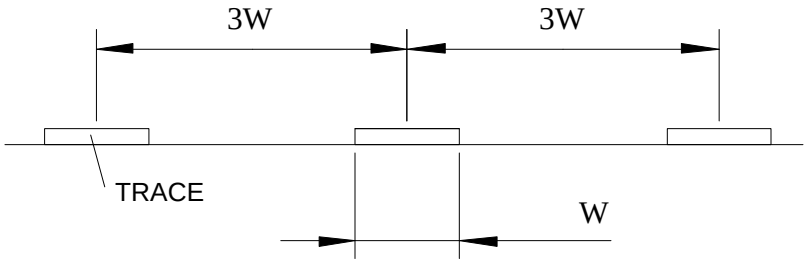


Figure 11. 3W Rule

4 Additional Considerations

Additional methods are available for reducing EMI emissions when the application uses a shielded chassis. Some manufacturers offer a metal bracket to fill the slot area between the 1394 connector and the chassis. Other means to achieve a similar effect is to use a conductive spacer or metal fingers. Some companies offer 1394 connectors with back shield for PCB. For additional information see the presentation “Industrial 1394 PWB Design” on the 1394 Trade Association’s web site (member’s only section) or contact TI.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265