TSB81BA3 Silicon Errata

This document contains corrections and additions to the following device data sheets: TSB81BA3 (TI Literature Number SLLS559) and TSB81BA3-EP (TI Literature Number SGLS194).

SILICON ERRATA ID	PROBLEM DESCRIPTION	RESOLUTION / WORK-AROUNDS
1. S800β jitter	Symptom The TSB81BA3 device does not meet all the jitter requirements specified for S800 operation in IEEE Std1394b-2002 tables 9-12 and 9-13.	The TSB81BA3 meets or exceeds the recommended IEEE Std 1394b-2002 corrections by the 1394 Trade Association. Refer to 1394TA Document *TB2002001 Technical Bulletin 1394b Clarifications and Errata*, Draft 1.6:107, July 11, 2003, §9.7.1, Tables 9-12 and 9-13.
2. BOSS arbitration issue	Symptom A bus-reset may occur in certain topologies when 1394b BOSS arbitration is in use. Occurrences This issue is only possible if three or more BOSS-arbitration capable nodes are connected through a 1394b connection. To be BOSS-arbitration capable a node must have a 1394b PHY and a 1394b Link using the 1394b PHY-Link interface connection. If a narrow timing window is violated (dependent on cable lengths and/or mixed speed bus hops) a middle node may detect a packet collision, causing a PHY state timeout. The state timeout causes a bus reset. Repetitive occurrences result in repetitive bus resets. Example Topologies A. Mixing short and long cable lengths. A BOSS arbitration issue may occur in the middle node. Figure 1 shows an example topology that would exhibit the condition.	A. Use one or more 1394a link-layer controllers (LLCs). If the network only consists of nodes using 1394a link layers, then BOSS arbitration is not utilized; Gap_Count delays are maintained and therefore nodes are not affected by this errata. B. In nodes that do not have a link, disable BOSS arbitration (e.g., force the BMODE pin to the logic 0 state). C. Use a topology where all nodes use the same 1394a compatible bus speed (e.g., S400) and at least one IEEE Std 1394a-2000 node is present. D. Use a topology where all 1394B nodes are at the same 1394b bus speed, using matched cable lengths between 1M and 4.5M.

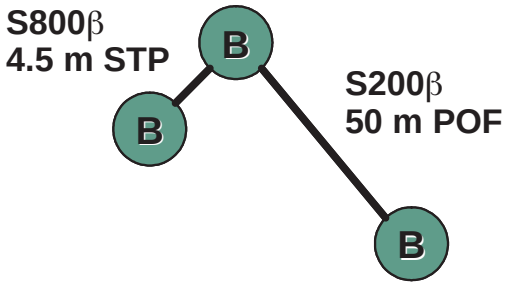

Figure 1. BOSS Arbitration Issue Caused By Mixed Cable Lengths

SILICON ERRATA ID	PROBLEM DESCRIPTION	RESOLUTION / WORK-AROUNDS
2. BOSS arbitration issue (continued)	Example Topologies (continued) B. Mixing bus hop speeds. Either transition node (B_T) may have a BOSS arbitration issue. See Figure 2.	

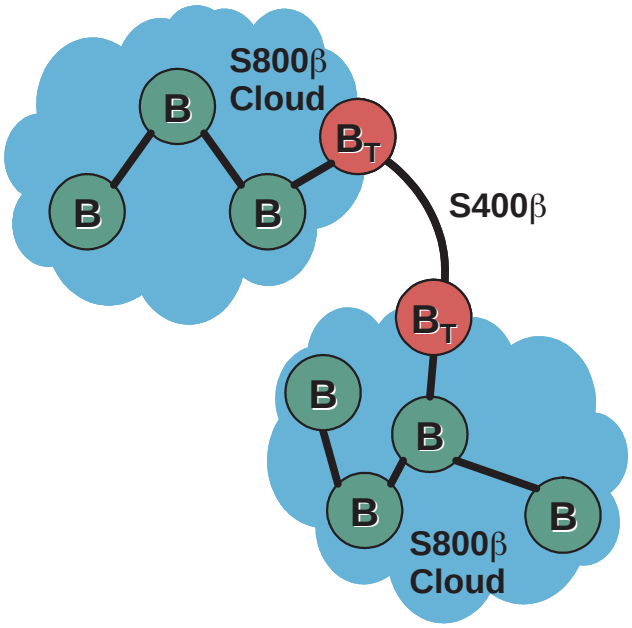

Figure 2. BOSS Arbitration Issue Caused By Mixed Bus Hop Speeds

SILICON ERRATA ID	PROBLEM DESCRIPTION	RESOLUTION / WORK-AROUNDS
2. BOSS arbitration issue (continued)	Detailed Example Situation See Figure 3. 1. Node #2 transmits a high-speed packet that ends an Async subaction or the Isoch period. 2. Node #2 advances the Async phase (no requests pending for the current phase). 3. Node #0 has a bus request pending for the new phase. 4. Node #2 sends an Async grant. 5. The Async grant is forwarded through a senior node (Node #1) and down through a junior connection to Node #0. 6. If a narrow timing window is violated the middle node (Node #1) will detect a packet collision, causing a state-timeout while forwarding the grant to the next node. The state-timeout will cause a bus reset.	

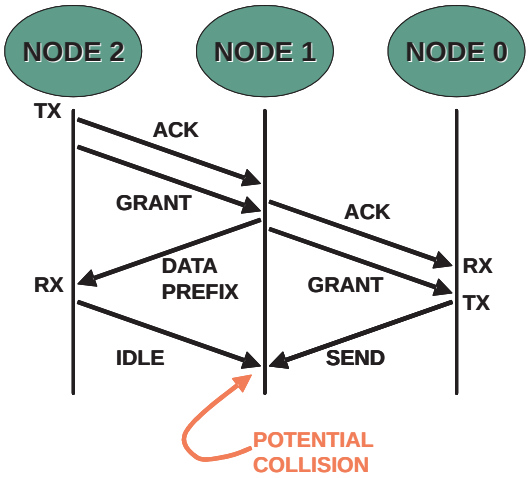

Figure 3. BOSS Arbitration Issue—Detailed Example Situation

SILICON ERRATA ID	PROBLEM DESCRIPTION	RESOLUTION / WORK-AROUNDS
3. Missing subaction gap issue	When nonroot 1394b nodes request transactions and do not receive an Ack (missing-Ack timeout occurs) the 1394b link layer is only sent an arbitration reset gap indicator rather than a both the Subaction gap and arbitration reset gap indicators. Some LLC hang if the Subaction gap indicator is not received.	Instruct the LLC to use 1394a mode for the PHY-Link interface.
4. Cycle start concatenation issue	When the PHY-Link interface is in the 1394a mode (BMODE terminal is logic 0) cycle start concatenation only works at S100. Furthermore, only one Isoch packet per Iso interval is allowed unless all Isoch packets are S100.	Configure the LLC to only transmit one Isoch packet per Iso interval and do one (or both) of the following: A. Disable cycle-start packet concatenation in the LLC. B. Clear the EAA and EMC CFR register bits in the TSB81BA3. These bits are cleared by chip reset (default).
5. 1394b Loop Prevention algorithm may cause bus resets in early production devices	Symptom The TSB81BA3 may cause bus resets during its 1394b mode loop prevention algorithm. This is a result of a Loop-test packet (LTP) collision with a cycle start packet or other 1394b subaction transaction completion, causing slow loop detection processing. Although the bus resets will eventually stop, multiple bus resets may occur. Occurrences This issue only occurs in early production devices. These devices are identified in software by reading the Product_ID from the TSB81BA3 vendor identification registers. Problem devices have a Product_ID of 83_13_01h. Good devices, with a Product_ID of 83_13_04h (or greater) do not have this issue.	Software must tolerate multiple bus resets spaced closely together. Software must wait until the bus reset process is complete (receipt of a subaction gap status) prior to enabling cycle master processing or queuing packet requests.
6. Legacy node maximum speed incorrectly reported in early production devices	Symptom The TSB81BA3 incorrectly calculates the *Max Legacy SPD* value (stored in the base register configuration area) if another device on the bus has four or more ports and is a lower node number. Occurrences This issue only occurs in early production devices. These devices are identified in software by reading the Product_ID from the TSB81BA3 vendor identification registers. Problem devices (early production) have a Product_ID of 83_13_01h. Good devices, with a Product_ID of 83_13_04h (or greater) do not have this issue.	The *Max_legacy_path_speed* field is a new CFR addition in the IEEE Std 1394b-2002. It is strongly recommended that software not utilize this register field but rather determine node speeds by a try-and-see method. In this method legacy packets are sent at the fastest speed and then at successively slower speeds until success or failure is determined.
7. Disappearing IDLE in a Beta system	Symptom In Beta systems with more than four cable hops, unwanted bus resets may occur. Cause A short IDLE between a data packet and an arbitration grant disappears. As signals propagate across the 1394 network, the IDLE between a data packet and an arbitration grant shortens since the time needed to repeat a data packet is longer than the time needed to repeat a grant.	A. Force all 1394B connections to S400B and add a 1394A PHY to the system to force legacy gap timing on the 1394 bus. B. Add a 1394A connection every fifth cable hop in the system.

DATA SHEET ERRATA ID	PROBLEM DESCRIPTION	RESOLUTION / WORK-AROUNDS
8. Incorrect PHY repeater delay	Table 1 and Table 2 in the data sheet give the PHY repeater *Delay* parameter as 144 + (delay x 20) ns and the *Delay* field as 0000b. The correct *Delay* field listing should be 4b'0010 (02h). The *Delay* field is the repeater delay for the S400β case, which is slower than the S800β or 1394a cases. Since the IEEE 1394b-2002 std PHY register set only has a single field for the delay parameter, the slowest value is used. If a network only uses S800β connections, only 1394a connections, or only a combination of S800β and 1394a connections, then the *Delay* value that may be used is 4b'0000 (00h). The worst-case PHY repeater delay is 197 ns and 127 ns for S400β and S800β cable speeds (i.e., trained, raw bit rate speed), respectively.	System designers may need to evaluate overall packet transfer time from worst-case nodes. Star or Hub approaches are usually within design timeout limits.
9. Power-up reset formula is incorrect	The *power-up reset* section passive capacitor formula is incorrect. The correct formula is: C_{MIN} = (0.0077 x T) + 0.085 + (external_oscillator_start-up_time x 0.05)	If a fundamental mode crystal is used rather than an oscillator then the start-up_time parameter may be set to 0. The RESETz must be asserted for 2 ms once the device power is at its minimum level and the input clock is valid. As an example, if the power ramp is 2 ms and the oscillator startup time is 2 ms then: C_{MIN} = (0.0077 x 2)+0.085+(2 x 0.05) = ~0.2 μF
10. Incorrect Product_ID	Table 6, *Page 1 (Vendor ID) Register Field Descriptions,* gives an incorrect value for the Product_ID field. The correct Product_ID is 83_13_04h or greater. The correct Product_ID for early production parts is 83_13_01h.	
11. Beta mode V_{OD} and V_{CM} omission	The TSB81BA3 *electrical characteristics over recommended ranges of operating conditions* section omitted the IEEE Std 1394b-2002 beta mode differential output voltage (V_{OD}, 700 mV typical) and the beta common mode voltage (V_{CM}, 1.5 V typical).	
12. Power dissipation	The TSB81BA3 *electrical characteristics over recommended ranges of operating conditions*, the *device* section omitted the supply current when the TSB81BA3 is in the low-power/suspend state. When in this state the supply currents are: I_{DD}, Supply current 3.3V_{DD} is 4 mA (typical) I_{DD}, Supply current 1.8V_{DD} is 3 mA (typical)§ §The low-power/suspend state current consumption assumes the device is not receiving packets, and it is toning. The typical device operating power consumption and the typical low-power/suspend state power consumption is, respectively, P_D = (120 mA x 3.3 V) + (79 mA x 1.8 V) = 539 mW P_{D-LP} = (4 mA x 3.3 V) + (3 mA x 1.8 V) = 19 mW	
13. Dissipation rating table correction	The third row in the *Dissipation Rating Table* should be removed. Only the 5.05 W and 3.05 W (T_A = 25°C) rows are valid.	

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14. PowerPAD recommendation	Figure 9, *Example of a Thermal Land for the TSB81BA3 PHY,* should show thermal vias.	It is required that the TSB81BA3 uses a thermal land under its PowerPAD unless an external heatsink is used. It is strongly recommended that the thermal land be soldered to the PowerPAD. The recommended thermal land size is 10mm x 10mm with 36 thermal vias (6 x 6 array, 13-mil drill plated with no thermal web reliefs). Refer to TI Application Note SLMA002 for more information on PowerPAD enhanced packages.
15. 1394b cable grounding	Figure 4, *Typical TP Cable Connections*, does not clearly state the ground connections. IEEE Std 1394b-2002 Beta cables have individual ground return paths for the TPA and TPB signal pairs, plus a ground return for power and an outer shield.	System designers must ensure the power ground return and the TPB ground return are shorted on the PCB. The TPA ground return is isolated from the TPB ground by the parallel combination of 0.1-μF capacitor and a 1-MΩ resistor.

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