Application Report
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TUSB1002A Configuration Guidelines

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ABSTRACT

The TUSB1002A is a dual-channel USB 3.2 x1 10 Gbps SuperSpeedPlus Linear redriver. Signal integrity issues place additional limitations on system trace length at these high data rates. The TUSB1002A provides several levels of receive linear equalization to compensate for cable and board loss due to inter-symbol interference (ISI). This document is intended to provide general guidelines on how to use the TUSB1002A in a Host (Source) application. The TUSB1002A can also be used in a Device (Sink) application using these same guidelines.

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Trademarks

1 Introduction

The TUSB1002A is a dual-channel USB 3.2 x1 SuperSpeedPlus redriver that can be used for in a Host or Device application. The USB signal amplitude is attenuated through a typical FR4 channel. A longer channel with large attenuation can result in signal integrity issues at a USB 3.2 receiver. The TUSB1002A is used to eliminate or minimize the attenuation effects of the channel to produce a compatible eye at the device receiver. The TUSB1002A can be configured with 16 receiver equalization settings along with 3 voltage output linear ranges and additional DB Gain adjustment settings..

2 Equalization Selection

The TUSB1002A used in a Host or Device application enables the system to pass USB 3.2 Gen 1 or Gen 2 transmitter electrical and receiver jitter tolerance compliance testing. The TUSB1002A recovers incoming data by applying equalization that compensates for channel loss, typical FR4 channel loss is given in Table 2. The equalization should be based on the amount of insertion loss of the channel before the TUSB1002A receiver (Pre-Channel). The EQ value of each channel is set independently, the equalization selection is configured through the CH[2:1]_EQ[2:1] pins. The equalization values available for the TUSB1002A are detailed in Table 1.

Table 1. TUSB1002A Equalization

EQ SETTING No.	CHx_EQ2 PIN LEVEL	CHx_EQ1 PIN LEVEL	EQ GAIN at 2.5 GHz (dB)	EQ GAIN at 5 GHz (dB)
1	0	0	1.0	3.6
2	0	R	2.1	5.5
3	0	F	3.0	6.8
4	0	1	4.0	8.1
5	R	0	4.6	9.0
6	R	R	5.5	10.0
7	R	F	6.2	10.8
8	R	1	6.9	11.6
9	F	0	7.3	11.9
10	F	R	7.9	12.6
11	F	F	8.4	13.1
12	F	1	9.0	13.7
13	1	0	9.4	14.1
14	1	R	9.9	14.6
15	1	F	10.3	14.9
16	1	1	10.7	15.3

Table 2. Example FR4 Trace Loss

FR4 PCB Trace Length (Inches)	Loss at 2.5 GHz (dB)	Loss at 5 GHz (dB)
1	0.5	0.9
2	1	1.7
3	1.5	2.6
4	2	3.5
5	2.5	4.3
6	2.9	5.2
7	3.4	6.1
8	3.9	7
9	4.4	7.8
10	4.9	8.7
11	5.4	9.6
12	5.9	10.4
13	6.4	11.3
14	6.9	12.2

3 VOD Linear Range and DC Gain

The TUSB1002A supports different levels of linear range and DC Gain. For best performance, the TUSB1002A should operate within its defined VOD linear range. The gain of the incoming VID signal should be less than or equal to the TUSB1002A VOD linear range setting. Operating the TUSB1002A outside of the VOD linear range can result in additional jitter.

The DC Gain can be adjusted from -1 dB up to +2 dB in select combinations with VOD Linear range. In general, there are three cases to adjust DC Gain:

1. Input VID too high resulting in VOD higher than the USB 3.2 specification allows. In this case, a negative DC gain should be used.
2. Input VID too low resulting in VOD lower than the USB 3.2 specification allows. In this case, a higher DC Gain should be used.
3. Low frequency discontinuities resulting in DC components clipping the vertical eye mask. In this case, a higher DC Gain should be used.

The CFG1 and CFG2 pins of the TUSB1002A are used to configure the VOD and DC Gain of the device. VOD Linear range and DC Gain are defined in Table 3. In addition, the DCBOOST# pin when asserted can provide an additional +1 dB of gain up to +2 dB.

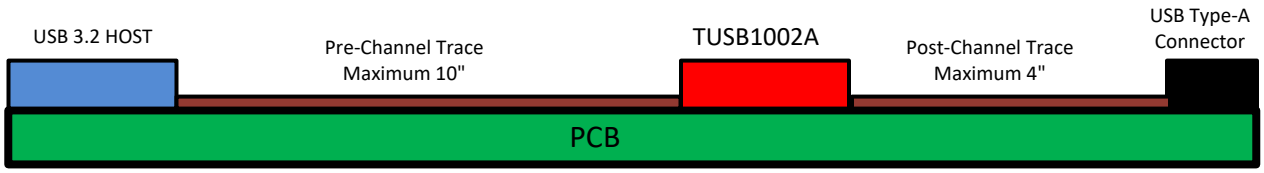
Table 3. VOD Linear Range and DC Gain

SETTING No.	CFG1 PIN LEVEL	CFG2 PIN LEVEL	CH1 DC GAIN (dB)	CH2 DC GAIN (dB)	CH1 VOD LINEAR RANGE (mVpp)	CH2 VOD LINEAR RANGE (mVpp)
1	0	0	+1	0	900	900
2	0	R	0	+1	900	900
3	0	F	0	0	900	900
4	0	1	+1	+1	900	900
5	R	0	0	0	1000	1000
6	R	R	+1	0	1000	1000
7	R	F	0	-1	1000	1000
8	R	1	+2	+2	1000	1000
9	F	0	-1	-1	1000	1000
10	F	R	+2	+2	1000	1000
11	F	F	0	0	1200	1200
12	F	1	+1	+1	1200	1200
13	1	0	+2	0	1200	1200
14	1	R	0	+2	1200	1200
15	1	F	0	+1	1200	1200
16	1	1	+1	0	1200	1200

4 TUSB1002A Placement

Closely following the layout guidelines listed in this document can enable the TUSB1002A to recover a signal from a Host or Device up to a typical 10" FR4 trace. In addition, the FR4 trace from the TUSB1002A to the USB connector can be up to 4". These recommended maximum trace lengths assumes the Host/Device provides -3 dB of de-emphasis and has a compliant receiver that can recover the 14.5dB loss budgeted by the USBIF for cable + Host/Device. By adjusting the equalization, de-emphasis and VOD settings of a Host/Device, these maximum trace lengths could possibly be extended. The engineer should work with the Host/Device manufacturer to determine optimal settings. Conversely, if a Host/Device cannot recover the signal with the amount of budgeted loss set by the USBIF, then concessions may be required in the system design such as placement of the Host/Device.

Figure 1. TUSB1002A Maximum Trace Length Placement Example



5 TUSB1002A Configuration Example

Figure 2 provides an example configuration of a host system using a USB3.2 Gen 2 Host operating at 10 Gbps with the TUSB1002A.

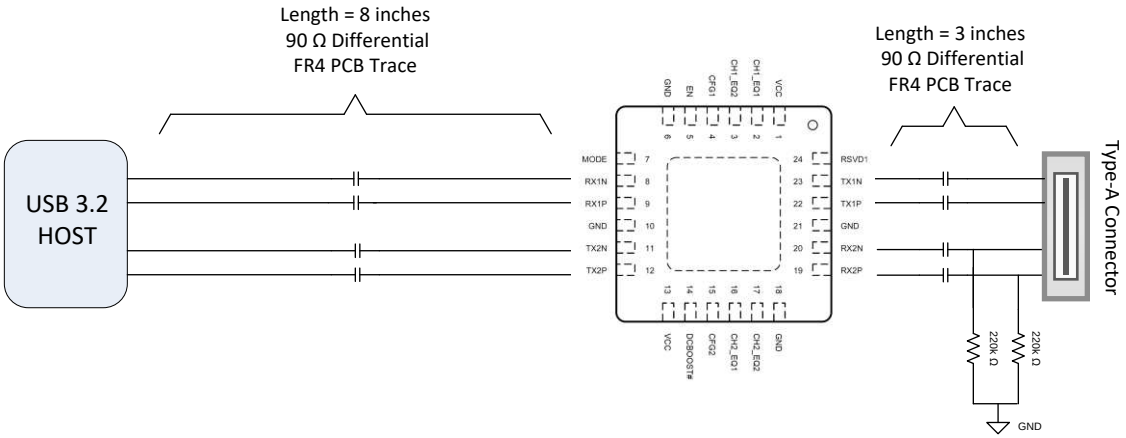


Figure 2. Host System Example

Using the given trace lengths in this example, the method to select the equalization values for RX1 and RX2 is to select the closest EQ gain available to match the trace loss + additional loss through the connector, components and device package:

- USB Host to TUSB1002A RX1 = 8 inches (-7 dB) + typical loss in Host package + capacitor (-1.5 dB) = total loss of -8.5 dB. TUSB1002A RX1 setting used = Setting #4 (8.1 dB).
- Type-A connector to TUSB1002A RX2 = 3 inches (-2.6 dB) + typical connector loss + component (-2 dB) = total loss of -4.6 dB. TUSB1002A RX2 setting used = Setting #2 (5.5 dB).
- VOD and DC Gain for CH1 and CH2 = Setting #5 (1000 mV, 0 dB). These values to be adjusted based on VID input to TUSB1002A RX1 and RX2.

Please note that other factors such as the layout quality, Host driver and receiver quality may require the EQ settings to be adjusted higher or lower for best performance. The aove method should be used for selecting initial configuration values based on system board trace lengths.

6 Layout Guidelines

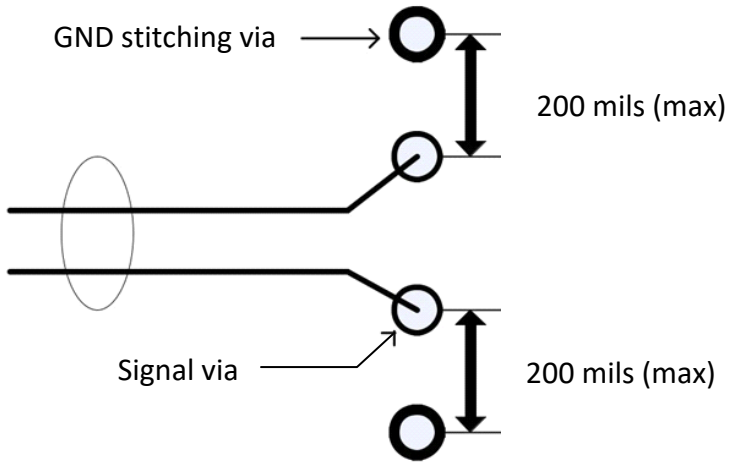
The following layout guidelines should be used in routing the high-speed USB signals to and from the TUSB1002A.

- RXP/N and TXP/N pairs should be routed with controlled 90-Ω differential impedance (±15%).
- Keep differential pairs away from other high-speed signals.
- Intra-pair routing should be kept to within 2 mils.
- Differential pair length matching should be near the location of mismatch.
- Each pair should be separated by at least 3x the signal trace width.
- The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135º. This will minimize any length mismatch caused by the bends and minimize the impact bends have on EMI.
- Route all differential pairs on the same layer.
- Minimize the number of vias, it is recommended to keep the via count to 2 or less.
- Keep differential traces on layers adjacent to a ground plane.
- Do not route differential pairs over any split plane.
- If using a through-hole connector, route the high-speed signals on opposite side of the connector such that the connector pin does not create a stub in the transmission line.

6.1 GND Stitching

The entirety of any high-speed signal trace should maintain the same GND reference plane from origination to termination. If the same GND reference plane is not maintained, via-stitch both GND planes together to ensure continuous grounding and uniform impedance. Place these stitching vias symmetrically within 200 mils (Center-to-center, closer is better) of the signal transition vias. See Figure 3 for an example of GND stitching vias.

Figure 3. GND Stitching Via Example



6.2 AC Coupling and Resistor Placement

When placing AC-Coupling capacitors, the maximum component size used should be 0402. During layout, on the Host/Device channel, the AC-Coupling capacitors should be placed equidistant to the Host/Device and the TUSB1002. On the connector to TUSB1002A channel, the AC Coupling caps should be placed close to the TUSB1002A with symmetrical placement to ensure optimum signal quality and to minimize reflections. The optional pull-down resistors should be placed such that the pad of the resistor shares the high-speed trace to minimize the presence of a stub. See Figure 4 for example placement and Figure 5 for AC Coupling capacitor layout symmetry.

Figure 4. TUSB1002A Layout Example

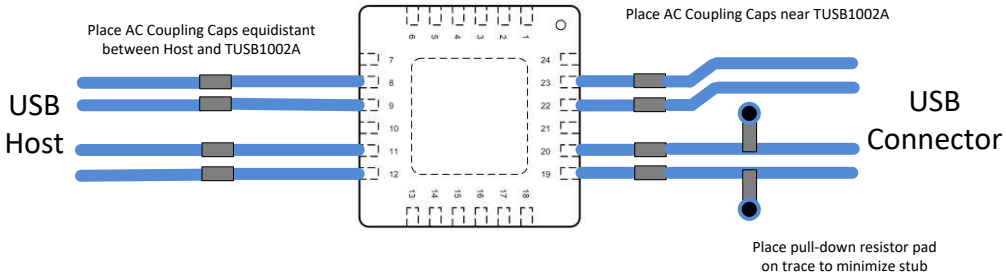
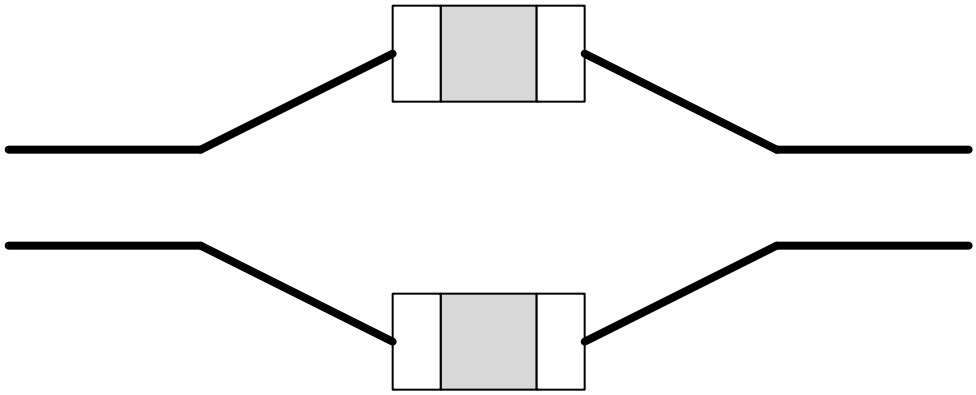


Figure 5. AC Coupling Layout Symmetry



NOTE: Adding test points to the high-speed traces can cause impedance discontinuity which negatively impacts signal performance and is not recommended. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair.

7 References

- Datasheet: TUSB1002A USB3.2 10 Gbps Dual-Channel Linear Redriver

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