Application Report
SLLA395–April 2018

TUSB215 Schematic Checklist

Malik Barton

ABSTRACT

This application notes for the TUSB215, a USB High-Speed (HS) signal conditioner, designed to compensate for ISI signal loss in a transmission channel which helps passing USB electrical compliance tests. TUSB215 is agnostic to USB Low Speed (LS) and Full Speed (FS) signals while USB High Speed (HS) signals are compensated. TUSB215 further acts as Charging Downstream Port (CDP) controller and handles the necessary handshakes with the downstream device. This schematic checklist provides a brief explanation of each device pin and the recommended configuration of the device pin for default operation. Use this information to check the connectivity for each TUSB215 on a system schematic.

This document is intended to aid design on the system level for general applications but should not be the only resource used. In addition to this list, customers are advised to use the information in the TUSB215 datasheet, TUSB215 EVM user's guide and associated documents to gain a full understanding of device functionality. Project collateral discussed in this application report can be downloaded from the following URL: www.ti.com/lit/zip/SLLA395.

NOTE: This device needs to have its thermal pad connected to ground for RGY packages.

1 TUSB215 Schematic Checklist

Table 1. TUSB215 Schematic Checklist

Pin Name	Pin Number	Pin Description	Recommendation
VCC	12	5 -V power	Parallel array of 1 µF and 0.1 µF capacitors on VCC to GND
VREG	8	1.8-V LDO output.	Connect a 0.1 µF capacitor between VREG and GND
GND	7	Ground	GND must be connected to GROUND
RSTN	14	Device disable/enable.	Connect a 0.1 µF capacitor between RSTN and GND. A second option is to control this pin externally. The device should not be enabled until the power on ramp has settled to 3 V or higher to ensure a correct power on reset of the digital circuitry.
EQ	1	USB High Speed boost select via external pull down resistor. Sampled upon power up, no real time changes.	PD resistor connected to the EQ pin, the value options are 160 W (max), 1.4 - 2 KΩ, 3.7 - 3.9 KΩ or 6 KΩ (min) for the EQ levels 0 - 3 respectively. See Table 3 in datasheet.
D1P	10	USB High Speed positive port.	Make sure the USB2 signals DP/DM polarity corresponds to the pins DxP/DxM respectively.
D1M	9	USB High Speed negative port.	Make sure the USB2 signals DP/DM polarity corresponds to the pins DxP/DxM respectively.
D2P	7	USB High Speed positive port.	Make sure the USB2 signals DP/DM polarity corresponds to the pins DxP/DxM respectively.
D2M	8	USB High Speed negative port.	Make sure the USB2 signals DP/DM polarity corresponds to the pins DxP/DxM respectively.
SDA	11	In I2C Mode, Bidirectional I2C data pin. In Non-I2C Mode, no function.	I2C Mode: 4.7 kΩ (5%) pull-up resistor required for I2C Mode. Non-I2C Mode: This pin must be floating or connected to ground.
SCL/CD	13	In I2C Mode, I2C clock pin. In Non - I2C mode, Flag indicating that a USB device is attached.	I2C mode: I2C clock pin [I2C address = 0x2C], 4.7 kΩ (5%) pull-up resistor required for I2C Mode. Non-I2C mode: CD can be connected to a LED in series with a resistor to GND. If no LED is needed, the pin can be left unconnected.
DC_BOOST/ENA_HS	9	I2C Mode: Pin is reserved for testing. Non-I2C Mode: DC Boost set before reset then becomes flag indicating that channel is in High Speed mode.	Ensure DC_BOOST/ENA_HS upon reset has correct input voltage for desired DC gain. This can be set via resistive divider with pull-down and pull-up (to 3.3 V) resistors between 22 kΩ to 47 kΩ. See Table 3 in TUSB215 datasheet. After reset pin outputs flag indicating High Speed mode.
NC	2,3	N/A	Leave unconnected.
Notes: Common mode chokes placed as close as possible to the USB connectors. Verify the pinout of the USB connectors. Verify pin-out of TUSB215 matches datasheet. Always refer to the datasheet of this device for complete descriptions of each pin.			

2 References

- TUSB215 USB 2.0 High Speed Signal Conditioner Datasheet
- TUSB215 Evaluation Module

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265