TVP5150A Frequently Asked Questions - FAQs

HPA Digital Audio Video

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ABSTRACT

The following frequently asked questions (FAQ) on the TVP5150A are from a variety of sources covering many aspects of the device itself, its features, application and EVM. This document is organized into sections related to different areas of the TVP5150A. Questions related to multiple areas are shown in each area along with the corresponding answer.

The size of this document and the number of questions covered may make it difficult to locate an FAQ. If this is the case, try using the Search tool to locate specific words associated with the FAQ.

Questions not covered in this document may be available by referring to the TVP5150A Data Manual, SLES087, as well as the various application notes and user guides available at www.ti.com.

1 Input and Output Formats and Standards

1. What inputs are supported with the TVP5150A?

   The TVP5150A supports two composite (CVBS) analog inputs or one S-Video analog input. Additional inputs can be made available using a low-cost analog switch or by routing multiple inputs together. In the case of the latter, it is important not to simultaneously connect multiple video sources to the inputs that are routed to the same input pin of the TVP5150A.

2. What input video formats does the TVP5150A support?

   The TVP5150A supports the following video formats:

   - NTSC (J, M, 4.43)
   - PAL (B, D, G, H, I, M, N, Nc)
   - SECAM (B, D, G, K, K1, L)

3. Does the TVP5150A autoswitch or auto-detect? What is the difference?

   The TVP5150A performs autoswitch meaning that it automatically detects and then reinitializes itself to decode the input video standard without reprogramming I2C register settings.

   Autoswitch is the ability for a video decoder to detect and then automatically reconfigure itself to adapt to an input video standard. Auto-detect only detects the video standard and then relies on a backend to reinitialize it.

4. Do all of the video standards autoswitch by default?

   No, by default only the following video standards are supported in the autoswitch.

   - NTSC (J, M)
   - PAL (B, D, G, H, I)

   The remaining video standards (PAL-M, N, NTSC 4.43, and SECAM) are masked off and require a register write to enable them in the autoswitch process. Once they are enabled in the autoswitch process, it is not necessary to enable them again unless a HW reset is performed.

5. What outputs does the TVP5150A support?

   The TVP5150A supports the following user programmable video output formats:

- 8-bit ITU-R BT.656 4:2:2 YCbCr with embedded syncs
- 8-bit 4:2:2 YCbCr with discrete syncs
- 2x sampled raw VBI data in active video during a vertical blanking period
- Sliced VBI data during a vertical blanking period or active video period (Full Field mode)

6. Can I use ITU-R BT.656 and still use the HSYNC and VSYNC outputs?

   Yes, the HSYNC and VSYNC outputs from the TVP5150A are still available when outputting ITU-656 digital video outputs.

7. Does the TVP5150A have a built in scaler?

   No, the TVP5150A does not have a built in scaler. The TVP5150A does however support AVID cropping. While all of the video data is still output from the TVP5150A, AVID, a programmable signal representing the active video data, can be used to gate the amount of active data taken into a backend device. This signal would work similar to a Write Enable on a backend processor.

8. Does the TVP5150A support 4:2:0 outputs?

   No, the TVP5150A does not support 4:2:0 sampled digital video outputs.

9. When switching between inputs, how many fields does it take to lock? Is it possible to enable a faster lock speed?

   The TVP5150A takes approximately 6 fields when switching between inputs. The fast lock speed within the TVP5150A is optimized by default.

10. Will the TVP5150A automatically detect whether composite (CVBS) or S-Video inputs are connected?

    No, the TVP5150A does not automatically detect inputs. It only detects and autoswitches input video standards on the selected video input.

11. Does the TVP5150A have an external output enable (OE) pin?

    No, the TVP5150A does not have an external OE pin. The OE for the digital data output and the clocks is available via the Miscellaneous Control Register, 03h, bit 3 and bit 0 respectively. By default only the data output is high impedance. The SCLK output is already enabled by default. When enabling the data outputs, ensure the SCLK is not accidentally disabled.

12. What happens to SCLK and the sync outputs when no video signal is present on the inputs?

    If no video signal is present on the selected input into the TVP5150A, the SCLK and sync information is still valid for the last detected video standard, and the output video will be black.

13. Does the TVP5150A oversample the input? How does it meet the 13.5-MHz output from the ITU-601 specification?

    Yes, the TVP5150A performs 2x oversampling on all analog input signals. The ADC outputs are then decimated to reduce the data rate to 1x the pixel rate. This oversampling and decimation technique effectively increases the overall SNR by approximately 3dB.

14. What is meant by “extended coding range”?

    I2C register 0Dh bit 6 controls the YCbCr coding range of the digital outputs. By default the coding range is set to 1, “Extended Coding Range”, 1 – 254 on Y, Cb and Cr. The ITU-R BT.601 specification only allows codes of 16 - 235 for Y and 16 - 240 for Cb and Cr. To avoid clipping, the extended coding range allows for overshoot outside of the ITU-R BT.601 specification. Within the output formatter of the TVP5150A, the digital outputs are then rescaled to conform to the ITU-R BT.601 or ITU-R BT.656 outputs.

15. Are the F bit and the V bit within the ITU-R BT.656 digital outputs programmable?

    The F bit and V bit within the ITU-R BT.656 digital outputs are programmable using the F and V Bit Control Register, 15h, bits [5:4].

Table 1. F and V Bit Control Register Settings

BIT 5	BIT 4	NUMBER OF LINES PER FRAME	F BIT	V BIT
0	0	Standard	ITU-R BT.656	ITU-R BT.656
		Nonstandard even	Force to 1	Switch at field boundary
		Nonstandard odd	Toggles	Switch at field boundary
0	1	Standard	ITU-R BT.656	ITU-R BT.656
		Nonstandard	Toggles	Switch at field boundary
1	0	Standard	ITU-R BT.656	ITU-R BT.656
		Nonstandard	Pulse mode	Switch at field boundary
1	1	Illegal		

16. During the horizontal and vertical blanking periods, does the TVP5150A output the digital data?

    Digital data is output during vertical blanking, but not during horizontal blanking. Output data during the vertical blanking can have VBI information while output data during horizontal blanking is black.

    If VBI ancillary data is enabled (register CDh), sliced VBI data may be transmitted during horizontal blanking.

17. Is it possible to mask the output data during the horizontal and vertical blanking period?

    If using ITU-R BT.656 digital outputs, only the horizontal blanking data may be masked by using the AVID cropping feature. The AVID registers are AVID Start Pixel Register, 16h – 17h and the AVID Stop Pixel Register, 18h – 19h. Masking the data during the vertical blanking period is not available since compliance with ITU-R BT.656 must be maintained.

    If using ITU-R BT.601 digital outputs with discrete syncs then data in both the horizontal and vertical blanking periods may be masked using the AVID Start and Stop registers and the VBLK Start and Stop registers, respectively.

18. Can the TVP5150A generate an arbitrary number of samples per line?

    No, the TVP5150A generates the standard number of samples per line based on the input video standard.

2 Initializing the TVP5150A

1. Once the TVP5150A is up and running, are there additional register settings that would further optimize its performance?

    By default the video performance of the TVP5150A is considered optimized. On power up the TVP5150A is configured by default to enable the following:

    - Composite (AIP1A) input
    - Autoswitch between NTSC-M or PAL (B, G, H, I)
    - ITU-R BT.656 digital outputs
    - Adaptive 4-line comb filter

2. What is the minimum number of register writes required to begin using the TVP5150A?

   For a basic setup, the number of I2C writes required to begin using the TVP5150A typically ranges from 1 to 5. Please refer to the TVP5150A Quick Start Guide, SLEU042 for more information.

3 I2C Communication

1. How do I configure the TVP5150A for a specific I2C address?

   The I2C address for the TVP5150A is configured using YOUT7/I2CSEL, pin 11, on the TVP5150A. When pulled high the I2C address is BAh, when the YOUT7/I2CSEL pin is pulled low the I2C address is B8h. The level on this pin is read at the end of the reset.

Table 2. I2C Address Selection

YOUT7/I2CSEL	I2C Base Address
DGND	B8h
IO_DVDD	BAh

2. What is the maximum I2C speed the TVP5150A will support?

   The TVP5150A I2C operates at a maximum speed of 400Kbits/sec.

3. When using the TVP5150AEVM I continue to get I2C error messages. What is wrong?

   See Table 9 for troubleshooting information.

4. What is the I2C bus latency of the TVP5150A?

   TVP5150A requires delays in I2C accesses to accommodate its internal processor's timing. Delays are of variable length, maximum delay is 64-µs (1 horizontal line time). TVP5150A holds I2C clock line (SCL) low to indicate the wait period to the I2C master and prevent further accesses. The I2C master must not attempt further accesses while the clock line is held low. There are two ways to prevent this:

   - Check for SCL held low before issuing I2C Stop. (Preferred method, more efficient.)
   - Insert a 64-µs delay into every I2C access.

Start	Slave address (B8/BA)	Ack	Subaddress (xx)	Ack	Data (xx)	Ack	Wait up to 64us (SCL held low)	Stop

Figure 1. Example I2C Write Sequence

The above 64-µs delay will be valid for most registers. However, access to some TVP5150A registers will trigger a device internal initialization process. For these registers a much longer SCL-low wait time will be required. These registers are Autoswitch mask (04h), Software reset (05h), Color killer threshold control (06h), Luminance processing control #1 & #2 (07h, 08h), Video standard (28h), and Macrovision on/off counter (2Eh & 2Fh). Therefore, it is highly recommended that the system I2C master should follow I2C standard to implement check for SCL held low before issuing I2C Stop.

5. Can the TVP5150A be programmed while in reset?

   No, the TVP5150A cannot be programmed while in reset.

6. Can I write to reserved register bits?

   The reserved registers should never be programmed. If your system automatically increments through the I2C registers as they are programmed then it is highly recommended that the reserved registers be avoided when doing so.

   The default values of the register bits within active registers are defined in the I2C register summary and the register description. The default value for each register is listed here including the reserved bits. When writing to active bits within registers, it is important that the default value of any reserved bits is maintained. Also, it is not safe to assume that all reserved bits are zero. Some reserved bits may actually have a default value of 1.

7. Does the TVP5150A auto increment the I2C registers when they are programmed?

   Yes, the TVP5150A auto increments the I2C register address after each write.

4 Device Registers

1. Are there status registers available that indicate the horizontal and vertical lock status, field rate, color subcarrier lock status, etc?

   Yes, there are multiple status registers within the TVP5150A that provide this information. The status registers begin with the Status Register #1, 88h, and end with Status Register #5 at 8Ch.

2. Is there a pin on the TVP5150A that provides horizontal lock or vertical lock?

   The VSYNC/PALI, pin 24, can be set to output HLK. This can be configured using the Miscellaneous Control Register, 03h, and the Configuration Shared Pins Register, 0Fh.

The FID/GLCO, pin 23, can be set to output HLK. This can also be configured using the Miscellaneous Control Register, 03h, and the Configuration Shared Pins Register, 0Fh.

3. Does the TVP5150A detect Macrovision and identify which type is present?

   Yes, the TVP5150A provides status registers that indicate the type of Macrovision detected on the analog input. The Status Register 2, 89h, bits [2:0] provide this information. Please refer to the TVP5150A Data Manual, SLES087, for more information.

4. Does the TVP5150A support brightness, contrast, hue and sharpness controls via I2C?

   Yes, the TVP5150A does support brightness, contrast, hue and sharpness controls via I2C. The sharpness control within the TVP5150A register map is called luma peaking. Please refer to the TVP5150A Data Manual, SLES087, for more information.

5. What is the Black Output feature within the Video Input Source Selection #1 Register, 00h?

   During normal operation, when the TVP5150A is decoding the analog video input, setting the Black Output, bit 3, to 1 forces the digital output data to black.

6. Can the TVP5150A be programmed while in reset?

   No, the TVP5150A cannot be programmed while in reset.

7. Can I write to reserved register bits?

   No. The reserved registers should never be programmed. If your system automatically increments through the I2C registers as they are programmed then it is highly recommended that the reserved registers be avoided when doing so.

   The default values of the register bits within active registers are defined in the I2C register summary and the register description given in the TVP5150A Data Manual, SLES087. The default value for each register is listed here including the reserved bits. When writing to active bits within registers it is important that the default value of any reserved bits is maintained. Also, it is not safe to assume that all reserved bits are zero. Some reserved bits may actually have a default value of 1.

8. Do the TVP5150A I2C registers auto increment when they are programmed?

   Yes, the TVP5150A auto increments the I2C register address after each write.

9. Does the TVP5150A have a software reset? Hardware reset?

   Yes, the TVP5150A supports a hardware and software reset. An active low on RESETB, pin 8, for >200ns resets the TVP5150A. The software reset is controlled using the Software Reset Register, 05h, bit 0. By default this register is configured for normal operation. The hardware reset has priority over the software reset.

5 Application Circuit, Schematic & Layout

1. Do I need to use the AC coupling capacitor on the analog inputs?

   Each analog input must be AC coupled through a 0.1-µF capacitor. Unused analog inputs must be AC coupled through a 0.1-µF capacitor to ground.

2. What is the purpose of the attenuation circuit (voltage divider) on the analog input?

   A resistor divider network is used to attenuate the input signal while still providing a termination of approximately 75 Ohm. Recommended attenuation is 50%, achieved with two commonly available 39-Ohm resistors. The recommended AC-coupling capacitor value is 0.1µF.

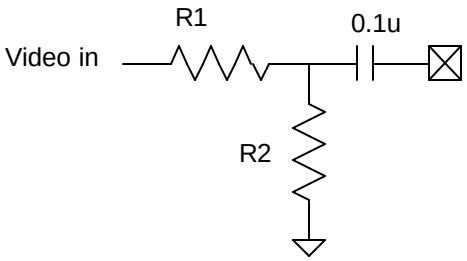

Figure 2. TVP5150A Input Termination

The automatic gain control of the TVP5150A properly scales the inputs with amplitudes of approximately 30-135% amplitude when the recommended resistor-divider termination is used. Other resistor-divider pairs are possible which result in different effective ranges for automatic gain control. Table 3 shows how the AGC range changes for different termination pairs.

NOTE: Due to the 0.75-Vpp input limit, the upper end of each amplitude range includes certain signals (example: 100% amplitude, 100% saturation color bars) which exceed the range of the TVP5150A input circuit.

Table 3. AGC Range for Common Resistor-Divider Terminations

Resistor pair R1:R2	Attenuation	Approx. AGC range	Notes
56:18	24%	65 - 280%	Worse SNR
56:22	28%	55 - 240%	
47:27	36%	45 - 185%	
39:33	46%	35 - 145%	
39:39	50%	30 - 135%	Recommended termination
33:39	54%	30 - 125%	
27:47	64%	25 - 105%	Better SNR

3. What type of crystal should I use for the TVP5150A?

   We recommend using a 14.31818-MHz parallel-resonant, fundamental mode crystal, not a third-overtone crystal. The crystal tolerance should be 50ppm or better.

   The manufacturer's load capacitance required should be carefully considered when designing the crystal circuit. The capacitors used on the TVP5150AEVM for instance were chosen based on the specific crystal used. Please refer to the TVP5150A Quick Start Guide, SLEU044, for more information.

4. Are both the 1.8-V and 3.3-V supplies required by the TVP5150A?

   Yes, both voltage supplies are required to properly power the TVP5150A. The 1.8-V supply is used for DVDD and AVDD18 while the 3.3-V supply is used for IO_DVDD and AVDD33.

5. What pins are required to be pulled up or pulled down on power up and what are their purpose? Can I still use the pin as intended without issues?

   YOUT7/I2CSEL, pin 11, should be pulled up or down depending on the desired I2C address for the TVP5150A. When pulled high the I2C address is BAh, when the YOUT7/I2CSEL pin is pulled low the I2C address is B8h.

Table 4. I2C Address Selection

YOUT7/I2CSEL	I2C Base Address
DGND	B8h
IO_DVDD	BAh

Also, it is important to note that SDA and SCL of the I2C bus require pull-up resistors somewhere in the system design.

6. Is a 0.1-µF decoupling capacitor required on each supply pin of the TVP5150A?

   We highly recommend using a 0.1-µF capacitor on each power supply pin to reduce the level of noise in your system.

7. Can you recommend an anti-aliasing filter circuit for my design?

   Anti-alias filtering may be required if out-of-band noise is present on the inputs to the TVP5150A. Figure 3 shows two example filters with good cost/performance characteristics for typical applications. A different filter is shown for S-video because the TVP5150A sample rate for each S-video component is 13.5 MHz, compared to 27 MHz for composite video. Similarly effective noise attenuation, therefore, requires a steeper rolloff and a higher-order filter.

   The example S-video filter is shown in a form which can be implemented in two stages separated by a switch so that only the second stage is used for composite video input. If a two-stage approach is not desired then the 470-pF/180-pF capacitor pair may be replaced in the design with a single 680-pF capacitor.

   Figure 4 and Table 5 show amplitude and group delay characteristics for the example filters of Figure 3.

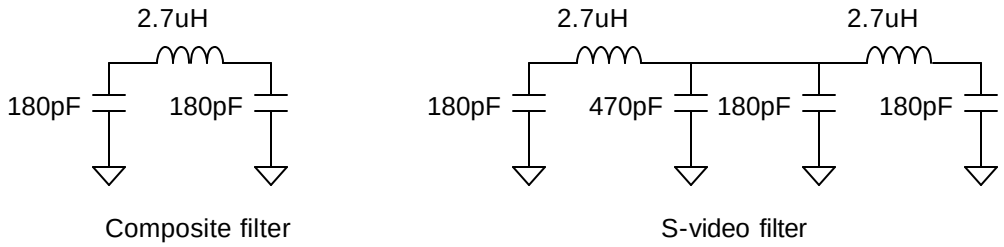

Figure 3. Example Anti-Alias Filters for Composite and S-Video

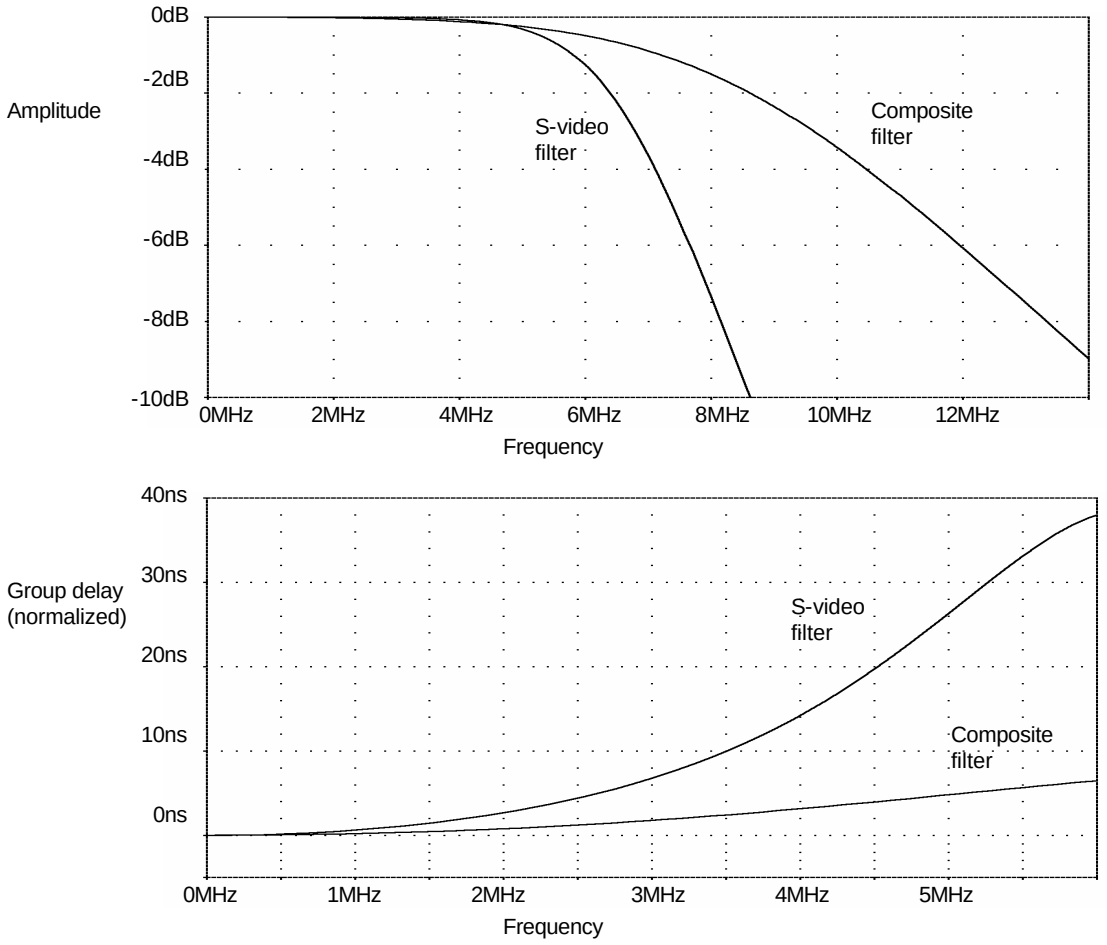

Figure 4. Example Anti-Alias Filter Characteristics

Table 5. Example Anti-Alias Filter Characteristics (detail)

Frequency	Composite filter		S-video filter		Notes
	Amplitude	Delay	Amplitude	Delay	
3.58 MHz		3 ns		11 ns	NTSC color subcarrier
4.2	-0.1 dB	4 ns	-0.1 dB	16 ns	NTSC bandwidth
4.43		4 ns		19 ns	PAL color subcarrier
6.0	-0.5 dB	7 ns	-1.3 dB	38 ns	PAL-D bandwidth
7.5	-1.1 dB		-5.4 dB		PAL sampled image for S-video
9.3	-2.7 dB		-13 dB		NTSC sampled image for S-video
21.0	-18 dB		-47 dB		PAL sampled image for composite
22.8	-20 dB		-51 dB		NTSC sampled image for composite

8. What is the purpose of the GPCL pin?

   The GPCL, pin 27, is a general purpose IO pin and is muxed with INTREQ and VBLK. The Configuration Shared Pins Register, 0Fh, bit 1 is used to determine whether pin 27 outputs GPCL/VBLK or INTREQ. Once the Configuration Shared Pins Register, 0Fh, has been configured for GPCL/VBLK, the Miscellaneous Control Register, 03h, can be setup to determine if pin 27 will be GPCL or VBLK.

   The Miscellaneous Control Register is used to configure GPCL. GPCL is configured as the default, not VBLK. Next, it is necessary to decide whether GPCL should be an input or output. If an output, the state, 1 or 0, can also be selected.

9. How do I use an oscillator instead of a crystal in my design?

   To use a 14.31818-MHz oscillator instead, connect the oscillator output to the XTAL1 input. The capacitors used in the crystal circuit are not required.

10. How do I use a crystal instead of an oscillator in my design?

    The crystal design requires the use of XTAL1 and XTAL2 and two capacitor s as seen in the following figure. C1 and C2 must be calculated based on the load capacitance requirements of the crystal selected. These requirements vary from manufacturer to manufacturer.

    The equation used to calculate the required capacitors is:

$$C1 = C2 = 2 \times C_{load} - C_{stray}$$

    where: C_{load} is the crystal manufacturer's load capacitance requirement

    C_{stray} is the stray capacitance (assume 3-8pF)

    Example: If C_{load} = 20pF, then C1 = 33pF, C2 = 33pF.

    Refer to the TVP5150A Quick Start Guide, SLEU044, or the following figure for more information.

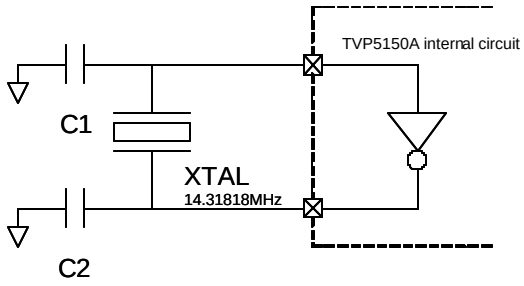

Figure 5. TVP5150A Crystal Circuit

6 System Applications & Interfaces

1. What applications or end equipments does the TVP5150A support?

   The TVP5150A supports a variety of end equipments not limited to the following:

   - Cell Phones
   - USB Capture
   - Notebook PC
   - PC Video Cards
   - LCD TV

2. In trying to achieve a lower compression ratio of the digital data, the high frequency luma data continues to be a limiting factor. Is there a solution to this?

   Yes, it is possible to disable the luminance comb filter and enable the luminance chroma trap filter instead. This filters out most of the high frequency luminance data but may adversely affect the video quality. This feature is available in the Luminance Processing Control #2 Register, 07h, bits 7 and 6.

3. What is the purpose of the GPCL pin?

   The GPCL, pin 27, is a general purpose IO pin and is muxed with INTREQ and VBLK. The Configuration Shared Pins Register, 0Fh, bit 1 is used to determine whether pin 27 outputs GPCL/VBLK or INTREQ. Once the Configuration Shared Pins Register, 0Fh, has been configured for GPCL/VBLK, the Miscellaneous Control Register, 03h, can be setup to determine if pin 27 will be GPCL or VBLK.

   The Miscellaneous Control Register is used to configure GPCL. GPCL is configured as the default, not VBLK. Next, it is necessary to decide whether GPCL should be an input or output. If an output, the state, 1 or 0, can also be selected.

4. How long must RESETB be held low in order to reset the TVP5150A?

   RESETB is active low and must be pulled low for >200ns in order to reset the TVP5150A.

5. I am looking for a high-performance video decoder with more inputs, superior Y/C separation and excellent VCR performance for high end solutions. Does TI have a solution available for this?

Yes, the TVP5146 video decoder was designed for medium to high end applications providing 10 analog inputs including SCART support, a 5-line comb filter for superior Y/C separation and a robust sync detector for high quality VCR performance. Please refer to the TVP5146 Data Manual, SLES084, for more information.

6. When switching between inputs, how many fields does it take to lock? Is it possible to enable a faster lock speed?

   The TVP5150A takes approximately 6 fields when switching between inputs. The fast lock speed within the TVP5150A is optimized by default.

7. How do I interface the TVP5150A to my backend video processor?

   Using the ITU-R BT.656 digital video outputs and SCLK is the simplest interface to a backend. The required number of pins is at a minimum and no additional clocks are required. This interface provides 8 bits of data out which include the embedded sync information.

   If the backend does not support ITU-R BT.656 then it may be necessary to use ITU-R BT.601 digital video outputs with discrete syncs. There is no performance difference between these two interfaces. It is merely a difference in the number of required signals. With the ITU-R BT.601 interface, the backend requires the discrete HS and VS syncs as well as the digital video data and SCLK.

8. How much current does the TVP5150A draw on the analog and digital supplies?

   The amount of current drawn on the supplies will vary with the type of input begin used. With a CVBS input the typical current is shown below:

Table 6. CVBS Input Current Draw

Supply	Description	Current
IO_DVDD	3.3V IO digital supply current	4.8mA
DVDD	1.8V digital core supply current	25.3mA
PLL_AVDD	1.8V analog supply current	5.4mA
CH1_AVDD	1.8V analog supply current	24.4mA

9. What is the total power consumption when the TVP5150A is in Power Down mode?

   The total power consumption of the TVP5150A in Power Down mode is typically less than 1mW.

10. Does the TVP5150A have to be the clock master?

Yes, the TVP5150A must always provide the SCLK, HSYNC, and VSYNC signals to the backend. The TVP5150A is not capable of receiving these signals as inputs.

7 Chrominance and Luminance

1. There are faint vertical lines in bright areas with strong color (e.g. cyan or yellow color bars). What is causing this? How do I fix it?

   This is called Chroma Clipping. The TVP5150A has protection to reduce or eliminate chroma clipping for nonstandard signals. It can still show up under some circumstances though. Chroma clipping occurs when signal exceeds range of ADC which can occur when:

   - AGC turned off
   - Peak protection turned off
   - Very high amplitude signal

   It causes faint vertical lines in bright areas with highly saturated color. Example: 100% color bars cyan and yellow.

   To confirm this is the problem:

   - Lower saturation and/or brightness of the source and verify lines go away.
   - Check amplitude of source and verify it does not exceed input range of the TVP5150A.
   - Turn TVP5150A AGC and peak protection back on if they are off (default is on).

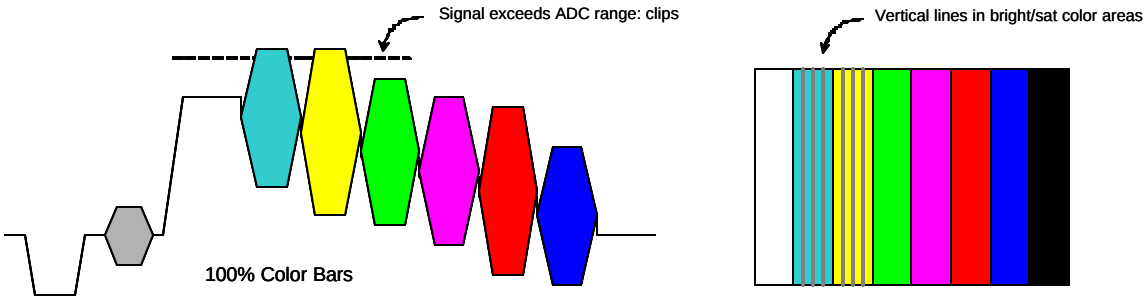

Figure 6. Faint Vertical Lines in 100% Color Bar

This can be caused by out-of-band signal beating against the sample clock of the decoder. A common source of this out-of-band signal is when digital video is converted to analog and not followed with an appropriate reconstruction filter. An anti-alias filter before the decoder input eliminates this problem.

2. The colors on the output of the TVP5150A are reversed or improper. What is the cause and how do I fix it?

   This problem is often caused by alignment or Genlock issues. These can be very easy to diagnose with a color bar test pattern.

   Picture is entirely magenta and green: Luma and chroma are reversed. Possible cause:

   - Multiplexed luma and chroma are reversed. This may be affected by TVP5150A AVID Start/Stop or HSYNC, or encoder horizontal alignment adjustments.

   Red and blue color bars are reversed order: Cb and Cr are reversed. Possible cause:

   - This may be affected by TVP5150A AVID Start/Stop or HSYNC, or encoder horizontal alignment adjustments.

3. There is no color or the color is intermittent on the output of the TVP5150A. What is the cause and how do I fix it?

   This is typically caused by an improperly designed crystal circuit. The load capacitance requirements from the manufacturer of the crystal are very important and must be considered when designing the crystal circuit. See previous discussions of crystal circuits.

   This can also be caused by improper use of genlock/RTC. See the following Genlock and RTC section.

8 Comb Filter

1. Can you recommend which comb filter settings I should use for a given input video format?

   The adaptive comb filter of the TVP5150A on power up is considered optimal for all video standards.

9 Genlock and RTC

1. Does my system require the use of the Genlock (RTC) or GLCO pin?

   This depends on the system. Proper composite (modulated) color requires an extremely accurate subcarrier frequency. An encoder using a line-locked clock must know when its input clock frequency changes in response to horizontal sync frequency changes at the decoder input.

   The decoder and encoder use a serial data stream to transfer the color discrete-time oscillator (DTO) increment value between them, to compensate for the changing clock frequency. This datastream is called Genlock or RTC. An alternative is to use a time base corrector to change clocks.

If neither of these techniques is used, the color with a noisy or unstable signal will be streaky, flash on and off, or be absent entirely on the re-encoded composite output of the encoder.

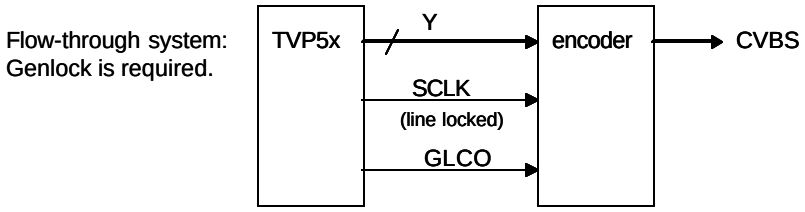

Figure 7. TVP5150A to Encoder Flow Through System – GLCO Required

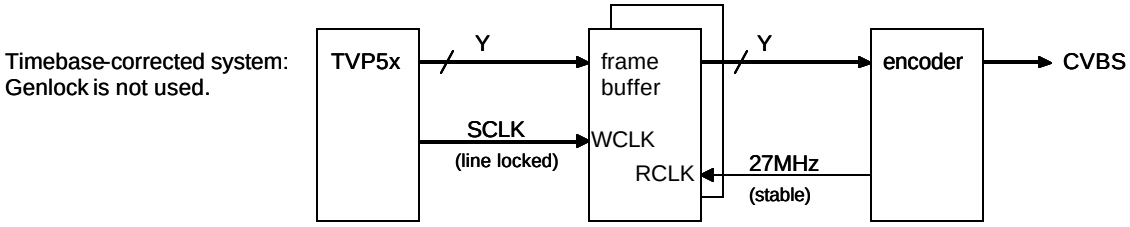

Figure 8. TVP5150A to Time Base Corrector to Encoder – GLCO Not Required

10 PLL and Sync Information

1. Can the TVP5150A be slaved to an external clock?

   No, the TVP5150A video decoder generates a clock that is locked to the sync frequency of the incoming video and cannot function as a slave to an external clock. The TVP5150A uses a external clock (crystal or oscillator) only as a reference for the PLL circuitry that generates its own clock. This clock must be 14.31818 MHz.

2. Does the TVP5150A have a built in time base corrector (TBC)?

   No, the TVP5150A does not have a built in TBC.

3. How does the TVP5150A lock to the incoming video input?

   The TVP5150A line locks to the incoming analog video input. This allows the TVP5150A to track the input signal, maintain horizontal and vertical sync, and provide an equal number of pixels per line.

4. Does TVP5150A sample asynchronous to the incoming analog video?

   No, by means of internal clock generation (PLL) the analog input signal is sampled synchronously (line-locked). Each horizontal line yields an integer number of samples. The video signal is two-fold over-sampled to avoid the need for sharp cut-off analog anti-aliasing filters. A digital decimation filter converts two samples to one pixel. Dependent on video standard the number of samples per line and the sampling rate amount are:

Table 7. Video Standards Information

Standard	Pixel Aspect Ratio	Samples per Line	Sample Rate [MHz]
NTSC	ITU-R BT.601	1716	27
PAL / SECAM	ITU-R BT.601	1728	27

The TVP5150A uses a line-locked clock to sample and output data. The clock frequency varies to ensure a constant number of pixels per line (858 NTSC, 864 PAL). Clock frequency is nominally 27 MHz but changes depending on the horizontal sync frequency. The worst case is usually with a VCR input and nonstandard (and changing) HSYNC frequency.

TVP5150A clock is generated by the internal PLL. It is not synchronous with the reference clock on the XTAL1 pin.

TVP5150A clock output **must** be used to drive the back end unless a time base corrector (FIFO or frame buffer) is used. If a time base corrector is used, the TVP5150A output clock must be used for its write timing.

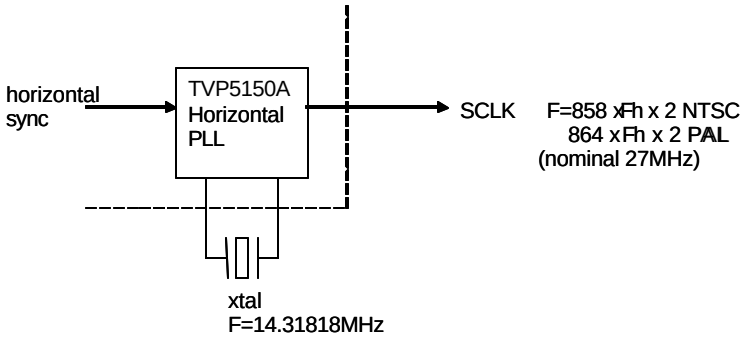

Figure 9. Line-Locked Sampling

5. Does the TVP5150A have to be the clock master?

   Yes, the TVP5150A must always provide the SCLK, HSYNC, and VSYNC signals to the backend. The TVP5150A is not capable of receiving these signals as inputs.

11 VBI Data Processing

1. What is the VBI data processor (VDP) and how does it work?

   VBI data is digital data that is encoded onto an analog video signal, usually transmitted in the non-active video region, vertical blanking interval (VBI). The VBI information includes many data types, current time, program info, VCR/PVR recording info, aspect ratio, etc. Some VBI information can be displayed on-screen (e.g., closed caption).

   The Vertical Blanking Interval data processor slices various data services like teletext and closed caption that are available during the vertical blanking interval.

   These data services are acquired by programming the VDP via I2C. The results can be stored in a FIFO and made available via I2C or ancillary data.

   VBI data processing stages in a video system:

   1. Capture analog waveform
   2. Slice analog waveform into data bytes
   3. Parse data bytes
   4. Decode data bytes
   5. Acts based on the data

   The TVP5150A video decoder does partial work. It processes VBI data up to and including step 2. Additional processing (step 3) can be applied to those with error detection and correction (e.g., Teletext: filtering by magazine/articles and row).

   Other devices in a video system need to finish the VBI data processing & action. Examples: OSD display for CC, Block a channel/program based on V-chip info, Record a program according to VPS, etc.

   The TVP5150A slices this digital information from the input video and supplies it to the user for processing.

   The TVP5150A does **not** automatically generate overlay graphics or OSD from sliced data. An external processor or OSD controller must be used to process and display sliced OSD data.

6. What VBI data formats does the TVP5150A support?

   The TVP5150A VDP supports the following formats. The User defined VBI System at the bottom of the following table is used to indicate that the VDP of the TVP5150A is may be customized to support nonstandard VBI systems.

Table 8. Supported VBI Data Formats

VBI SYSTEM	STANDARD
Teletext WST A	SECAM
Teletext WST B	PAL
Teletext NABTS C	NTSC
Teletext NABTS D	NTSC-J
Closed Caption	PAL
Closed Caption	NTSC
WSS	PAL
WSS-CGMS	NTSC
VITC	PAL
VITC	NTSC
VPS	PAL
V-CHIP	NTSC
Gemstar 1x	NTSC
Gemstar 2x	NTSC
User	Any

7. How would I use the VDP in my application?

   The Figure 10 shows one example: TVP5150A + video processor (VP) + OSD controller (OSD). In this implementation, the TVP5150A will supply VBI data, e.g., closed caption (CC) and V-chip data, to the backend video processor VP. The VP will perform the VBI decoding and then the OSD controller will perform the OSD operations to display CC on top of the video images.

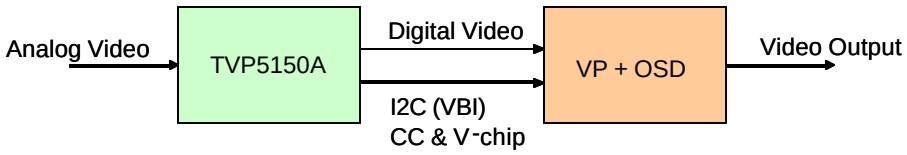

Figure 10. Example System Interface Using the VDP

8. Does VBI data processing mean the TVP5150A performs as a full Line 21 decoder or other VBI data decoding?

   No, the TVP5150A does not perform full decode of captured VBI data. It only captures and slices the VBI data bytes. It does not decode the VBI data bytes or perform actions based on them.

12 Macrovision

1. What version of Macrovision™ does the TVP5150A support?

   The TVP5150A is capable of detecting Type 1, Type 2 and Type 3 Macrovision™ as well as color striping. The detection of these different types is provided in the Status Register #2, 89h, bits [2:0].

13 Audio Clocks

1. Does the TVP5150A support audio clocks?

   No, the TVP5150A does not directly support audio clocks. However, we recommend using the low-cost PLL1708 to generate synchronized audio clocks from the SCLK output of the TVP5150A.

2. Since the TVP5150A does not support audio clocks what device(s) do you recommend generating these clocks?

   We recommend using the low-cost PLL1708 to generate synchronized audio clocks from the SCLK output of the TVP5150A.

14 TVP5150AEVM and WinVCC4 Questions

1. When using WinVCC4, I get I2C communication errors. What is the problem?

   Table 9 provides troubleshooting help to establish communication with the TVP5150AEVM.

Table 9. I2C Communications Errors

No I2C communication.	I2C slave address is wrong.	Close and restart WinVCC4. Choose the alternate slave address in the WinVCC4 Configuration dialog.
	Parallel cable is not connected from PC parallel port to the EVM DB25 connector.	Connect cable.
	EVM is not powered on.	Power supply must be plugged into a 110V/60Hz power source and the cord must be plugged into the power connector on the EVM.
	Wrong type of parallel cable.	Some parallel cables are not wired straight through pin-for-pin. Use the cable supplied with the EVM.
	PC parallel port mode is not set correctly.	Reboot PC, enter BIOS setup program, set parallel port LPT1 mode (Addr 378h) to DCP mode or bidirectional mode (sometimes called PS/2 mode or byte mode). If already set to one of these two modes, switch to the other setting.
	Device was placed in power-down mode.	Press the reset button on the TVP5150AEVM.
	EVM was configured for an external I2C master.	Re-install 0-ohm resistors R5 and R6. Control EVM using the PC parallel port.
	Still no I2C communication	PC may not be capable of operating in the required parallel port mode. This is true of some laptop computers. Use a different computer, preferably a desktop PC.

2. What Windows operating systems does WinVCC4 support?

   WinVCC4 supports Win95, Win98, WinME, WinNT, Win2000 and WinXP operating systems. Port95nt.exe must be installed regardless of the OS.

3. I have the TVP5150A powered up with everything connected. I2C communication is okay and I loaded the dataset from the CMD file, but there is no video.

Typically this can be resolved by verifying the WinVCC4 default input connection with the physical input connection on the TVP5150AEVM.

4. What is the Port95nt.exe and is it required in order to use the TVP5150AEVM?

   Port95nt.exe is a parallel port I/O driver and is required for WinVCC4 to operate correctly. The order of installation is not important as long as both Port95nt and WinVCC4 both running on the same PC.

5. Can I use WinVCC4 to communicate with devices not listed in the I2C Address Configuration screen?

   Yes, WinVCC4 is capable of supporting I2C devices that are not listed in the I2C Address Configuration screen. Once the configuration of the TI devices is complete, click on Edit->Register Map->Generic I2C. From this window it is possible to specify any I2C slave address, register address or data. WinVCC4 also supports I2C read and write capability for Generic I2C devices.

6. Do I need to supply 5V to each DC supply jack on the TVP5150AEVM?

   No, only one DC supply jack should be installed and powered up. The 5-V supply is then shared across the 120-pin connector interface to supply the other board.

7. Do I need to connect a parallel port cable to each DB25 connector on the TVP5150AEVM in order to communicate with both devices?

   No, only one DB25 connector should be installed. The I2C SDA and SCL signals are then shared across the 120-pin connector interface in order to provide I2C communication to both boards. Also, SCL and SDA testpoints are available on both boards of the TVP5150AEVM.

8. How many PCB layers does the TVP5150AEVM use?

   The TVP5150AEVM uses four layers on each board. There is a top and bottom signal layer, a split power plane, and a semi-split ground plane.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265