TVP5146 and TVP5150A VBI Raw Data Mode

HPA Digital Audio Video

Introduction

The TI family of video decoders offers a VBI raw data mode for use in systems where VBI data slicing and processing is handled in the digital backend receiver instead of the video decoder. In this mode of operation, the decoders are configured to output raw 2x over-sampled luma data on the ITU-R BT.656 output during the defined VBLK (vertical blanking) interval. The raw, un-sliced A/D video data is transmitted during the active video portion of the line with chroma samples being replaced with the luma samples.

The default VBLK interval for Field 1 is defined as lines 1 through 20 for 525-line video formats and lines 623 through 23 for 625-line video formats. This interval may be adjusted to include additional lines. Support for NTSC line 21 closed caption data, for example, requires extension of the VBLK interval to include line 21.

TVP5150A VBI Raw Data Mode

The default VBLK interval for the TVP5150A is defined as lines 1 through 20 for 525-line video formats and lines 623 through 23 for 625-line formats. The TVP5150A VBLK interval can be adjusted with the VBLK Start and Stop registers (18h-19h). The TVP5150A VBLK Start and Stop registers provide relative adjustments to the default VBLK interval. After configuring the desire VBLK interval, the Luma bypass (bit 4) in the Luminance Processing Control #1 register (07h) must be set to a logic 1 to enable raw data output. Table 1 shows the default I2C registers with a modified VBLK interval for Line 21 inclusion, while Table 2 shows the default 625 line setup. Also shown in Figures 1 and 2 are digital captures of the TVP5150A ITU-R BT.656 output for comparison of normal operation and raw data operation. Insertion of a 4-byte preamble (00h FFh FFh 60h) prior to the start of the raw data is optional in I2C register 07h.

Table 1. TVP5150A 525-Line Raw Data Setup to Include Line 21

I2C Subaddress	Default	I2C Data	Description
07h	00h	10h	Enable raw data (Luma bypass) and Preamble
18h	00h	00h	VBLK Start = default line 1
19h	00h	01h	VBLK Stop= default +1 to include line 21

Table 2. VP5150A 625-Line Raw Data Setup

I2C Subaddress	Default	I2C Data	Description
07h	00h	10h	Enable raw data (Luma bypass) and Preamble
18h	00h	00h	VBLK Start LSB = default line 623
19h	00h	00h	VBLK Stop = default

Note: Detailed descriptions of the TVP5150A I2C registers related to VBI Raw Data Mode are shown in Appendix A.

TVP5150A Example (set up NTSC for raw data on lines 1 through 21)

1. Set up VBLK interval.
   - Write 01h to register 19h to include line 21.
2. Enable Raw Data Mode
   - Write 10h to register 07h to enable raw data mode.

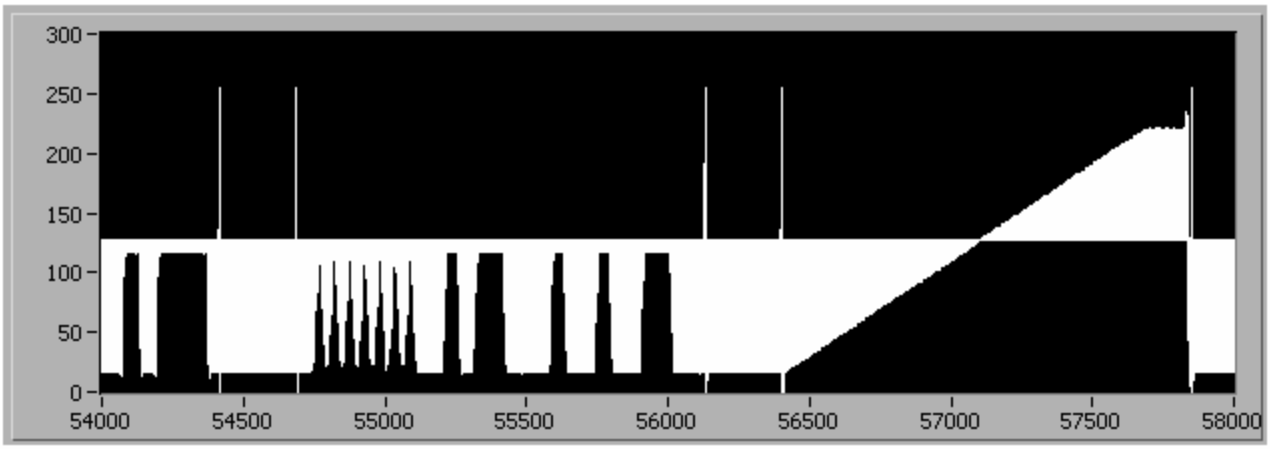

Figure 1. TVP5150A Line 21 Closed Caption ITU-R BT.656 Digital Output Capture With YUV Samples Present. Raw Data Mode disabled.

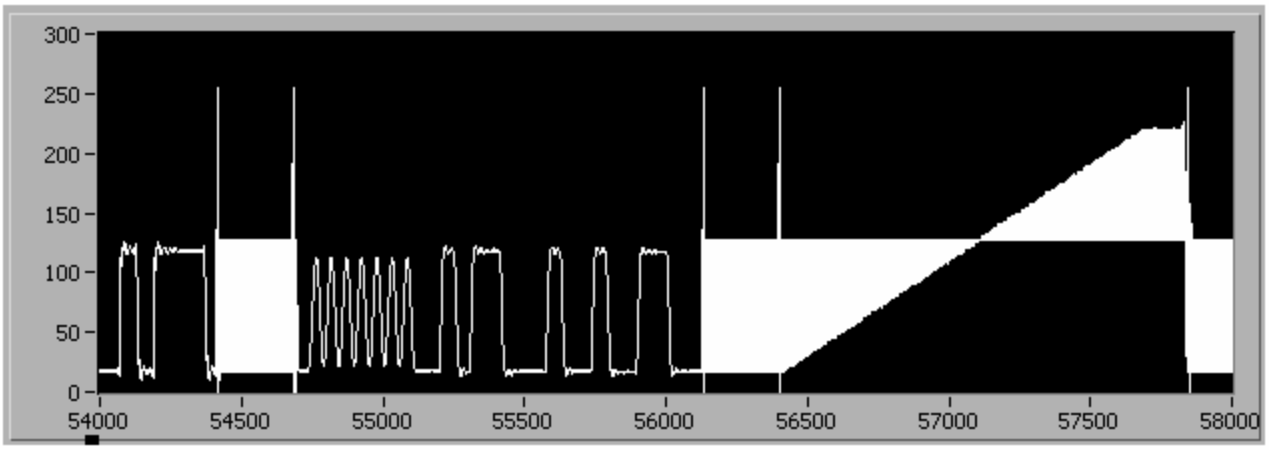

Figure 2. TVP5150A Line 21 Closed Caption ITU-R BT.656 Digital Output Capture in Raw Data Mode. UV (chroma) data are replaced with Y (luma) data.

Note: The full-scale transitions are embedded sync codes.

TVP5146 VBI Raw Data Mode

The TVP5146 default vertical blanking interval for Field 1 is defined as lines 1 through 20 for 525-line video formats and lines 623 through 23 for 625-line video formats. This interval is programmable with the VBLK Start Line and VBLK Stop Line I2C registers (22h-25h). The VBLK Start and Stop registers in the TVP5146 are programmed with absolute line numbers. After configuring the desire VBLK interval, the VBI raw bit (bit 4) in the Luminance Processing Control 1 register (06h) must be set to a logic 1 to enable raw data output. Table 3 shows the default I2C registers with modified VBLK registers for Line 21 inclusion, while Table 4 shows the default 625 line setup. Also shown in Figures 3 and 4 are digital captures of the TVP5146 ITU-R BT.656 output for comparison of normal operation and raw data operation. A four-byte preamble (000h 3FFh 3FFh 180h) is inserted by the TVP5146 prior to the start of the raw data.

Note: The TVP5146 VBLK start and stop values are absolute line numbers. Other TI video decoders, such as the TVP5150A, may use values that are relative adjustments to the default VBLK interval.

Table 3. TVP5146 525-Line Raw Data Setup to Include Line 21

I2C Subaddress	Default	I2C Data	Description
06h	00h	10h	Enable raw data mode
22h	01h	01h	VBLK Start LSB = line1
23h	00h	00h	VBLK Start MSB
24h	15h	16h	VBLK Stop LSB. Change to 22 to include line 21
25h	00h	00h	VBLK Stop MSB

Table 4. TVP5146 625-Line Raw Data Setup

I2C Subaddress	Default	I2C Data	Description
06h	00h	10h	Enable raw data mode
22h	6Fh	6Fh	VBLK Start LSB = line 623 default
23h	02h	02h	VBLK Start MSB
24h	18h	18h	VBLK Stop LSB = line 24 default
25h	00h	00h	VBLK Stop MSB

Note: Detailed descriptions of the TVP5146 I2C registers related to VBI Raw Data Mode are shown in Appendix B.

TVP5146 Example (set up NTSC for raw data on lines 1 through 21)

1. Set up VBLK interval.
   - Write 16h to register 24h to include line 21.
2. Enable Raw Data Mode
   - Write 10h to register 06h to enable raw data mode.

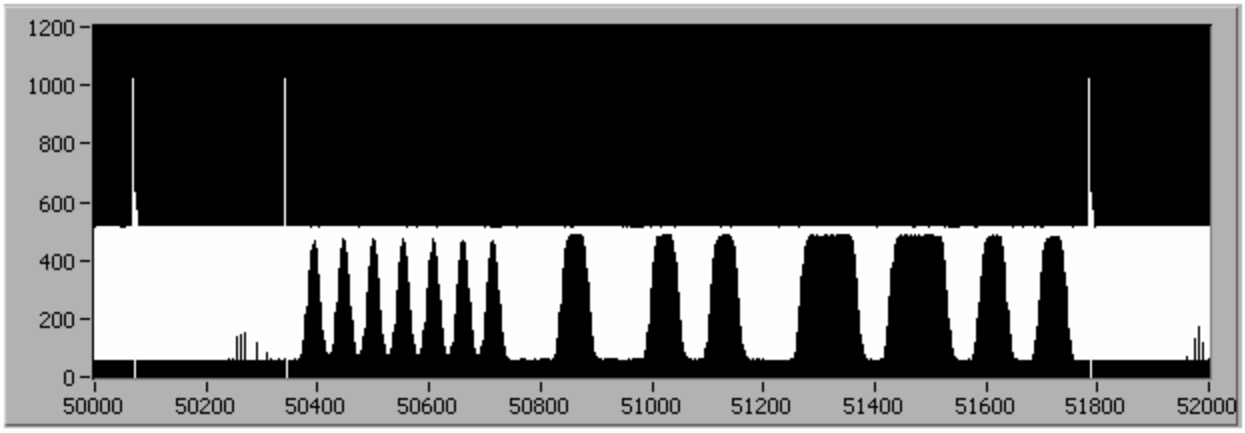

Figure 3. TVP5146 Line 21 Closed Caption ITU-R BT.656 Digital Output Capture With YUV Samples Present. Raw Data Mode is disabled.

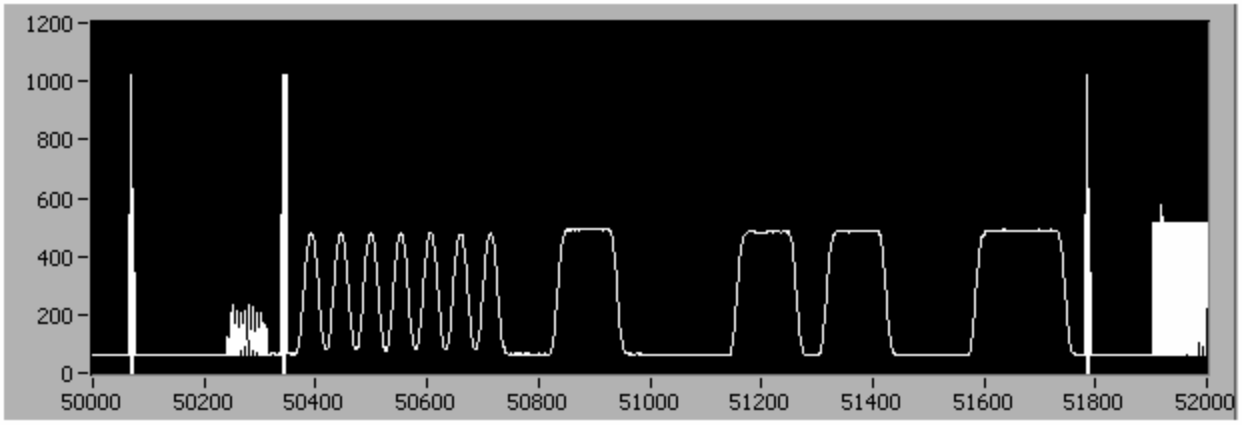

Figure 4. TVP5146 Line 21 Closed Caption ITU-R BT.656 Digital Output Capture in Raw Data Mode. UV (chroma) data are replaced with Y (luma) data.

Appendix A. TVP5150A VBI Raw Data I2C Registers

Luminance Processing Control #1 Register

Address	07h

7	6	5	4	3	2	1	0
Luma bypass mode	Pedestal not present	Disable raw header	Luma bypass during vertical blank	Luminance signal delay with respect to chrominance signal			

Luma bypass mode:

0 = Input video bypasses the chroma trap and comb filters. Chroma outputs are forced to zero (default).
1 = Input video bypasses the whole luma processing. Raw A/D data is output alternatively as UV data and Y data at SCLK rate. The output data is properly clipped to comply with ITU-R BT.601 coding range. Only valid for 8–bit YUV output format (YUV output format = 100 or 111 at register 0Dh).

Pedestal not present:

0 = 7.5 IRE pedestal is present on the analog video input signal (default).
1 = Pedestal is not present on the analog video input signal.

Disable raw header:

0 = Insert 656 ancillary headers for raw data.
1 = Disable 656 ancillary headers.

Luminance bypass enabled during vertical blanking:

0 = Disabled (default)
1 = Enabled

Luminance bypass occurs for the duration of the vertical blanking as defined by registers 18h and 19h. This feature may be used to prevent distortion of test and data signals present during the vertical blanking interval.

Luma signal delay with respect to chroma signal in pixel clock increments (range -8 to +7 pixel clocks):

1111 = -8 pixel clocks delay
1011 = -4 pixel clocks delay
1000 = -1 pixel clocks delay
0000 = 0 pixel clocks delay (default)
0011 = 3 pixel clocks delay
0111 = 7 pixel clocks delay

Vertical Blanking Start Register

Address	18h

7	6	5	4	3	2	1	0
Vertical blanking start							

Vertical blanking (VBLK) start:

0111 1111 = 127 lines after start of vertical blanking interval
0000 0001 = 1 line after start of vertical blanking interval
0000 0000 = Same time as start of vertical blanking interval (default)
1000 0001 = 1 line before start of vertical blanking interval
1111 1111 = 128 lines before start of vertical blanking interval

Vertical blanking is adjustable with respect to the standard vertical blanking intervals. The setting in this register determines the timing of the GPCL/VBLK signal when it is configured to output vertical blank. The setting in this register also determines the duration of the luma bypass function (see register 07h).

Vertical Blanking Stop Register

Address	19h

7	6	5	4	3	2	1	0
Vertical blanking stop							

Vertical blanking (VBLK) stop:

0111 1111 = 127 lines after stop of vertical blanking interval
0000 0001 = 1 line after stop of vertical blanking interval
0000 0000 = Same time as stop of vertical blanking interval (default)
1000 0001 = 1 line before stop of vertical blanking interval
1111 1111 = 128 lines before stop of vertical blanking interval

Vertical blanking is adjustable with respect to the standard vertical blanking intervals. The setting in this register determines the timing of the GPCL/VBLK signal when it is configured to output vertical blank (see register 03h). The setting in this register also determines the duration of the luma bypass function (see register 07h).

Appendix B. TVP5146 VBI Raw Data I2C Registers.

Luminance Processing Control 1

Subaddress	06h

Default (00h)

7	6	5	4	3	2	1	0
Reserved	Pedestal not present	Reserved	VBI raw	Luminance signal delay [3:0]			

Pedestal not present:
0 = 7.5 IRE pedestal is present on the analog video input signal (default)
1 = Pedestal is not present on the analog video input signal

VBI raw:
0 = disable (default)
1 = enable

Duration of the vertical blanking as defined by register 22h through 25h the chroma samples are replaced by luma samples. This feature may be used to support VBI processing done by an external device during the vertical blanking interval. In order to use this bit, the output format must be 10-bit ITU-R 656 mode.

Luma signal delay [3:0]: Luma signal delays respect to chroma signal in 1x pixel clock increments.
0 1 1 1 = Reserved
0 1 1 0 = 6 pixel clocks delay
0 0 0 1 = 1 pixel clocks delay
0 0 0 0 = 0 pixel clocks delay (default)
1 1 1 1 = -1 pixel clocks delay
1 0 0 0 = -8 pixel clocks delay

VBLK Start Line

Subaddress	22h-23h

Default (001h)

Subaddress	7	6	5	4	3	2	1	0
22h	VBLK start [7:0]							
23h	Reserved						VBLK start [9:8]	

VBLK start [9:0]: This is an absolute line number. The TVP5146 device updates the VBLK start line only when the VBLK start MSB byte is written to. If user changed these registers, the TVP5146 retains values in different modes until device resets.
NTSC: default 01h, PAL : default 623 (26Fh)

VBLK Stop Line

Subaddress	24h-25h

Default (015h)

Subaddress	7	6	5	4	3	2	1	0
24h	VBLK Stop[7:0]							
25h	Reserved						VBLK Stop [9:8]	

VBLK stop [9:0]:This is an absolute line number. The TVP5146 device updates the VBLK stop only when the VBLK stop MSB byte is written to. If user changed these registers, the TVP5146 retains values in different modes until device resets.
NTSC: default 21 (15h), PAL : default 24 (18h)

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