Application Report
SLUA836A–August 2017–Revised March 2018

UCC25630x Practical Design Guidelines

ABSTRACT

This application note provides system design guidelines for the UCC25630x resonant LLC controller. The process for optimizing certain LLC design parameters such as burst-mode threshold, soft-start considerations, and audible noise are presented. The layout guidelines and suggested system bring-up processes are introduced.

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1 Introduction

The UCC25630x is a fully-featured LLC controller with an integrated high-voltage gate driver. The controller is designed to pair with an external PFC stage to provide a complete AC-to-DC power solution. This guide aims to provide some useful tips in the practical design. Some possible design issue scenarios are discussed as well, along with suggested solutions.

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2 Soft Start

Figure 1 shows the soft-start logic within the UCC25630x device. During startup, an internal MUX selects the SS signal as the input to the pick lower block. Because the optocoupler does not consume much current from the feedback loop at startup, the FBreplica signal will be at maximum. As a result, the pick lower block will select the SS signal to pass on to the pick higher block. During the startup period, a second MUX will select ground as the input to the pick higher block. As a result, the SS signal will be sent to a differential amplifier to convert the signal to two thresholds symmetrical to Vcm: VTH and VTL.

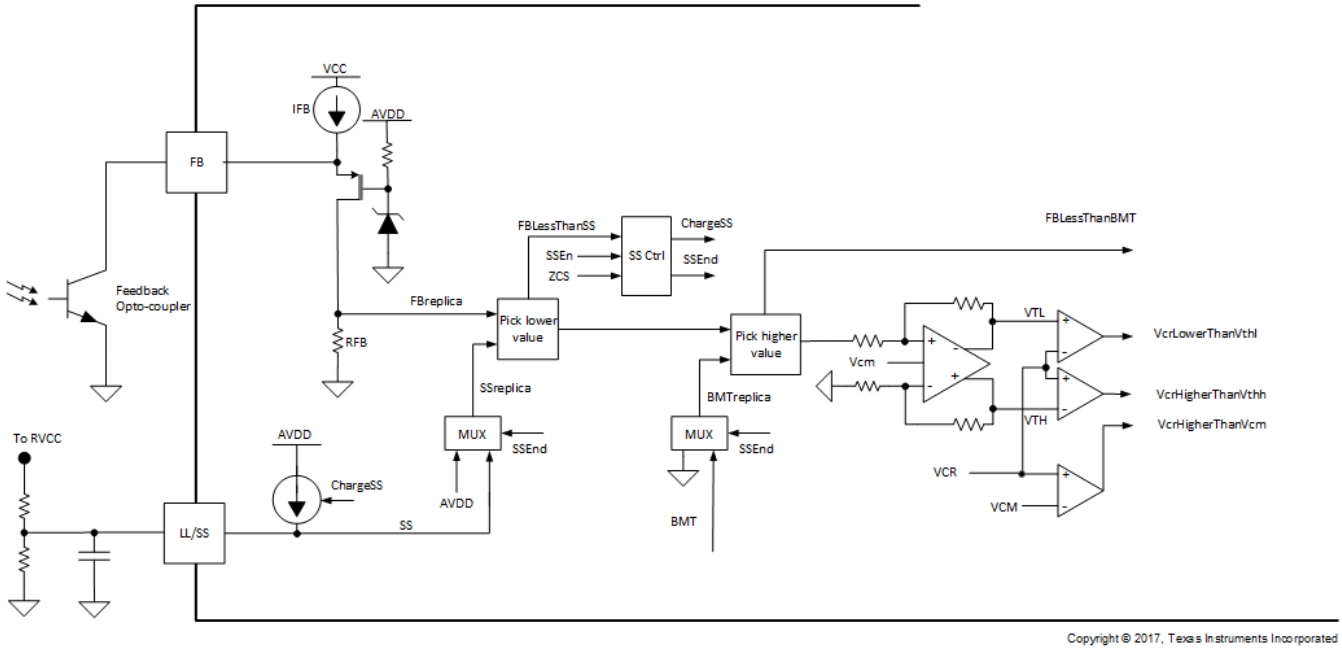

Figure 1. Soft-Start Block Diagram

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During startup, the difference between the VTH and VTL thresholds is equal to the amplitude of the SS signal as shown in Figure 2. As the soft-start capacitance continues to be charged by the internal current source, the difference between VTH and VTL increases at a rate proportional to dVss / dt. The soft-start period is terminated once the FBreplica signal becomes less than the SSreplica signal.

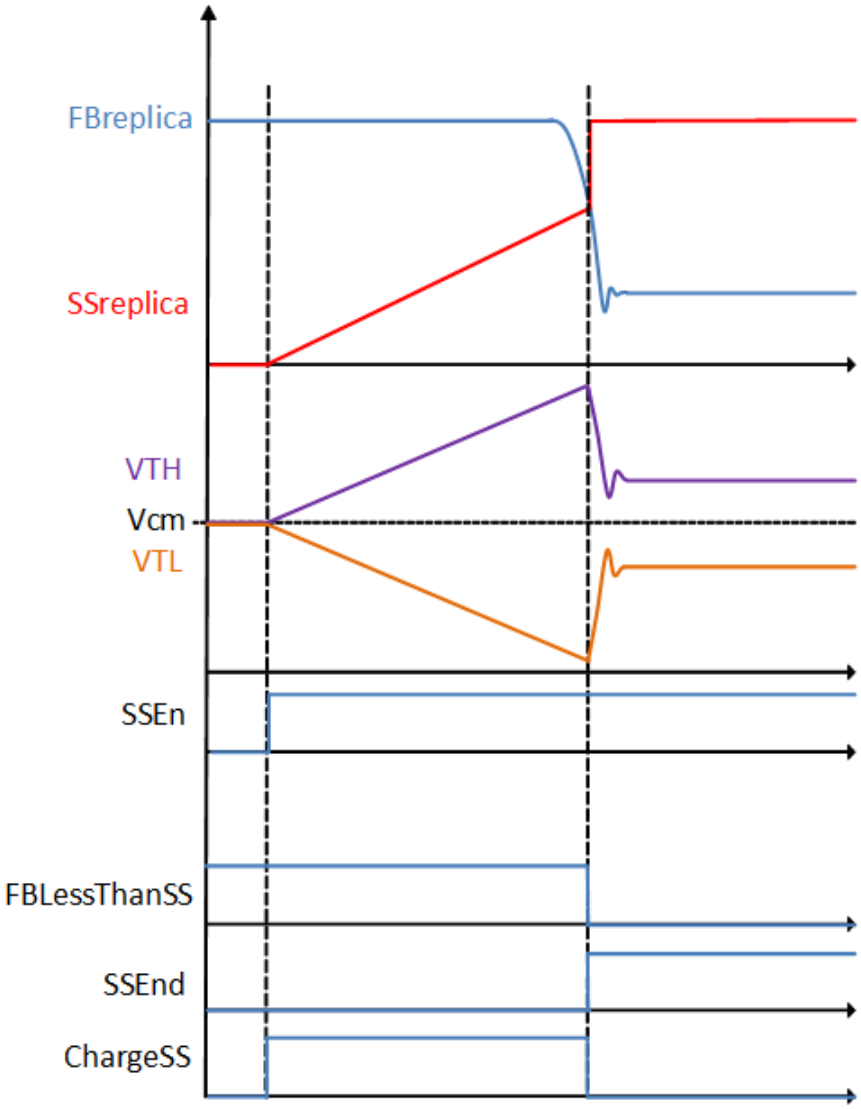

Figure 2. Soft-Start Waveforms

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After exiting the charge boot state, a narrow LO pulse is generated followed by a narrow HO pulse. After these initial two pulses, switching action is determined by comparing the VCR voltage to VTH and VTL. When VCR is > VTH, the high-side switch is turned off. When VCR is < VTL, the low side switch is turned off. This is illustrated in Figure 3

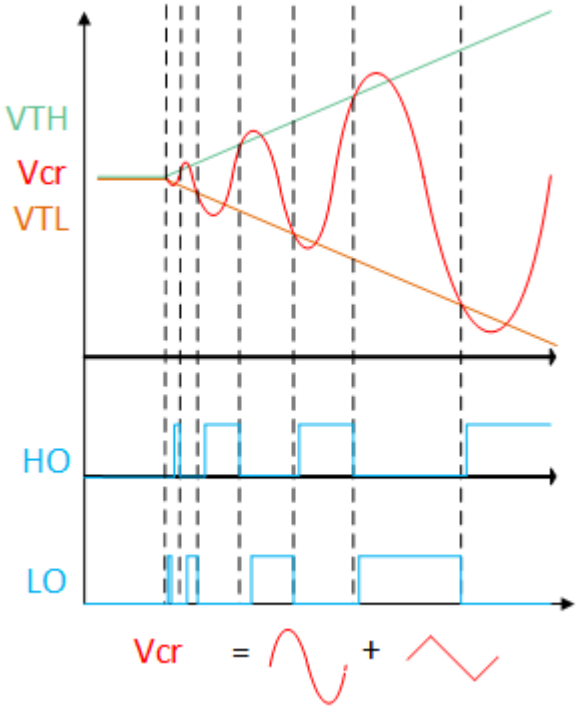

Figure 3. Soft-Start Switching

The soft-start time is determined by three items: the capacitance connected to the SS pin, the capacitance of the VCR divider and the FB signal. The switching frequency during soft start is determined by the capacitance connected to the SS pin and the capacitance of the VCR divider. For further insight, the relationship between switching frequency f_{sw} and control effort V_{COMP} is expressed in Equation 1:

$$V_{COMP} \approx \frac{C_1}{C_2}\frac{1}{C_r} \times I_{in\,(avg)} \times \frac{1}{f_{SW}} + I_{comp} \times \frac{1}{C_2} \times \frac{1}{2f_{sw}} \quad (1)$$

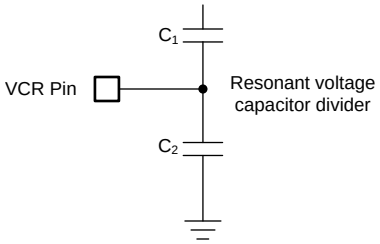

Figure 4. VCR Pin Capacitor Divider

C_1 and C_2 form the capacitive divider connected to the Vcr pin. During startup, V_{COMP} is open loop controlled by the soft-start capacitor connected to the LL/SS pin. By increasing the capacitance of C_1 and C_2 while keeping the same divider ratio (C_1 / C_2), the soft-start switching frequency is reduced. When the C_1 and C_2 capacitance is increased, the power stage delivers more energy to the output during each switching period due to the lower switching frequency. As such, the soft-start time will also reduce. Conversely, when the capacitance of C_1 and C_2 is decreased, the switching frequency during startup is increased and the soft-start time is increased.

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Increasing the soft-start capacitance increases the switching frequency and soft-start time. Decreasing the soft-start capacitance reduces the switching frequency and soft-start time. But for the first few cycles, when the system has the highest switching frequency, changing the soft-start capacitance usually has smaller impact than changing the VCR capacitor.

Table 1. Soft-Start Timing And Switching Frequency Tuning

	Startup Switching Frequency	Soft-Start Time
Increase C_1 and C_2 capacitance (C1 / C2 ratio kept constant)	Decreases switching frequency during startup	Shortens soft-start time
Decrease C_1 and C_2 capacitance (C1 / C2 ratio kept constant)	Increases switching frequency during startup	Lengthens soft-start time
Increase soft-start capacitance	Increases switching frequency during startup	Lengthens soft-start time
Decrease soft-start capacitance	Decreases switching frequency during startup	Shortens soft-start time

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3 Burst Mode Design

3.1 Burst Mode Threshold Tuning

The *Burst Mode Programming* section in UCC25630x data sheet has already described a method to set the burst mode threshold to work with different input voltages. If the system does not need the burst mode threshold to adaptively change with input voltage, there is a simpler method to set the burst mode threshold. The detailed steps are as follows:

1. Disconnect the upper resistor on the LL/SS pin resistor divider temporarily from RVCC pin as shown in Figure 5.
2. Connect an external DC voltage source to the upper resistor as shown in Figure 5. Run the system at the desired load condition where the system enters into burst mode, and then tune the DC source voltage to change the burst mode threshold. Record the DC source voltage, Vext, when the system operates at the boundary between burst and non-burst mode. The UCC25630x data sheet *Burst Mode Programming* section has provided the relationship between V_{LL} and BLK pin voltage V_{BLK}. V_{LL} is calculated as:

$$V_{LL} = \left\{ \left(\frac{V_{ext} - V_{BLK}}{R_1} \right) - \left(\frac{V_{BLK}}{R_2} \right) \right\} \times 250\ k\Omega \quad (2)$$

3. Calculate the required R_1, if it is connected to the RVCC pin.

$$R_{1new} = \frac{(V_{RVCC} - V_{BLK}) \times R_1}{V_{ext} - V_{BLK}} \quad (3)$$

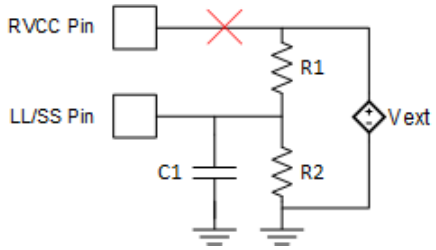

Figure 5. Burst Mode Threshold Tuning Circuit

3.2 Burst Mode Related Issue Debug

This section discusses several possible issues that may appear related to burst mode operation.

- Unstable burst frequency
- Resonant current overshoot during burst

When the system operates at burst mode, the switching frequency and the resonant current should be nearly constant. If this is not observed, the following waveforms should be checked:

1. Measure the boot capacitor voltage to make sure the voltage is higher than the turn-on threshold during burst off period of the selected power device. If there is not enough energy left in the boot capacitor, the high-side gate may not be turned on for a few switching cycles, which may result in unstable burst frequency.
2. Measure the VCR pin voltage waveform. The VCR peak-to-peak voltage should be approximately equal in amplitude for each burst on cycle. If VCR voltage appears to vary cycle to cycle, check the layout, especially around the BLK and LL/SS pins. This is because the burst mode threshold voltage is determined by both BLK voltage and the current flowing into the LL/SS pin. Both pins should have short ground connections. The filtering capacitors should be placed as close to the pins as possible. If there is an overshoot on VCR voltage and the number of burst cycles become larger than expected, it is typically caused by optocoupler saturation. When optocoupler comes out of saturation, there is a long delay. This causes a condition when the secondary-side optocoupler current is changing rapidly, but the primary-side optocoupler current does not change. This causes an overshoot on the resonant capacitor voltage and current. A solution to mitigate this issue is introduced in Section 5.2.

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4 VCR Pin Tips and Tricks

4.1 Use Low Distortion Capacitors

Since the VCR pin voltage directly impacts the gate signals, it is critical to have a clean VCR voltage with low distortion. Distortion on the VCR pin voltage may cause unstable operation. Capacitors with low voltage coefficient, that is, the capacitance does not change much with the applied voltage, should be used. An NP0 ceramic capacitor or film capacitor have good voltage coefficient and are recommended to be used here.

4.2 Add Additional Circuitry on VCR Pin

Add a small resistor between the VCR pin and the middle point of the capacitor divider as shown in Figure 6 will effectively add an offset on the V_{COMP} signal, thus changing the switching frequency. This circuit can be used to increase the switching frequency during soft start.

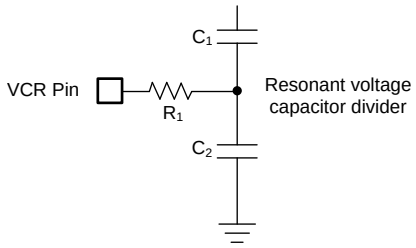

Figure 6. Additional Circuitry on VCR Pin

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5 Feedback Circuit

5.1 Optocoupler Selection Considerations

If an optocoupler is used in the feedback circuit, the following selection guide is suggested:

- Select an optocoupler with high CTR (> 100%) for lower standby power consumption
- Select an optocoupler with high speed ([rise time + turn on time] or [fall time + turn off time] < 5 µs) for better no-load to full-load transient performance
- Select an optocoupler with smaller CTR variation (suggested ratio between maximum and minimum is less than 2) for consistent performance across temperature.

5.2 Circuits to Avoid Optocoupler Deep Saturation

Figure 7 shows the feedback chain block diagram. Normally, FB pin voltage is kept constant to achieve a fast feedback loop. At very light load, the feedback optocoupler may draw a current larger than the current source IFB. The FB pin voltage will drop and optocoupler may get saturated. Once the optocoupler is saturated, a delay will be present when the optocoupler comes out of saturation. This delay may cause resonant current overshoot during burst mode, and V_{OUT} may dip out of specification during a transient from no load to full load.

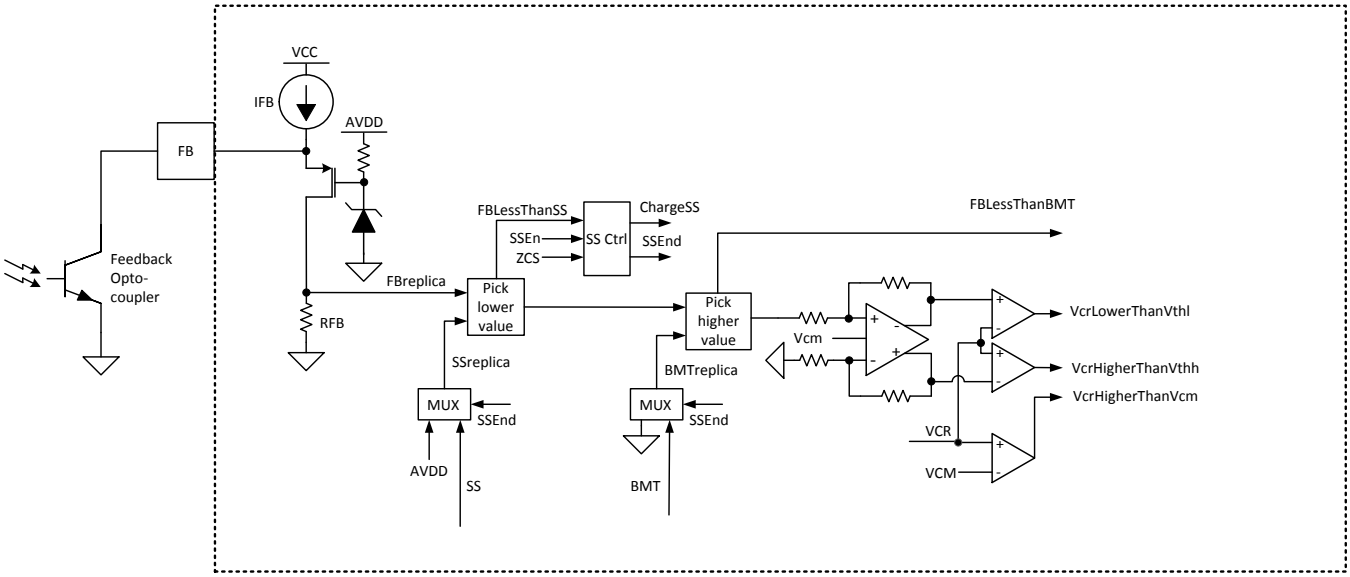

Figure 7. Feedback Chain Block Diagram

The following two methods can be used to avoid the optocoupler saturation issue:

1. Add a Zener diode and a series resistor between the RVCC pin and FB pin as shown in Figure 8. The Zener diode voltage should be selected as RVCC typical voltage minus FB typical voltage. In normal operation, there will be very little current flowing through the Zener but when FB voltage begins to decrease, it will provide extra current to prevent FB voltage drop. For example, a 6.1-V Zener diode and 10-kΩ resistor is used in the UCC256301 EVM.

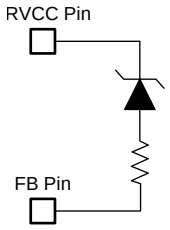

Figure 8. Circuit I to Avoid Optocoupler Saturation

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2. Limit the photo diode current using the circuit in Figure 9 to make sure the optocoupler does not draw current higher than IFB. Therefore, the FB pin voltage can be maintained constant. The maximum photo diode current can be derived based on the IFB and selected optocoupler CTR. The Zener diode and the resistor should be sized to limit the photo diode current below the maximum value.

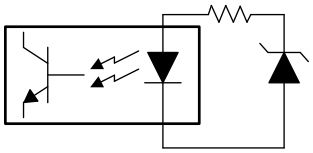

Figure 9. Circuit II to Avoid Optocoupler Saturation

6 Optimize the System for Audible Noise

6.1 Adjust Burst Mode Threshold Level

Burst mode threshold can be easily adjusted with the method mentioned in Section 3.1. Using a lower burst mode threshold will make the switching frequency during burst on period higher. Higher switching frequency will result in a smaller resonant current, which flows through the transformer. The audible noise is positively related to the resonant current magnitude. Therefore, lower burst mode threshold can reduce the audible noise.

6.2 Soft Burst On Circuit

Another method to optimize the audible noise is to slowly increase the resonant current when entering the burst on period. Figure 10 shows the additional circuitry to achieve soft burst on.

1. A small resistor R_1 is added in series with the bottom capacitor on the VCR pin. Similar to the circuit in Section 4.2, it can raise the switching frequency.
2. In burst mode, R_2 and C_3 create a ramp out of low side gate signal (LO). The ramp controls MOSFET Q_1 and turns Q_1 into a variable resistor. The Q_1 resistance decreases as the C_3 voltage increases. Therefore, in the first few burst on cycles, the switching frequency is high and slowly decreasing, which makes the resonant current slowly increase.
3. During normal operation, C_3 voltage is high enough to make Q_1 fully conduct to bypass R_1.

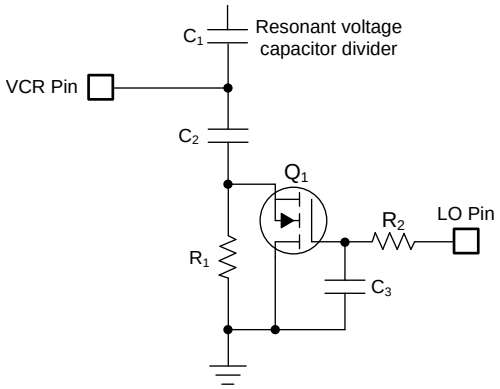

Figure 10. Soft Burst on Circuit

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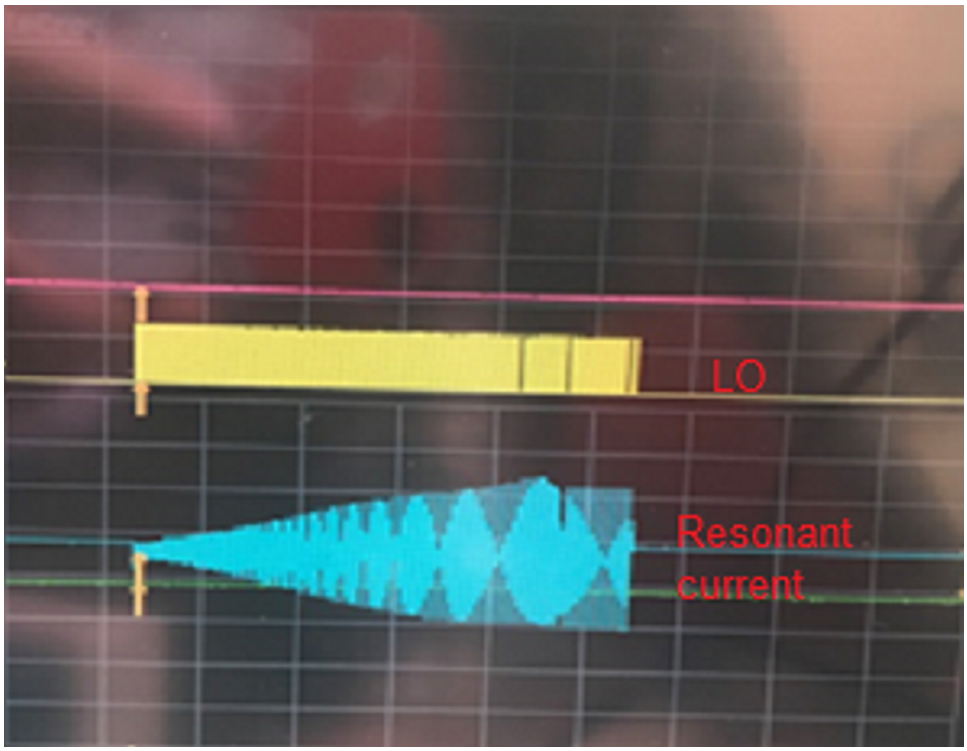

Figure 11. Test Waveform With Soft Burst on Circuit

7 Layout Guidelines

7.1 Layout Recommendation

Follow the subsequent layout recommendations:

- The filtering capacitor on BW, ISNS, BLK should be put as close as possible to the pin. The ground loop of these pins should be as small as possible.
- Add necessary filtering capacitors on the BW pin to filter out the high spikes on the bias winding waveform. It is critical to filter out the high spikes because internally the signal is peak detected and then sampled at the low side turn off edge.
- FB trace should be as short as possible.
- Place the soft-start capacitor as close as possible to the LL/SS pin.
- Use film capacitor or NP0 ceramic capacitor on the VCR divider and the ISNS capacitor.
- The ISNS resistor should be less than 500 Ω to keep the node impedance low.
- The boot capacitor needs to be sized based on the minimum burst frequency, refer to the boot leakage current in the electrical table. Recommended minimum 0.1-µF capacitor.
- Do not put any capacitor on the HV pin to ground. The layout of this pin should result in low parasitic capacitance (< 60 pF) from HV pin to ground.
- Use large copper pour around GND pin.
- Keep necessary high voltage clearance.

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7.2 Layout Examples

Figure 12 gives an example for single-layer layout. Figure 13 gives an example of the layout in the EVM. More details are found in *Using the UCC25630-1EVM-291*.

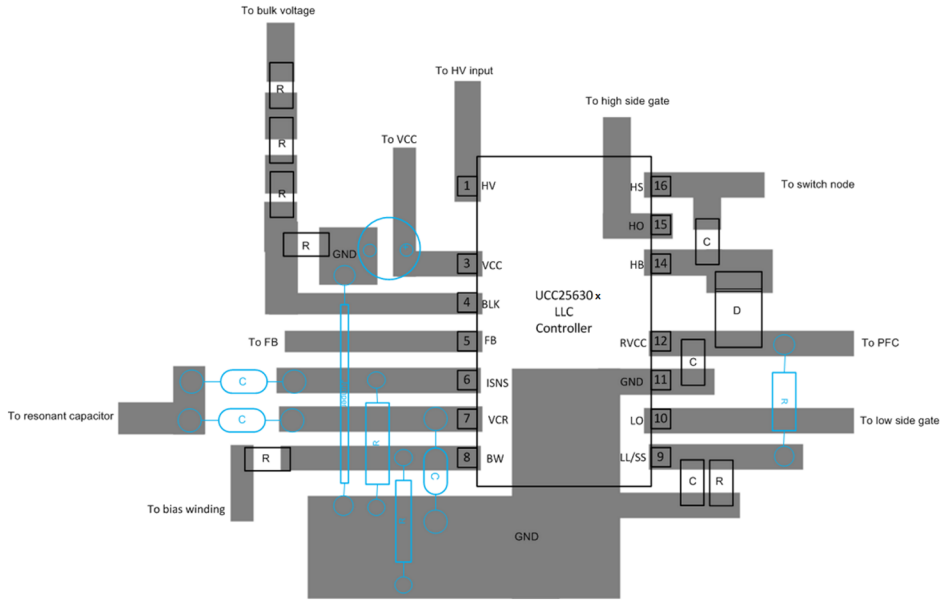

Figure 12. Single-Layer Layout Example for UCC25630x Surrounding Circuits

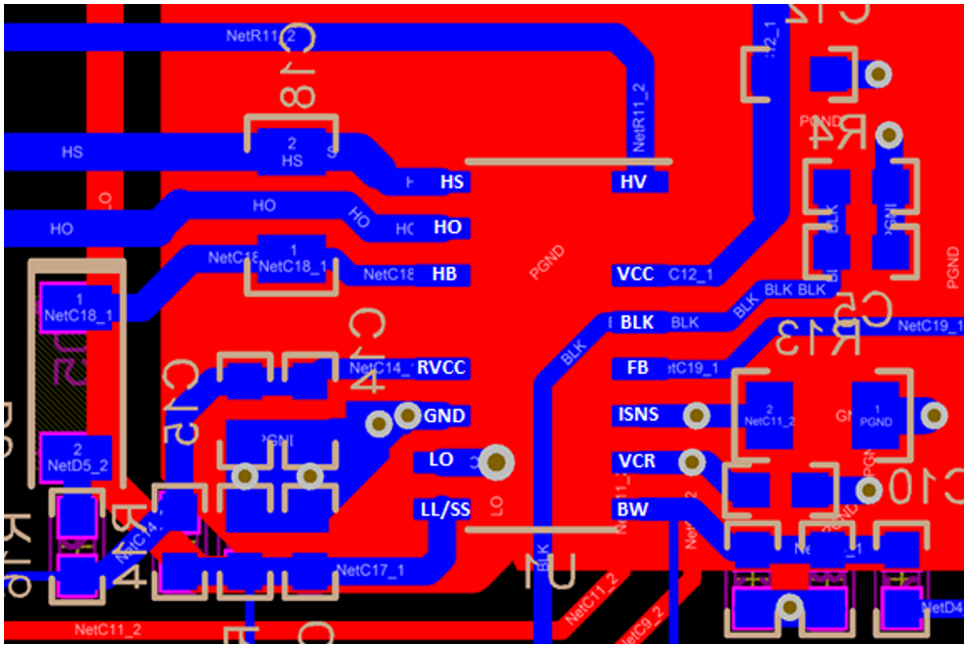

Figure 13. Layout Example for UCC25630x Surrounding Circuits in EVM

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8 System Bring Up Procedure and Debugging Notes

Section 8.1 through Section 8.12 provide system start-up procedures or notes on debugging:

8.1 Bring Up Procedure

1. Check the HV pin. AC or DC voltage should be available.
2. Check the VCC voltage, it should be charged to 26 V and then go down.
3. Check the RVCC voltage, it should start when VCC reaches 26 V, and should stay at 12-V constant. If RVCC goes up and down every 1s, it means that there is a fault condition.
4. Check the BLK, ISNS, and BW pins for input voltage OVP and undervoltage protection (UVP), overcurrent protection (OCP), output OVP protections.
5. Check gate pulses. A long LO pulse is an indicator of system restart.
6. Check FB pin voltage. If the FB pin is pulled low, the system will not start switching.

8.2 HV Pin

- When x-cap discharge is disabled, this pin can connect to either AC or DC.
- When x-cap discharge is enabled, this pin can only be connected to AC. Connecting this pin to DC may not break the device, but system will consume more power and may run into overtemperature protection
- For debugging purpose, the current flowing into the HV pin can be measured by the voltage across the HV pin series resistors.

8.3 VCC Pin

- JFET is turned on when VCC drops below 10.5 V.
- JFET is turned off when VCC reaches 26 V.
- When VCC reaches 26 V, RVCC turns on.
- VCC should be kept above 13 V during normal operation to give RVCC enough headroom.

8.4 BLK Pin

- This pin has both overvoltage and undervoltage protection.
- This pin is a high impedance node. The voltage divider lower resistor and the filtering cap should be put as close as possible to the pin.
- The voltage on this pin is used for burst mode threshold generation, so a clean BLK voltage waveform is impotent for stable burst operation.

8.5 FB Pin

- The voltage on this pin does not move during normal operation (unless the optocoupler is saturated), so adding a capacitor from the FB pin to ground does not add a pole to the system.
- Adding a resistor from the FB pin to ground can set a maximum clamp on V_{COMP} level. This can be used for maximum power level, maximum input current, and minimum frequency clamp.

8.6 ISNS Pin

- Use < 500-Ω resistor on the ISNS pin.
- Too much low pass filtering on ISNS may result in a delay in resonant current polarity sensing and error in overcurrent protection.
- Inside the ISNS pin, input current is reconstructed and averaged.
- To set OCP level:
  - Calculate the desired input current level (in amps) for OCP.
  - Set the desired current sense ratio by adjusting R_{ISNS} and C_{ISNS}.
- Peak OCP level is 5 V during soft start and 4 V during normal operation.

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- Adding some low pass filtering on ISNS may help avoid OCP1 tripping during the first few switching cycles.

8.7 VCR Pin

- The ratio between Cupper and Clower on the VCR pin should be determined by the maximum peak-to-peak resonant capacitor voltage waveform. The maximum VCR pin voltage peak to peak should be less than 6 V.
- Lower Clower results in a higher switching frequency at a given V_{COMP} level.
- Putting a small series resistor between the VCR pin and the mid-point of the capacitor divider can help increase the switching frequency of the first few startup cycles and reduce inrush current.
- The internal 2-mA current source is on during dead time. If VCR voltage rails out to 0 V during burst, it means that the dead time is very long. This is usually caused by the boot capacitor too small and the high-side gate does not turn on.

8.8 BW Pin LL/SS Pin

- The voltage level on the negative half cycle on BW is sampled and compared with OVP comparator.
- Add necessary low pass filtering on this pin if there are high spikes on the BW signal.

8.9 LL/SS Pin

- This pin should have a small ground loop
- Removing the top resistor on the resistor divider will set the burst mode threshold to the minimum value: 0.4 V.

8.10 LO

- A long LO pulse at the beginning of switching is used to charge the boot capacitor.

8.11 RVCC

- Whenever a fault happens (except ZCS fault), RVCC will be shut off and the system will retry startup every 1s.
- RVCC supplies the gate driver and various internal circuits.
- RVCC is also used as a reference for burst mode generation, so a clean RVCC waveform is very important for stable burst operation

8.12 HS, HO, HB

- High-side gate has UVLO protection.
- If one high-side pulse is missing, it usually means that the boot voltage is not enough.
- System state machine will not react to boot UVLO protection.

9 References

For additional references, see:

- Texas Instruments, *UCC256301 Enhanced LLC Resonant Controller with High Voltage Gate Driver Data Sheet*
- Texas Instruments, *Using the UCC256301EVM-291 User's Guide*

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2017) to A Revision	Page
• Redid *Soft-Start* section.	1
• Deleted *Adjust VCR Pin Capacitance to Change Start Up Switching Frequency* section.	7

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