Application Report
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Improving Efficiency of DC-DC Conversion through Layout

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ABSTRACT

Server, Telecom, Automotive, and Industrial power supply applications frequently use resonant converters for the DC-DC Conversion portion of the system. Some automotive applications, specifically hybrid electric vehicles (HEV) and electric vehicles (EVs), require bidirectional DC-DC converters to charge the low-voltage battery (12 V) during normal operation (buck mode) and charge the high voltage battery during emergency events (boost mode). Resonant converters are good solutions for medium and high power applications because of their efficiency and power density. To help minimize switching losses from the power FETs and achieve higher system efficiency, designers often use a low-side driver + FETs (on the secondary side of the transformer) to work as synchronous rectifiers in buck mode and as push-pull switches in boost mode. An optimized layout on the gate drive portion of the circuit is necessary to reduce system losses, to meet industry standards, and meet the ever-increasing power density requirements.

This application report discusses layout considerations and guidelines of the key components from the perspective of a gate driver using the UCC27524A in order to minimize switching losses and increase the overall system efficiency and robustness.

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Trademarks

1 Introduction

Automotive applications commonly use DC-DC converters as shown in Figure 1. This block diagram shows phase-shifted full-bridge topology (PSFB) with synchronous rectification to control power flow from a high voltage bus (400 V) to a low voltage (12 V–24 V battery) in step-down mode. A push-pull stage controls the reverse power flow from the low-voltage battery to the high-voltage bus in boost mode during abnormal conditions. On the push-pull stage, designers frequently use power switches over diodes to help improve the system efficiency.

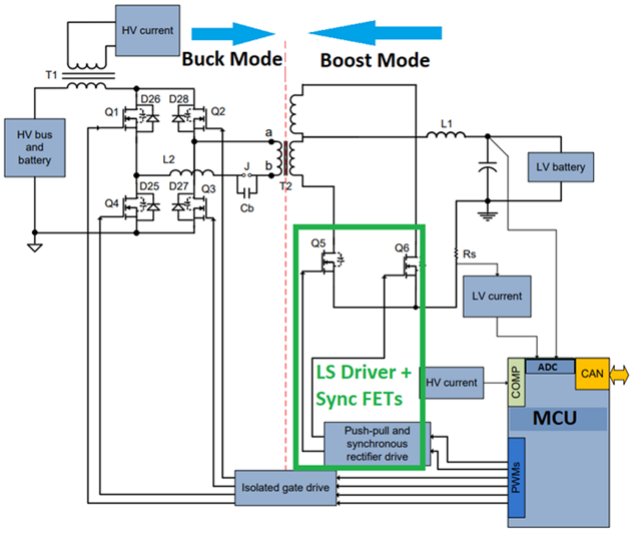


Figure 1. Block Diagram of a Bidirectional DC-DC Converter

2 Layout Guidelines

From the perspective of a gate driver, an optimized PCB layout is critical in order to reduce switching losses from the FETs and achieving higher system efficiency. It is therefore necessary to prioritize the following guidelines during the layout process to minimize the impact of noise in the design for optimum system performance:

1. Use low ESR/ESL decoupling capacitors and place them directly across the supply pin of the driver to minimize PCB trace inductance between the decoupling capacitors and the supply pin of the driver.
2. Place the FETs and other gate components (resistors, anti-parallel diodes, clamp diodes, and so forth) as close as possible to the output pins of the driver to minimize trace inductance. Because stray inductance is directly proportional to PCB trace length and inversely proportional to PCB trace width as shown on Equation 1, use short and wide traces to connect these components to the output pin of the driver.
    a. Check the turn-on and turn-off current loop path (driver, power MOSFET and VDD bypass capacitor) and ensure these components occupy a minimal physical PCB area. Small turn-on/off loops reduce parasitic inductance in the gate drive loop which minimizes switching noise especially evident for higher dv/dt applications or DC-DC converters with higher power ratings.
3. Separate power traces (the output of the driver) and signal traces (the input of the driver) to minimize effects of ground bounce and noise. The pulsating current required to turn-on/off the FETs create noise on the power stage. Noise coupling between the power traces and the signal traces could damage the controller, cause false triggering as well as driver malfunction. It is therefore important to route the power traces containing the noisy high peak current on separate areas of the PCB board.
4. Use large heavy copper planes to connect the decoupling capacitors to the ground/VDD thermal pad to improve the thermal performance of the device.
5. Use ground planes to help shield noise and help with power dissipation from the high frequency

switching.

6. If protection components like clamping diodes and snubbers are desired, place them very close to the device they are intended to protect if protection components like clamping diodes and snubbers are desired.

3 Gate Drive Critical Loops

From the perspective of the gate driver, there are three important loops to keep in mind during layout to minimize loop inductance and maximize the performance and efficiency of the system. In Figure 2, L_{src} (in green) shows the path of the peak currents required to turn on the synchronous FETs. When the driver receives a “High” command from the controller, the driver output goes high, and the decoupling capacitor, C_{VDD}, provides the necessary peak current to charge the gate capacitance of the FET.

The next loop, equally important, L_{snk} (in red), is the discharge path of the gate capacitance necessary to turn-off the FET. These loops have a large impact on the switching performance as they directly impact the rise and fall times of the synchronous FETs. It is critical to minimize these loops as much as possible to reduce the inductance in the gate drive loop. Significant inductance on these loops limits the drive current and cause ringing at the gate.

The third loop, L_{MCU}, is the controller return ground loop which is less critical than the previous two. Small RC filters as close as possible to the input pins of the driver, are a good way to help reduce spikes generated from the common mode current path and ground bounce. L_{src} and L_{snk} must have the highest level of priority, followed by the controller ground return loop L_{MCU}.

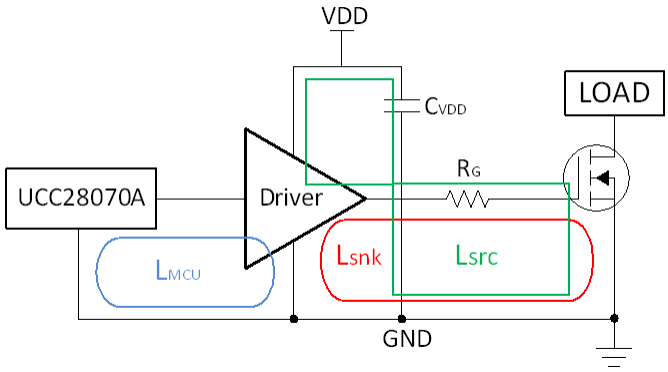


Figure 2. Gate Drive Critical Loops

4 Effects of Parasitic Inductance on Gate Drive Loop

Parasitic inductance in the high di/dt current loops L_{src} and L_{snk} in Figure 2 cause large voltage spikes in the gate drive portion. This results in EMI in the system degrading the performance and overall efficiency. It can also cause device and circuit malfunction when these large voltage transients exceed the absolute maximum operating ratings of the devices in the circuit. The inductance in these loops over a ground plane is directly proportional to the length of the PCB traces and inversely proportional to the width of the trace. You can estimate this inductance knowing the length (l), height (h), and the width (w) of the trace from the following formula:

$$L\left(\frac{nH}{cm}\right) = \frac{2 \times h \times l}{w} \quad (1)$$

To illustrate the impact of the parasitic inductance in these loops, use Figure 3 to simulate the gate drive portion frequently seen in DC-DC converter applications using the UCC27524. Drive both the input channels with a 5-V_{pp}, 400-kHz square wave. On the output side, OUTA connects to synchronous FET Q_1 through R_A using a short PCB trace estimated at L_2 = 20 nH while OUTB drives Q_2 through R_B using a long PCB trace simulated by L_5 = 400 nH. The driver is biased with a 12 V supply and both ENA/ENB pins are externally pulled to VDD. I_A and I_B measure the respective gate currents seen at the gates of the synchronous FETs Q_1 and Q_2. L_3 and L_4 represent the respective source inductances of the FETs Q_1 and Q_2.

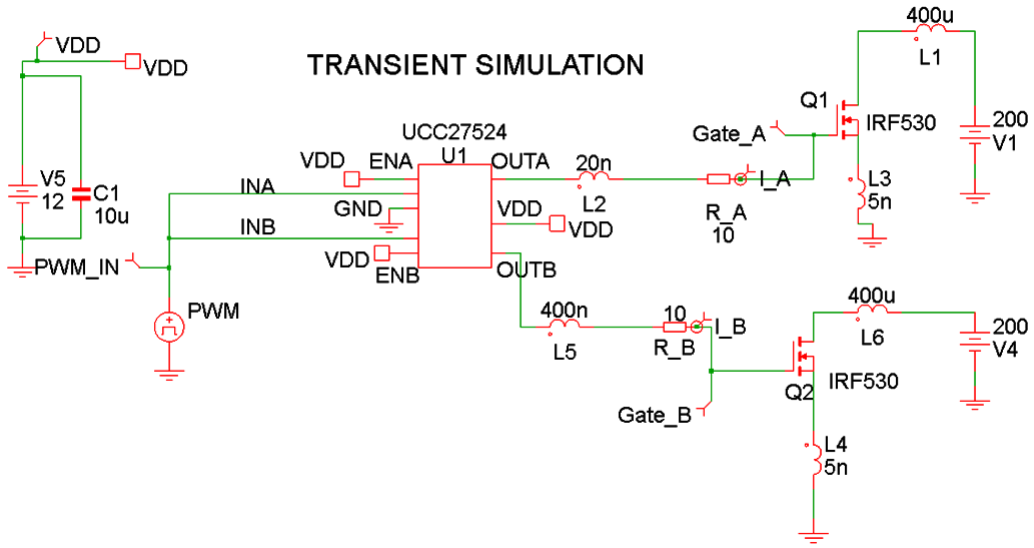


Figure 3. Example Simulation of Parasitic Inductance in Gate Drive Portion

Figure 4 shows the simulation results where the parasitic inductance represented by L_5 reduces I_GateB to about 300 mA which compromises the gate voltage of Q_2 labeled as V_gsB and causes significant ringing. This can compromise the efficiency of the overall system, and increase the presence of EMI in the system. The observed overshoot, undershoot at the gate can also damage the FET and potentially the driver when it exceeds the ratings of these devices.

On the second channel, the gate current (with the least amount of parasitic inductance between the output stage of the driver and the gate of the MOSFET) I_GateA, reaches a higher peak value and allows smooth rise and fall transients seen at the gate V_gsA of the corresponding FET Q_1.

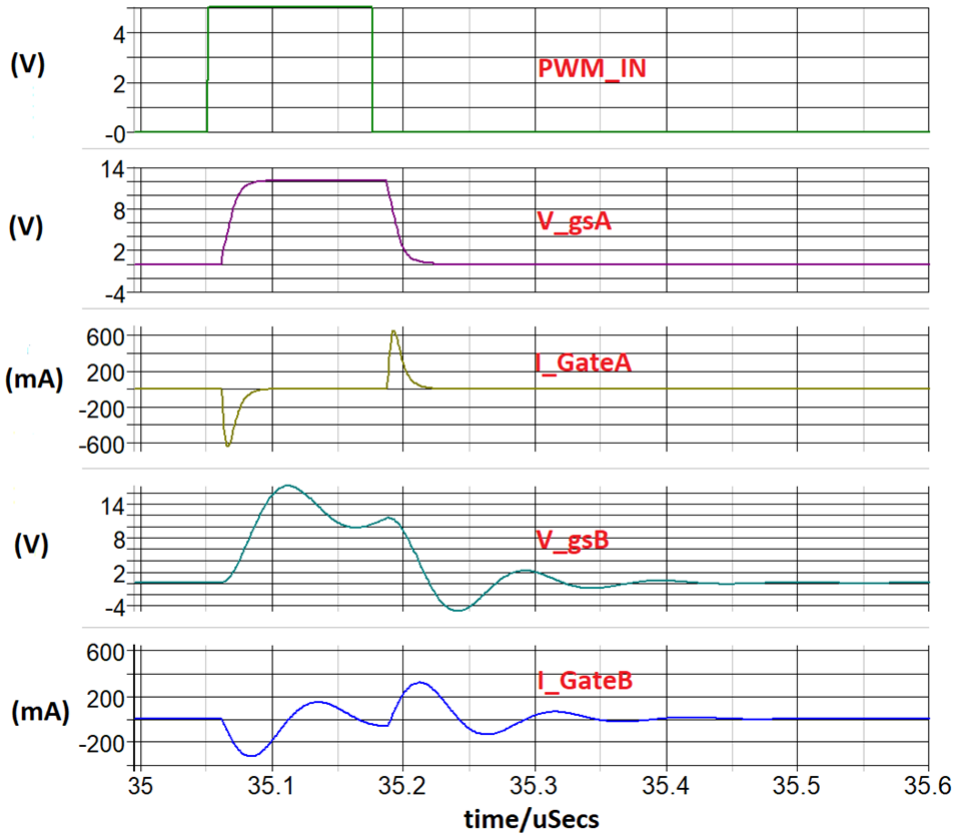


Figure 4. Simulation Results

To further illustrate the important of driver and FETs placement, use the schematic in Figure 5 to drive two FETs. Place Q_5 very close to OUTA while Q_6 connects to OUTB through long PCB traces. Drive both channels with the same 5 V, 100 kHz PWM signal.

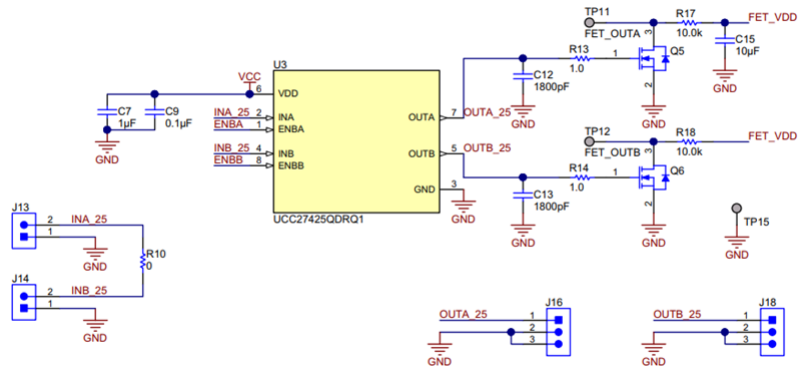


Figure 5. Gate Drive Bench Data Schematic

Channel-1 on the waveform in Figure 6 captures the input PWM signal while OUTA (Channel-2, blue) and OUTB (Channel-3 in red) capture the gate voltages of Q_5 and Q_6 respectively. Channel-4 (the green waveforms) shows the supply range at 12 V. There is significant overshoot and ringing at the gate of Q_5 caused by the stray inductance between the gate drive output stage of channel B and Q_5. As a result, the overshoot reaches a 6.5 V peak voltage and this high frequency ringing can introduce EMI in the circuit and compromise the performance of the design. Channel-2 shows a much cleaner gate voltage with little ringing demonstrating the improvement due to the placements of the FETs.

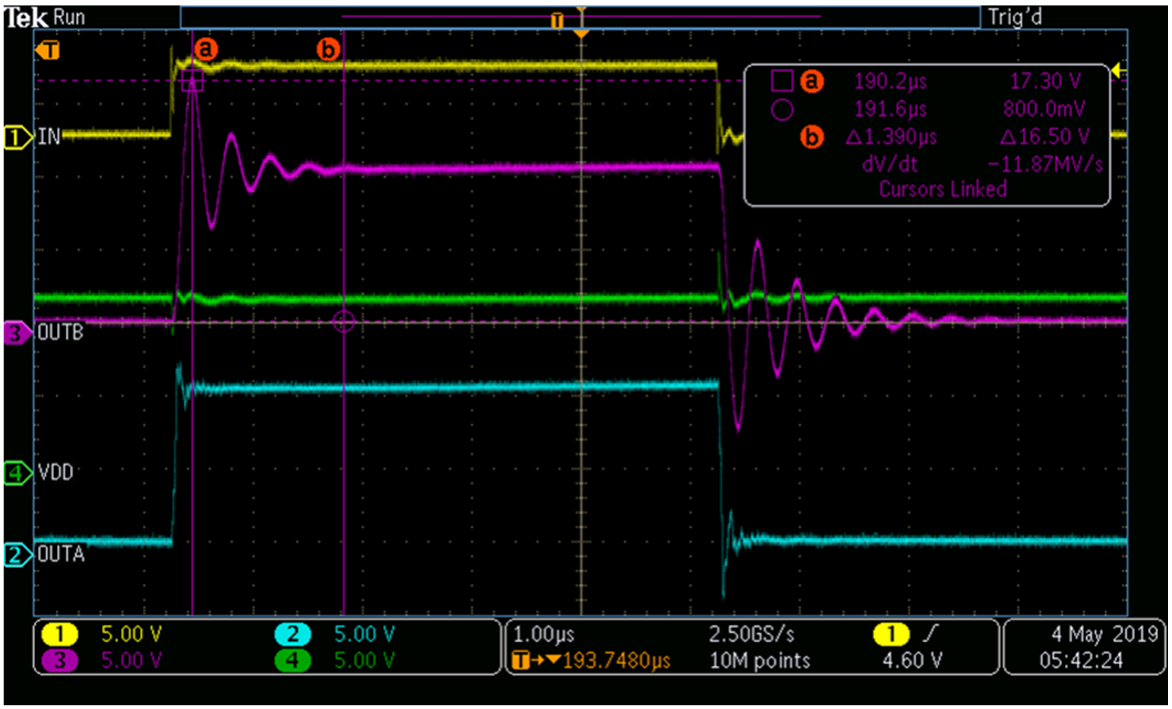


Figure 6. FETs Placement Comparison

5 Decoupling the Placement of the Capacitor

For effective filtering, the bypass capacitors must remain as close as possible to the supply pin of the driver. Because of their stability over temperature and bias, TI recommends X5R/X7R ceramic capacitors. Use Figure 7 to show the effects of PCB traces between the decoupling capacitors and the supply pin of the driver. Channels-1 (yellow), 2 (blue), and 3 (red) capture respectively the input, output, and the supply voltages of the driver in a typical gate drive circuit. On the left, the decoupling capacitor connects to the supply pin of the driver through long wires adding stray inductance on the supply. As a result, the ability of the capacitor to filter noise is significantly reduced causing ringing on both the supply and the output of the driver. If the noise on the supply is significantly high, it can exceed the absolute maximum rating and damage the driver. If the supply drops below the UVLO (under voltage lockout) threshold of the device, it can cause the driver to turn off instantaneously.

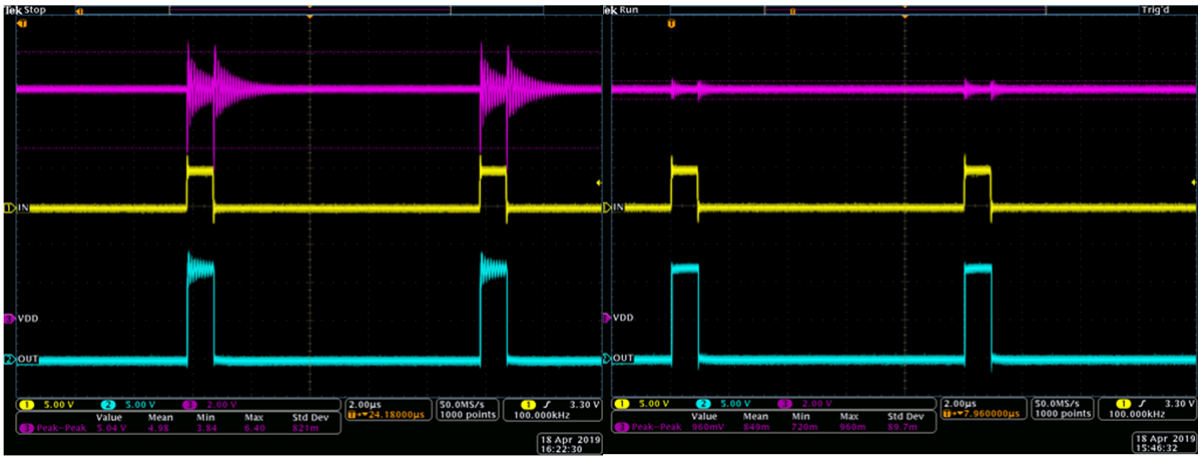


Figure 7. Effects of the Placement of the Decoupling Capacitor

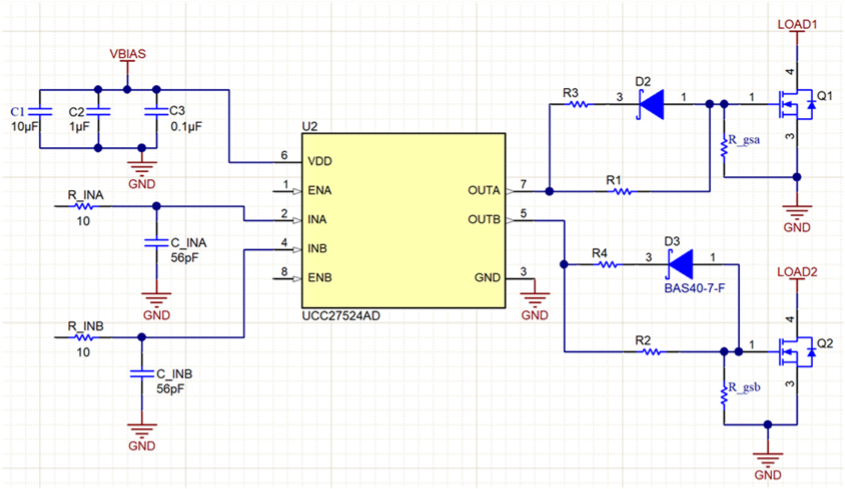
6 Example Schematic and Layout

Figure 8 is a typical gate drive using a dual low-side driver. The channel turns on Q_1 through the R_1 and turns off the FET through the anti-parallel diode D_2 and the series resistor R_3. OUTB of the driver delivers the peak turn-on current supplied by the decoupling capacitors C_1, C_2, and C_3 through the R_2 and turns-off Q_2 through D_3 and R_4.

Figure 8 shows an optimized gate drive circuit layout with the turn-on and turn-off paths highlighted in green and blue. This layout confines the peak current to a minimum physical area; the outputs of the driver connects to the respective FETs through short and thick PCB traces to minimize the issues presented in this app note.

The paralleled decoupling capacitors provide the peak currents necessary to charge and discharge the FETs. Use a copper plane to first minimize stray inductance on the supply and second to help with the thermal performance of the driver relevant for heavy loads and hard switching applications.

Separate digital signal traces (input traces) from the power traces (the output of the drive) to reduce impact of ground bounce on the input signal.



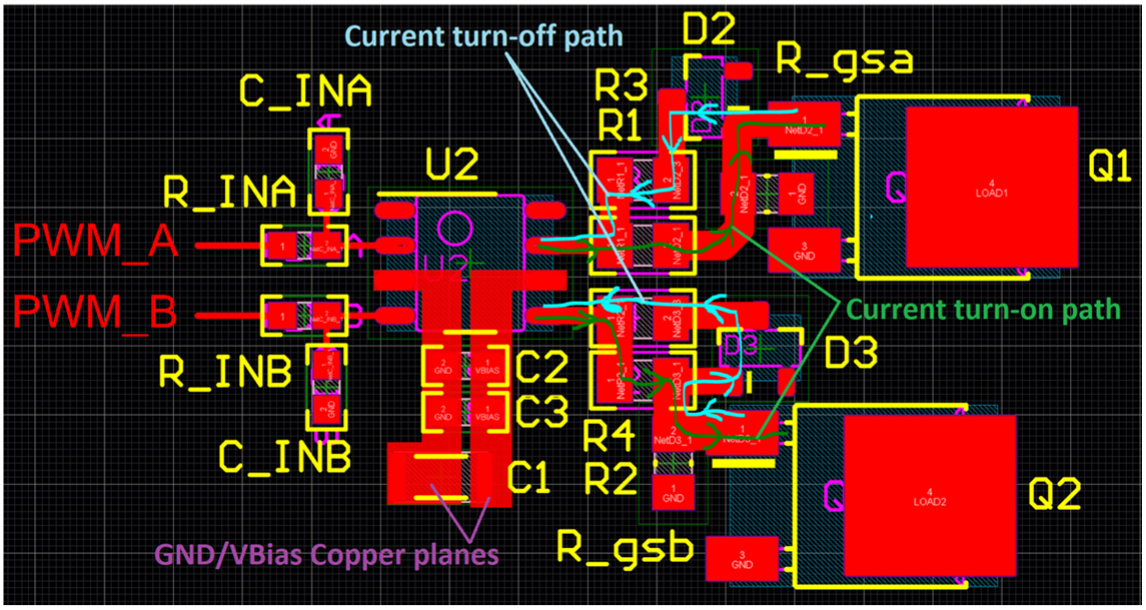


Figure 8. Example Schematic and Layout

7 Summary

This application report discusses layout considerations when using a dual channel low-side driver and shows the impact of a non-optimized layout in applications requiring high efficiency and minimal losses. It also shows an example of an optimized layout using the UCC27524A and shares good practices for an optimized layout necessary for a reliable system performance.

8 References

- *Gate Drivers Products*
- *UCC27524A-Q1 Dual 5-A, High-Speed, Low-Side Gate Driver With Negative Input Voltage Capability Datasheet* (SLVSDH6)
- *UCC27524A Product Folder*

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