Application Report
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UCC27531 35-V Gate Driver for SiC MOSFET Applications

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ABSTRACT

SiC MOSFETs are gaining popularity in many high-power applications due to their significant switching performance advantages. SiC MOSFETs are also available with attractive voltage ratings and current capabilities. However, the characteristics of SiC MOSFETs require consideration of the gate-driver circuit to optimize the switching performance of the SiC device. Although SiC MOSFETs are not difficult to drive properly, many typical MOSFET drivers may result in compromised switching speed performance.

The UCC27531 gate driver includes features and has operating parameters that allow for driving SiC power MOSFETs within the recommended optimum drive configuration. This application note reviews the characteristics of SiC MOSFETs and how to drive them to achieve the performance improvement that SiC can bring at the system level. The features of UCC27531 to achieve optimal performance of SiC are explained and results from a demonstration circuit are provided.

1 Introduction

In the past, the majority of applications such as uninterruptible power supplies (UPS), photovoltaic (PV) inverters, and motor drive have utilized IGBTs for the power devices due to the combination of high-voltage ratings exceeding 1 kV and high current capability. Usable switching frequency of IGBTs has typically been limited to 20–30 kHz, due to the high turnoff losses caused by the long turnoff current tail. Design comparisons have shown that SiC MOSFET designs can operate at considerably higher switching frequency and achieve the same or better efficiency. Although the device cost of the SiC MOSFETs are higher than the equivalent IGBTs, the significant savings in transformer, capacitor, and enclosure size results in a lower system cost.

The availability of Silicon MOSFETs with voltage ratings up to 900 V and low $R_{DS(on)}$ below 150 mΩ is improving. Beyond 900 V, low $R_{DS(on)}$ MOSFETs are not available. Although Si-MOSFET designs can be realized at considerably higher switching frequency than IGBTs, the cost of high-current and high-voltage Si MOSFETs is considerably higher than IGBTs.

2 Advantages of Wide Bandgap SiC

The primary advantage of SiC MOSFETs over Si MOSFETs is the availability of very low $R_{DS(on)}$ and high voltage ratings; up to 1200 V at 25 mΩ. SiC devices are capable of faster switching speeds than Si MOSFETs due to the very low parasitic capacitance and associated charge during switching, refer to Table 1 for details. Although the SiC MOSFET is driven with higher peak-to-peak gate-to-source voltage, per the device recommendation, the total gate charge of the SiC device is over 15 times lower than an equivalent Si MOSFET. A characteristic that must be considered in any converter design is the $R_{DS(on)}$ at the anticipated highest junction temperature. SiC MOSFETs exhibit a much lower increase in $R_{DS(on)}$ at high temperature than Si MOSFETs. The example SiC MOSFET curves indicate approximately 1.25 times increase in $R_{DS(on)}$ from 25°C to 125°C, where the Si MOSFET curves indicate approximately 2.2 times increase in $R_{DS(on)}$. At 125°C the conduction losses are higher on the Si MOSFET since the $R_{DS(on)}$ is approximately 265 mΩ versus the SiC $R_{DS(on)}$ of 150 mΩ.

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Table 1. SiC vs Si MOSFET Parameter Table 900 V, 120 mΩ

900 V/120 mΩ	Q_g (nC)	$t_{d(on)}$ (ns)	t_{rise} (ns)	$t_{d(off)}$ (ns)	T_{fall} (ns)	$R_{DS(on)}$ factor 25–125°C
Si N-Ch	270	70	20	400	25	2.2
SiC N-Ch	17.3	27	10	25	8	1.25

Si IGBT characteristics include high voltage ratings and low saturation voltage at very high current, resulting in the equivalent of a very low $R_{DS(on)}$ MOSFET. The well-known switching frequency limitation of IGBTs is the long current tail during turnoff which can exceed 300 ns even with the higher switching frequency rated devices. The IGBT long collector current fall time results in turnoff switching losses that can be 6 to 10 times higher than SiC MOSFETs.

3 SiC MOSFET Characteristics

SiC MOSFETs have a relatively low transconductance compared to Si MOSFETs. The result is a higher gate-to-source voltage required to achieve the lowest V_{DS} saturation voltage at high drain current. Where most Si MOSFETs achieve low V_{DS} saturation at 8 V to 10 V on the gate to source, SiC MOSFETs typically require 15 V to 20 V V_{GS} to achieve low V_{DS} saturation.

The turnon threshold voltage of SiC is similar or lower than Si MOSFETs which results in a larger V_{GS} transition when the SiC MOSFET is operating as a variable resistance.

The fast switching speed and low turnon threshold of SiC MOSFETs requires a negative V_{GS} level during turnoff. Depending on the device, –2 V to –5 V drive is recommended for SiC devices. Although the MOSFET parasitic C_{DS} (CRSS) is very low, the high V_{DS} dV/dt during turnoff can result in coupling enough charge from the drain-to-gate capacitance to reach the threshold voltage if negative drive and a close-coupled driver layout is not in place.

3.1 MOSFET Switching Transient Process and Effects of MOSFET Parasitics

The details of the MOSFET turnon and turnoff transient events are similar for Si and SiC MOSFETs. Both devices have parasitic C_{DS}, C_{GD}, and C_{GS}. Also Si and SiC C_{GD} and C_{DS} are dynamic, depending on the voltage level, much higher capacitance at a lower voltage level, and C_{GS} is relatively flat. There are detailed studies of the MOSFET switching transients from universities and device manufacturers. The following is a general summary of the switching transients in a continuous current power train for reference.

3.1.1 MOSFET Turnon Transient

The turnon event is generally the process of charging the MOSFET parasitic capacitances to the voltage level required to achieve low $R_{DS(on)}$. A basic step-by-step process is presented. Refer to Figure 1 and Figure 2 for the current flow and timing illustrations:

1. Pulse-width modulation (PWM) and driver start charging C_{GS} to the MOSFET turnon plateau.
   - The MOSFET plateau is defined as the V_{GS} threshold plus the voltage delta required to conduct the current amplitude flowing in the inductor, I_L. The transconductance of the MOSFET and current level determine the additional voltage required over the threshold voltage.
2. At the V_{GS} plateau, the V_{DS} begins to fall to ground. During the fall time to ground, the negative dV/dt of the drain generates a current flowing through C_{GD} that opposes the current from the gate-driver circuit, known generally as Miller effect current. The duration of this current flow is the V_{DS} fall time. Also note that the internal FET gate terminal is a lower voltage potential than observed on the gate terminal, due to the Miller current flowing into the internal FET resistance, R_G.
3. After the V_{DS} fall time, the gate is charged to the level determined by the driver source voltage. The MOSFET achieves the lowest $R_{DS(on)}$ based on the particular device parameters. Typically 8–10 V for high voltage Si MOSFETs and 15–20 V for SiC MOSFETs.

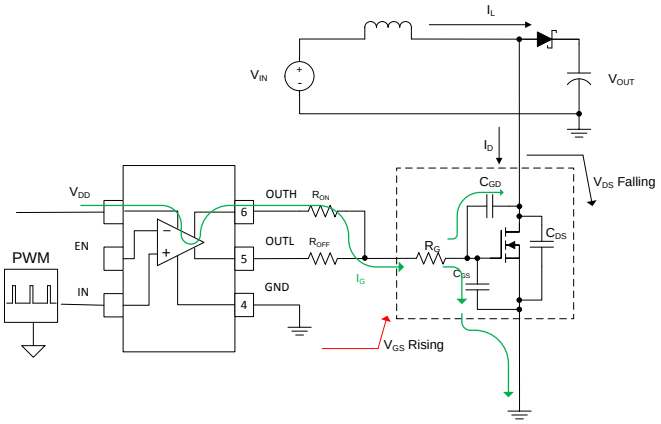

Figure 1. Turnon Circuit with Parasitic Capacitance

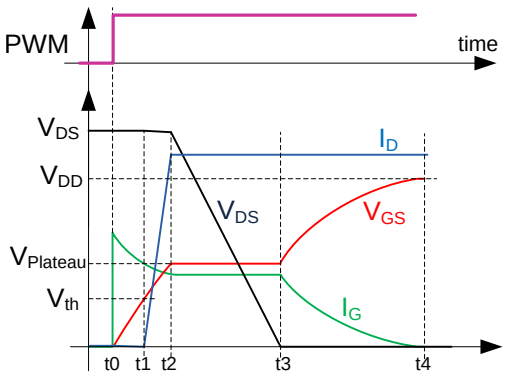

Figure 2. Turnon Waveform

3.1.2 MOSFET Turnoff Transient

The turnoff event is generally the process of discharging the MOSFET parasitic capacitances to the voltage level required to achieve the off state. A basic step-by-step process is presented in the following list. Refer to Figure 3 and Figure 4 for the current flow and timing illustration.

1. PWM and driver start discharging C_{GS} to the MOSFET turnoff plateau.
2. At the V_{GS} plateau, the V_{DS} begins to rise from ground. During the rise time of V_{DS}, the positive dV/dt of the drain generates a current flowing through C_{GD} that opposes the current from the gate-driver circuit, known generally as Miller-effect current. The duration of this current flow is the V_{DS} rise time. Also note that the internal FET-gate terminal is at a higher voltage than observed on the gate terminal due to the Miller current flowing through the internal FET resistance, R_G.
3. After the V_{DS} rise time, the gate is discharged from the plateau voltage to the driver ground reference.

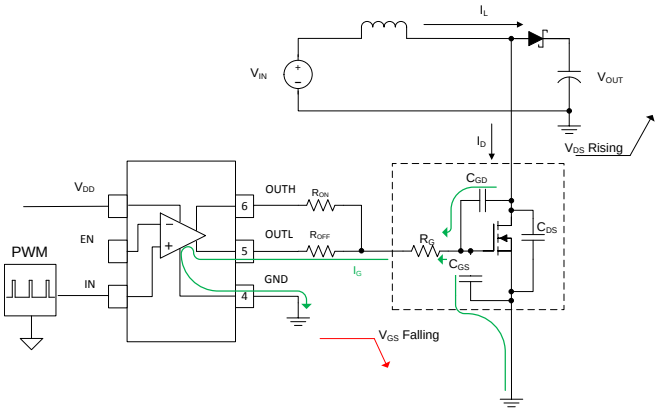

Figure 3. Turnoff Circuit with Parasitic Capacitance

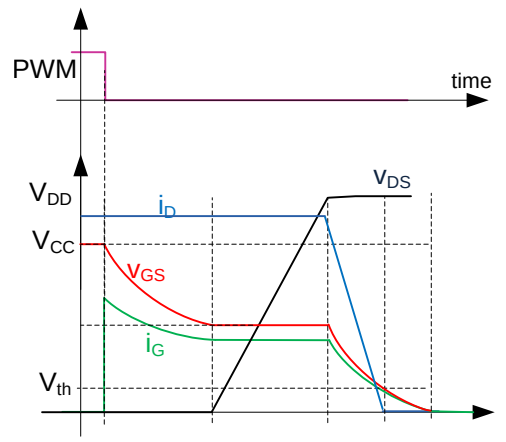

Figure 4. Turnoff Waveform

4 UCC27531 Advantages for SiC MOSFET Applications

The driver circuit voltage required for driving SiC MOSFETs within the recommended conditions includes the sum of the positive gate-drive level and negative-drive level. Some SiC MOSFETs recommend a positive voltage level close to 20 V and a negative drive of –5 V. The driver IC rating in this case requires 25 V minimum, plus margin for tolerance of the bias voltage and possible disturbance from line transients. The UCC27531 V_{DD} rating of 35 V allows the user to optimize the SiC MOSFET drive levels and have considerable UCC27531 V_{DD} rating margin. Many MOSFET drivers are rated at 20 V or 25 V resulting in lower than optimum drive levels, operating very close to the driver IC V_{DD} rating or a combination of both.

Similar to driving Si MOSFETs, the optimized turnon gate-drive resistance is usually higher than the turnoff gate-drive resistance in a well-tuned SiC driver circuit. The process of optimizing the gate drive for low switching losses and minimizing ringing of the V_{DS} waveform, typically results in some gate resistance for turnon and a lower or no resistance for gate-drive turnoff. The UCC27531 features separate high-side and low-side driver pins to program the optimum turnon and turnoff gate resistance. The separate pins eliminate the need for the parallel resistor and diode combination normally used with most single-pin output drivers. Eliminating the gate-drive diode drop is also advantageous to clamp V_{GS} low during the high dV/dt V_{DS} transition at turnoff.

Adequate available gate-drive current for SiC MOSFETs is important for a couple of reasons. The low threshold and relatively low transconductance results in a larger voltage swing on the gate when the MOSFET is in the variable resistance region. A fast transition through the variable resistance region results in achieving the lowest V_{DS} saturation in less time. The other consideration for driver sink current is the capability to clamp the V_{GS} low during the very fast V_{DS} rise times that SiC MOSFETs can achieve.

5 UCC27531 SiC Demonstration Circuit

A common circuit knows as the double pulse tester is utilized in testing power devices is used to demonstrate the switching waveforms. Refer to Figure 5 for the circuit schematic. A boost configuration is used as the power train for the SiC switching test. The power device can be switched at the desired V_{DS} and I_D peak current by adjusting the on time and frequency of the driver input. Since the output is connected to the input, the boost voltage is the VF of the boost diode; hence the off time must be long to allow the inductor current to decline to the desired turnon current. In order to keep layout parasitic inductance as low as possible, a low inductance 50-mΩ current shunt is used to measure the current on the SiC MOSFET source. All probe connections are Kelvin-referenced to the MOSFET device pins, and current shunt.

The details of turnon and turnoff are examined with the SiC MOSFET in hard-switching operation at high drain-to-source voltage and high drain-current condition.

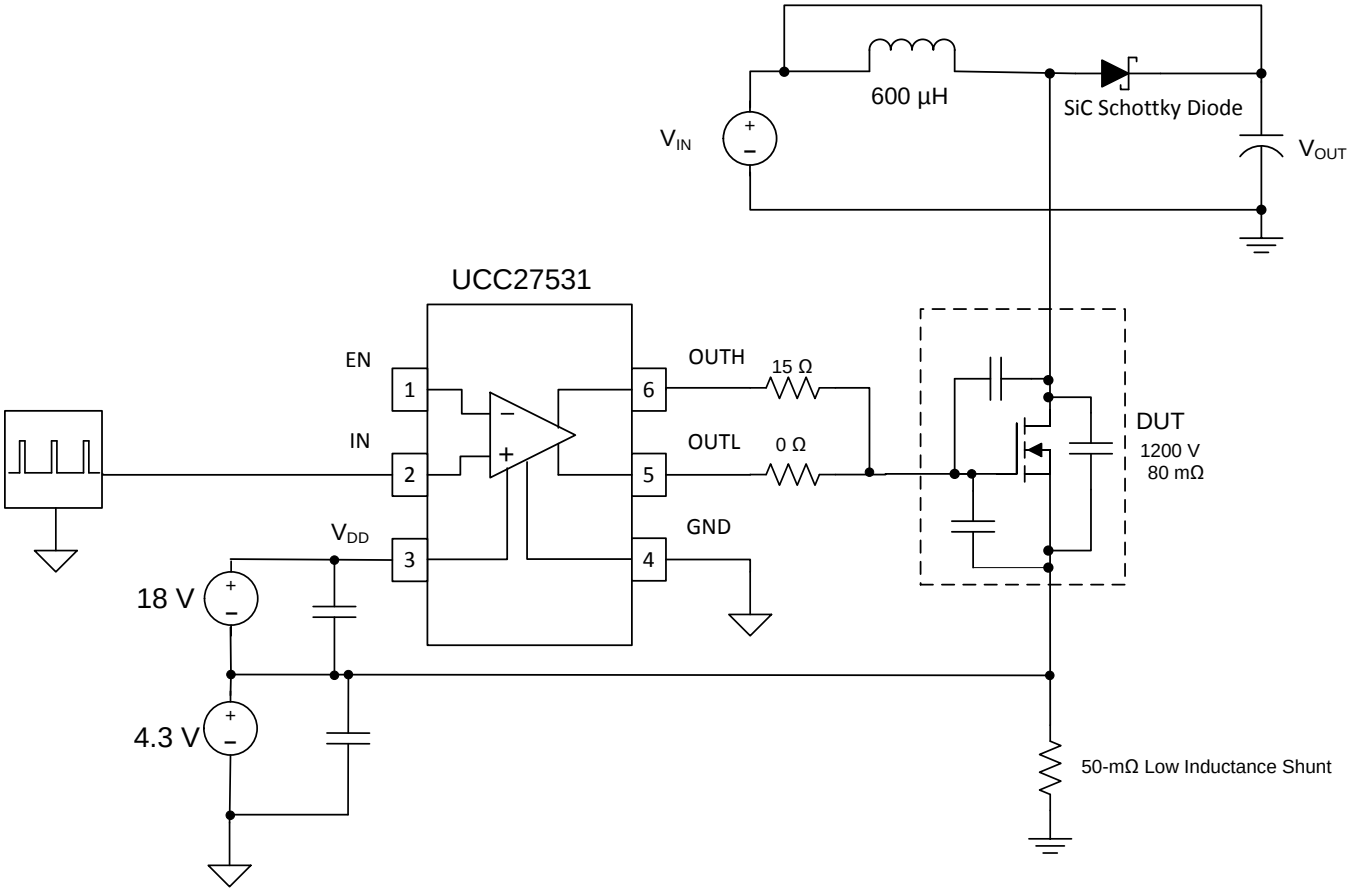

Figure 5. UCC27531 SiC MOSFET Demonstration Circuit Diagram

6 Test Data

6.1 Test Data With Sufficient SiC MOSFET Drive

The full cycle turnon and turnoff of the SiC MOSFET and the details of the turnon and turnoff are presented in the following oscilloscope waveform graphs.

The waveform in Figure 6 illustrates the V_{DS} high dV/dt during the turnon and turnoff transitions. The waveform clearly shows that the UCC27531 driver maintains the V_{GS} voltage during the Miller plateau during turnon without any significant negative voltage being induced.

During turnoff, the V_{GS} is falling and held low by the UCC27531 driver during the entire V_{DS} rising edge.

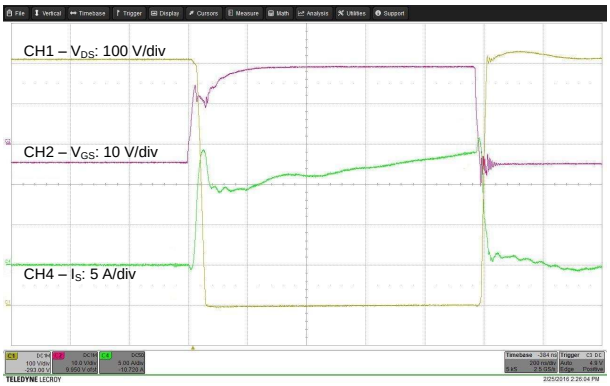

Figure 6. V_{DS}, V_{GS}, I_S Switching Cycle

The expanded scale zoom in Figure 7 of the turnon transition shows the V_{DS} falling within 30 ns and the Miller plateau occurring at approximately 12-V V_{GS}. The gate voltage initial rise to V_{DS} falling is approximately 30 ns and the gate voltage is maintained without significant dip during the V_{DS} rise time. This is with 15-Ω resistance for the driver OUTH source current.

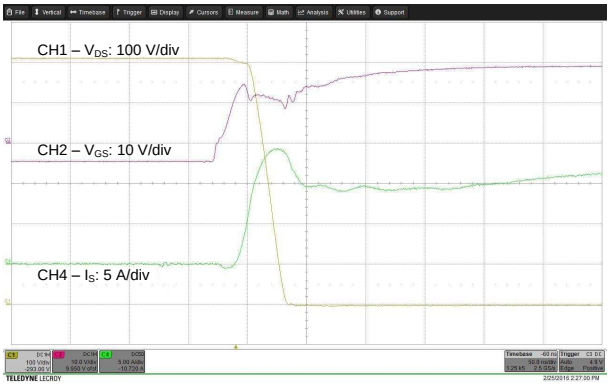

Figure 7. V_{DS}, V_{GS}, I_S Turnon Transition

The expanded scale zoom in Figure 8 of the turnoff transition shows the V_{DS} rising within 21 ns and the Miller plateau occurring at approximately 12-V V_{GS}. The gate voltage initial fall to V_{DS} rising is < 20 ns and the gate voltage is falling during the entire V_{DS} rising time. If the driver does not have adequate sink current, the fast dV/dt on V_{DS} can cause the V_{GS} to rise during the turnoff event, extending the turnoff switching time and increasing switching loss. The V_{GS} ringing peaks are below ground due to the negative drive bias.

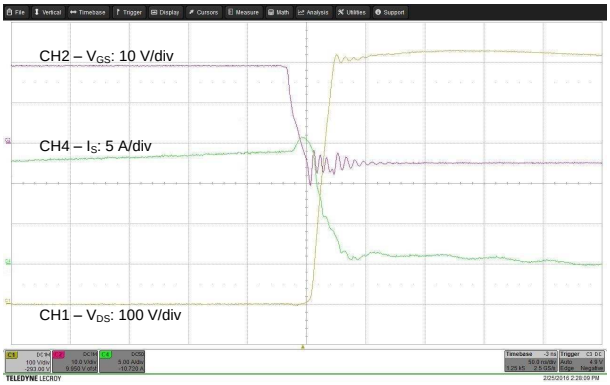

Figure 8. V_{DS}, V_{GS}, I_D Turnoff Transition

6.2 Test Data With Inadequate SiC MOSFET Drive

If the SiC MOSFET driver is not rated for adequate V_{DD} voltage to provide the suggested operating conditions for V_{GS} high plus the recommended negative drive voltage, the driver will not be able to fully enhance the MOSFET to the lowest $R_{DS(on)}$, or the V_{GS} may not be held to voltages comfortably below the threshold during switching. Also, if the driver does not have adequate current drive capability, the V_{GS} may not be maintained at the plateau during turnon or below the threshold during turnoff.

Figure 9 and Figure 10 show example waveforms that occur if the gate drive does not have adequate parameters to support well-tuned switching of SiC MOSFETs.

Figure 9 illustrates the lack of negative drive on the SiC MOSFET.

Without the negative drive bias, the V_{GS} does not have the margin to comfortably avoid the gate threshold voltage that can be as low as 1.6 V to 2 V during the turnoff transition.

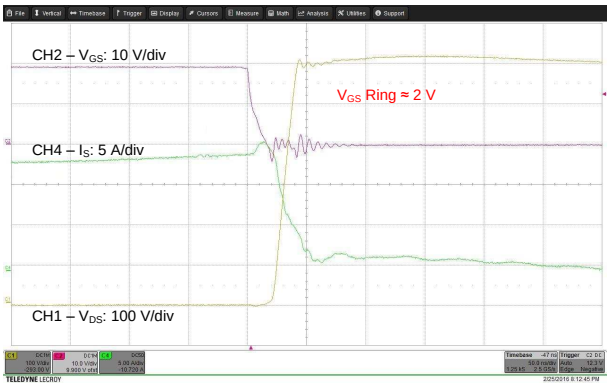

Figure 9. V_{DS}, V_{GS}, I_S Turnoff, No Negative Drive

Figure 10 illustrates if the gate drive has inadequate sink current. The lower sink current was duplicated by inserting a 10-Ω series resistance into the OUTL driver path.

Without high sink current capability from the driver, the driver cannot prevent the V_{GS} from rising due to the Miller charge coupled into the gate during the V_{DS} rising. The V_{GS} can rise close to the threshold voltage and inhibit or delay the turnoff transition.

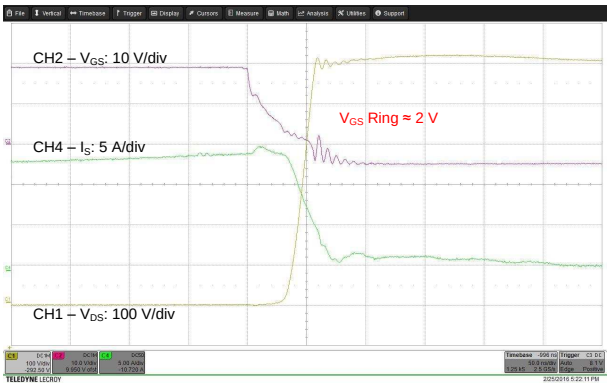

Figure 10. V_{DS}, V_{GS}, I_S, Reduce Driver Sink Current

7 Increasing the UCC27531 V_{DD} Turnon

Most high power systems' sequencing usually allows time or monitoring for the bias supply voltages to reach the normal operating point before the power train switching is enabled. If the power up sequencing is not controlled, or if there are concerns about fault conditions of the controller and driver bias, the UVLO of the UCC27531 can be increased from the device's internal threshold of 8.9 V.

A simple voltage supervisor as shown in Figure 11 increases the V_{DD} turnon of the UCC27531 to the desired threshold. The TPS3711 has a V_{DD} rating of up to 36 V, so the V_{DD} operating range of the UC27531 is not compromised.

The UCC27531 enable pin has an internal pullup resistance connected to a 5.6-V bias, which is compatible with the open-drain configuration of the TPS3711. The open-drain configuration of the TPS3711, and internal pullup of the UCC27531 allows the user to program the desired V_{DD} turnon and hysteresis, if desired, by connecting a resistance from the TPS3711 OUT to SENSE pins.

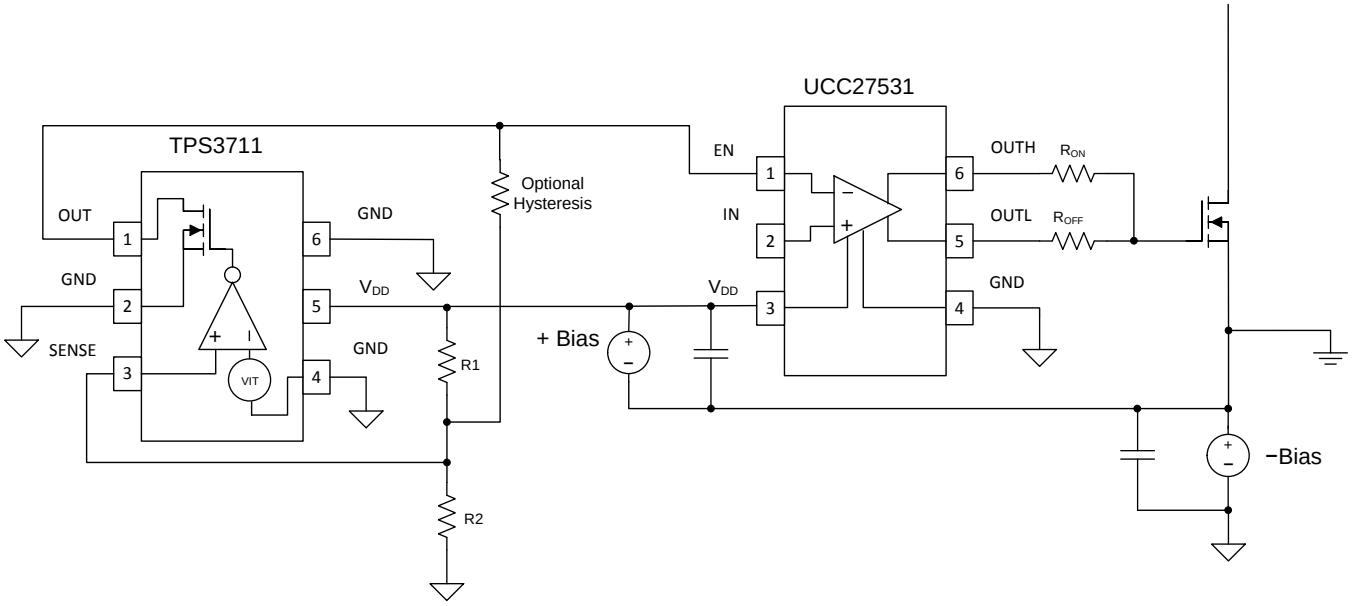

Figure 11. TPS3711 to Program UCC27531 UVLO Thresholds

Determine TPS3711 resistor values based on Equation 1.

$$R1 = \frac{(V_{VDD\_ON} - V_{IT+}) \times R2}{V_{IT+}} \quad (1)$$

where

- R2 recommended range is 20 kΩ to 50 kΩ.
- V_{VDD_ON} is target V_{DD} UVLO turn on threshold
- V_{IT+} is the TPS3711 SENSE pin positive input threshold, 405.5 mV nominal.

There is hysteresis on the TPS3711 SENSE pin with a falling threshold of 400 mV nominal (V_{IT-}). The UVLO turn off is determined using Equation 2:

$$V_{VDD\_OFF} = \frac{V_{IT-} \times V_{VDD\_ON}}{V_{IT+}} \quad (2)$$

where

- V_{DD_ON} = 12 V
- V_{DD_OFF} = 11.83 V

The hysteresis can be increased as shown in Figure 11 with an additional resistor.

8 Layout Recommendations

The switching speed of SiC MOSFETs makes it critical to provide close placement and good layout of the gate-driver circuit. The driver IC performance will be compromised if the gate-drive layout loop parasitic inductance is not kept to a minimum. Compact layout becomes simple due to the UCC27531's small package size and separate IC pins for the high- and low-side drive. A driver layout illustrating close placement and short connections is shown in Figure 12.

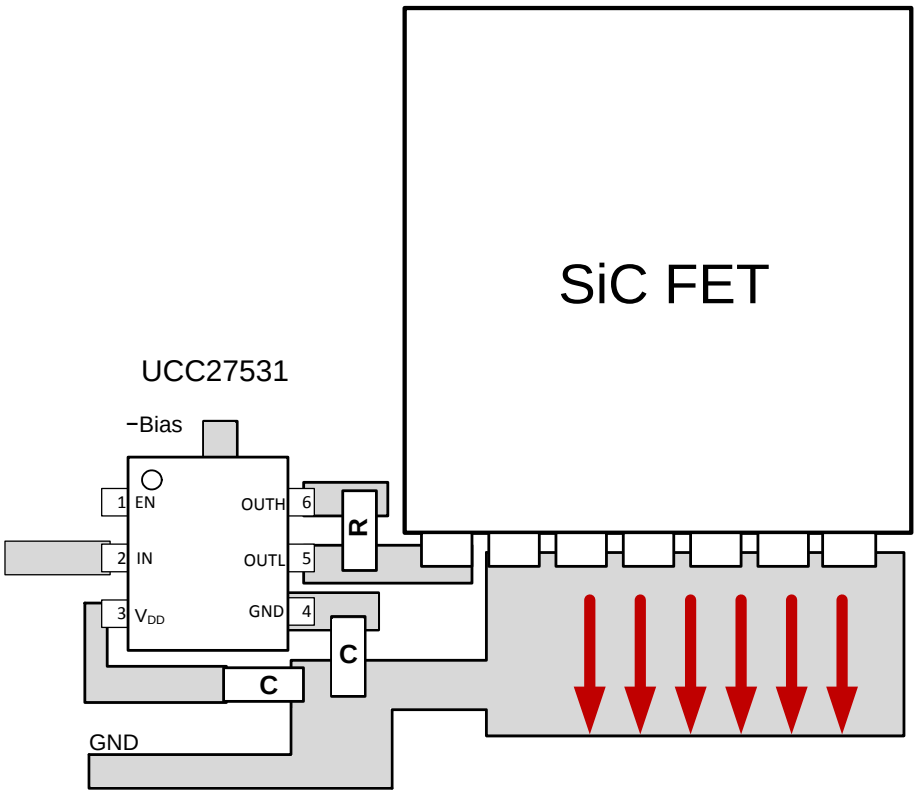

Figure 12. Driver and MOSFET Layout

9 Conclusion

Silicon Carbide MOSFETs are capable of very good switching performance in high-voltage, high-power applications. In order to maximize the capabilities of the SiC power MOSFETs, a high performance gate-drive circuit and good driver layout is required. The negative drive bias requirement and higher optimum positive V_{GS} require a drive circuit with higher V_{DD} ratings than typical Si MOSFET drivers. The UCC27531 35-V rating allows the designer to optimize the drive levels and have considerable driver circuit margin.

The fast switching of SiC devices will challenge many typical driver circuits during the switching transitions. The Miller charge can inhibit or even cause false triggering during the switching events if the driver is not low enough resistance, or high enough current capability. Also, since the SiC MOSFETs have a larger V_{GS} delta in the variable-resistance region, it is important to slew the V_{GS} as fast as possible. The UCC27531 split pins for the high- and low-side drive circuits provides an advantage to maintaining the V_{GS} during the Miller plateau. Additionally, the drive current capability of the UCC27531 enables fast turnon and turnoff of SiC MOSFETs. The UCC27532 is a driver in the same family as the UCC27531 and has CMOS compatible input thresholds if increased input threshold hysteresis is desired.

10 References

1. Infineon “IPW90R120C3 CoolMOS Power Transistor Datasheet,” Rev 1.0, July 30, 2008
2. Cree “C3M01120090D Silicon Carbide Power MOSFET Datasheet,” November, 2015
3. Jimmy Liu, Kin Lap Wong, Scott Allen, John Mookken, “Performance Evaluations of Hard-Switching Interleaved DC/DC Boost Converter with New Generation Silicon Carbide MOSFETs”
4. Cree “Application Considerations for Silicon Carbide MOSFETs”, (Online) under “Power Application Notes”

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (#IMPLIED) to A Revision	Page
• Changed Figure 4.	3

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