Application Report
SLUA783–October 2016

Troubleshooting TI PSR Controllers

Kening Gao

ABSTRACT

Power supply designers must often troubleshoot problems. The problems may include smoke upon first supplying power or the device displays no light or noise and does not start up at all. The fundamentals of debugging should be to make sure the components are assembled correctly according to the schematic with no incorrect PCB connections[1]. This document focuses on the design issues and assumes the board has been checked and that failed components have been repaired. This application note can be used for TI's primary-side regulated (PSR) controllers and switchers, such as the UCC2870X, UCC2871X, UCC2872X, UCC28730, and UCC2891X.

Contents

List of Figures

1 Background

Table 1 is a comparison table for TI's PSR controllers and switchers. Minor differences are noted even though the control laws and working principles may be similar.

Table 1. Comparison Table for TI PSR Parts

TI PSR Part	HV Start	Output Drive for
UCC2870X	No	MOSFET
UCC2871X	Yes	MOSFET
UCC28720	Yes	BJT
UCC28722	No	BJT
UCC28730	Yes	MOSFET
UCC2891X	Yes	Integrated MOSFET

Figure 1 is a simplified basic reference circuit used for description purposes in this application note. Note the part used in Figure 1 is the UCC28700. If using other parts, there are minor differences in the circuit that will not affect troubleshooting. Also note that primary and secondary snubbers are not shown.

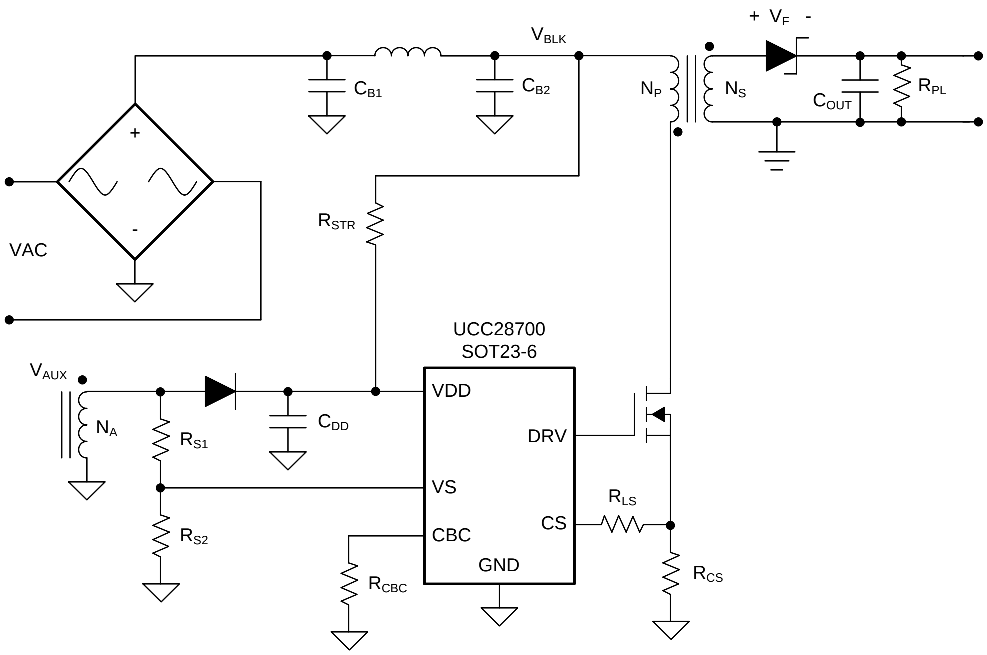


Figure 1. Simplified Typical TI PSR Flyback Application

2 Issue 1: Power Converter Cannot Startup or Shuts Down Unexpectedly

2.1 Cause 1: V_{DD} UVLO

Phenomenon: Before V_{DD} goes down to $V_{VDD(off)}$, there are switching pulses with which the frequency is higher than minimum frequency, $F_{sw(min)}$, as shown in Figure 2.

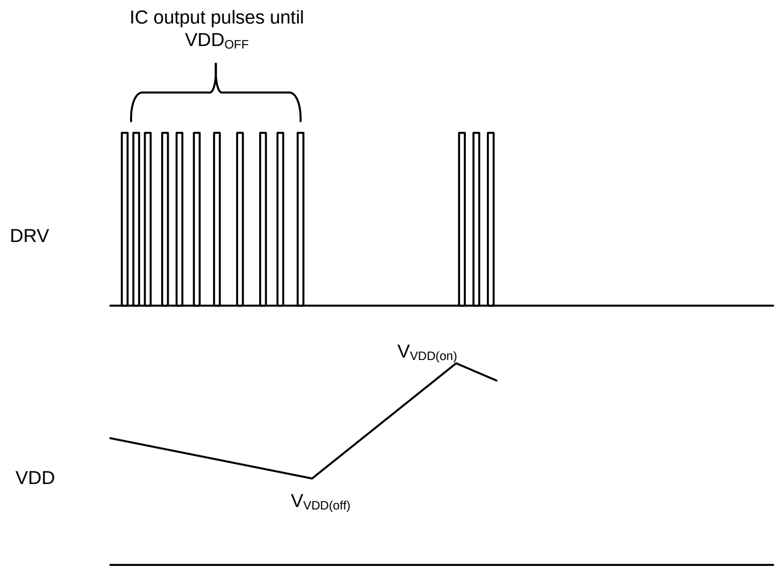


Figure 2. V_{DD} UVLO Protection

Potential Solutions:

- Increasing the auxiliary winding turns will elevate the V_{DD} level.
- Increase V_{DD} capacitance. This helps the V_{DD} sustain time also helping with startup.
- Decrease output capacitance and increase the constant current point. See the “primary side regulation” on the datasheet for the constant current. A simple way to increase the constant current point is to decrease the R_{CS} resistor. These methods increase the rising time of Vout to help startup.
- Decrease the resistor in-series with an auxiliary diode, if any. It will elevate the V_{DD} level by collecting more leakage energy of the transformer with some load.
- “Full Load, CC Mode, load-on point = 0 V” is the serious configuration of E-load for startup. Sometimes changes on the E-load configuration, such as setting half load or CR Mode or setting load-on point at higher value, are acceptable within the system requirements.

2.2 Cause 2: V_{DD} Clamp Current Exceeding Rating (Only for UCC2891X)

Phenomenon: V_{DD} reaches VDD_{CLP} (minimum 26 V), and the clamp flowing current exceeds 6 mA[2].

Potential Solutions: Make sure V_{DD} stays lower than VDD_{CLP} at all conditions by setting the Na/Ns properly and adjusting the resistor in-series with V_{DD} diode.

2.3 Cause 3: V_{IN} UVLO

TI PSR parts have AC-line input undervoltage protection functions by detecting current information at the VS pin during the MOSFET on-time. While the VS pin is clamped close to GND during the MOSFET on-time, the current through RS1 is monitored to determine a sample of the bulk capacitor voltage[4]. To make sure the converter works properly, the VS dividers should be designed carefully according to the datasheet.

However, if you believe the calculation is right, but there is a shutdown or startup issue, capture the last three cycles of V_{BLK}, V_{AUX}, and V_{DRV} as is suggested in Figure 3. Determine the root cause by checking the following:

1. Is the voltage of V_{BLK} too low? — A bulk capacitor value that is too small would make the ripple on V_{BLK} too much, especially at low-line input and full load. A rough suggestion for bulk capacitor selection is about 2 µF / W. For a 10-W design, 22-µF capacitance (22 µF is standard value) is suggested.
2. Is the V_{AUX} waveform flat and the V_{AUX} approach to V_{BLK} × Na / Np during MOSFET on-time? — If not, there is something wrong; check the transformer turns ratio and the voltage on the primary windings during Q1 on-time. A common issue is *Improper BJT Selection*.
3. Is the current from the VS pin at startup (for the issues where there are only three cycles of pulses) V_{AUX} / RS1 larger than $I_{VSL(run)}$? — Make sure the current is larger than $I_{VSL(run)}$, or else go back check the related parameters.
4. Is the current from the VS pin at the last switching cycle (for the issues where there are many cycles) V_{AUX} / RS1 lower than $I_{VSL(stop)}$? — If yes, it will cause the converter to shut down.

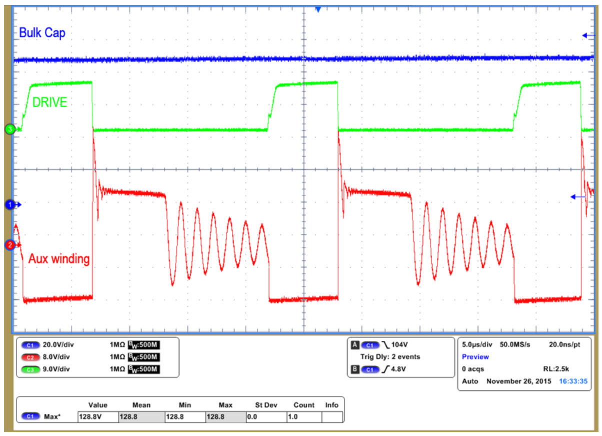


Figure 3. Waveforms Needed to Distinguish Input UVLO Issue

2.4 Improper BJT Selection

For UCC28722 and UCC28720 devices, improper selection for BJT could cause the input UVLO protection. The BJT may not be fully switched on due to the low current gain. V_{AUX} during MOSFET on-time is not flat and does not match V_{BLK} × Na / Np near the end of MOSFET on-time. Figure 4 shows a typical UVLO protection caused by improper BJT selection.

An important parameter for a BJT is h_{FE}, DC current gain. It varies with I_B, V_{CE} and temperature and can be quite low. For the UCC2872X application, base current I_B is decided by the controller's driving current I_{DRS} (19 mA to 37 mA).

So the h_{FE} current gain of BJT should be high enough to make the BJT operate with lower on-state V_{CE}.

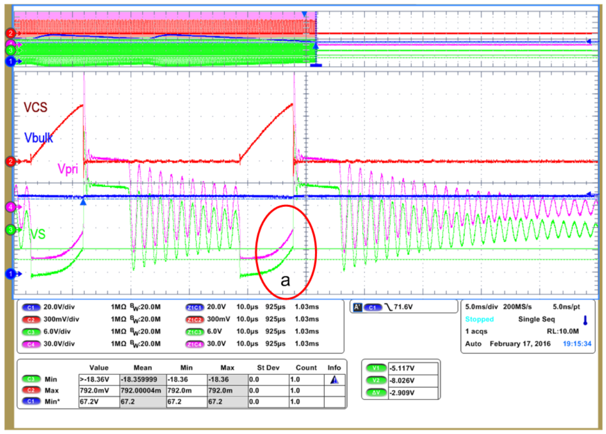


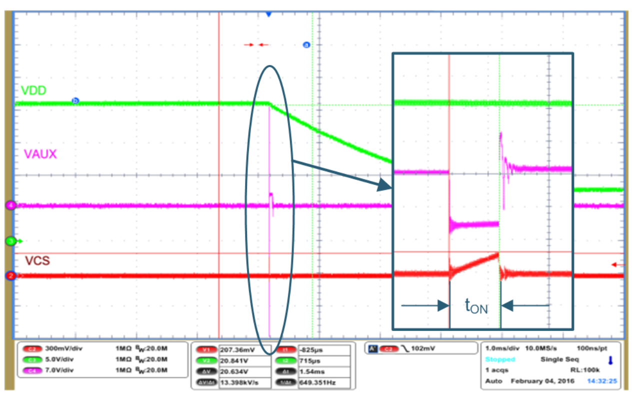
Figure 4. UVLO Protection Caused by Improper BJT Selection

2.5 Cause 4: On-time Detection

2.5.1 On-Time is Too Long at First Startup Cycle

Phenomenon: TI PSR controllers and switchers check the MOSFET on-time by detecting the voltage on the CS pin on the very first cycle after V_{DD} UVLO on. If the voltage on the CS pin does not reach $I_{PP(min)}$ in the desired time, the IC will confirm the fault and discharge V_{DD} to $V_{VDD(off)}$ where $I_{PP(min)} = V_{CST(min)} / R_{CS}$. For UCC28704 and UCC28730, this desired time is typical 4 µs. For UCC28700/1/2/3, UCC28710/1/2/3, UCC28720/2, UCC28740 the desired time for t_{ON} fault is 1 / $F_{SW(max)}$. As for the first cycle, $t_{ON} = (L_{PRI} \times I_{PRI}) / V_{BLK}$, too high inductance or very low input voltage can cause this startup issue. Figure 5 shows the t_{ON} fault of the UCC28704 circuit.

Potential Solutions: To verify the issue, increasing input voltage, decreasing L_{PRI} or increasing R_{CS} can be used. However, the circuit designer should check the power system design completely to find out why the t_{ON} time is so large.



Right side of image is zoomed in, t_{ON} is larger than 4 µs.

Figure 5. Startup Issue Caused by Long t_{ON} on a UCC28704 Board

2.5.2 Too Long On-Time Causes Shutdown

Phenomenon: This is only suited for the UCC2891X. The IC will stop DRV output and start the V_{DD} UVLO cycle when it detects three consecutive on-times larger than $t_{ONMAX(max)}$ at high load and $t_{ONMAX(min)}$ at light load.

Potential Solutions: To verify the issue, decrease L_{PRI} or increase R_{IPK}. However, the circuit designer should check the power system design completely to find out why the t_{ON} time is so large.

2.6 Cause 5: CS Short Circuit (1.5-V) Protection

The converter will stop the switching cycle and start a V_{DD} reset cycle when the IC detects a voltage on the CS pin higher than 1.5 V for three consecutive cycles.

2.6.1 CS Noise Caused by Layout

Phenomenon: The typical noise caused by the suddenly raised dv/dt of the Vds of primary MOSFET / BJT is illustrated in Figure 5. The voltage peak on the CS pin after MOSFET / BJT turn off exceeded the overcurrent threshold V_{OCP}, for UCC28710 its typical value is 1.5 V. The noise can be serious if there is poor layout and the R_{LC} is too high.

Potential Solutions: Improve the CS circuit layout and MOSFET to decrease the noise.

The situation improves with a smaller R_{LC}. However, changeing the R_{LC} resistor will also impact the constant current regulation. Make sure R_{LC} is close to the controller package.

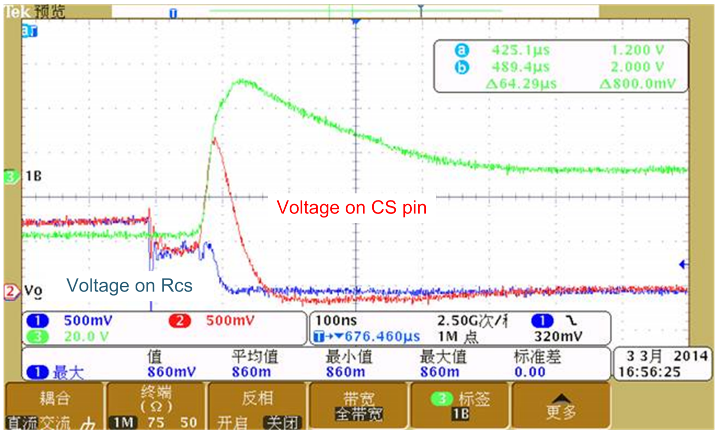


Figure 6. OCP Caused by the Noise

2.6.2 Transformer Saturation

Phenomenon: The typical saturation for a transformer is illustrated in Figure 6. The current through R_{CS} increases rapidly when the transformer becomes saturated.

Potential Solutions: Check the transformer design to make sure no saturation occurs. The equation to check B_{MAX} is:

$$B_{MAX} = \frac{L_{PRI} \times I_{PRI}}{N_P \times Ae}$$

where

- $I_{PRI} = \frac{V_{CST(max)}}{R_{CS}}$ for UCC2870X,UCC2871X and UCC2872X
- $I_{PK} = \frac{V_{CCR}}{R_{IPK}}$ for UCC2891X
- N_p is the primary winding turns of the transformer
- L_{PRI} is the primary inductance
- Ae is the cross-sectional area of the core (1)

B_{MAX} should always be lower than B_{SAT} which is the core saturation flux density and decided by the core material. The curve or value of B_{SAT} is found in the ferrite core book as shown in Figure 7. The temperature characteristic of B_{SAT} should be considered.

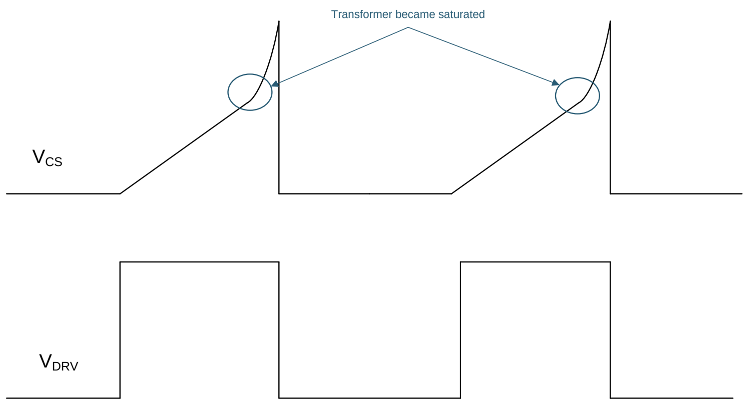


Figure 7. OCP Protection Caused by Transformer Saturation

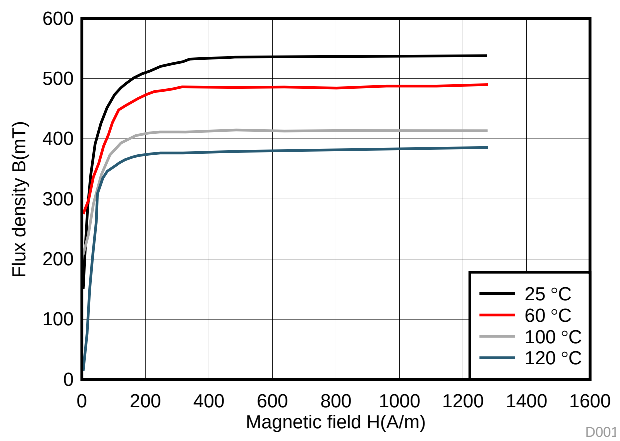


Figure 8. B-H Temperature Characteristics of the TDK PC95

2.7 Cause 6: AUX Winding Detection (OVP)

The output overvoltage function is determined by the voltage feedback on the VS pin. The device stops switching and starts to discharge the V_{DD} capacitor to the $V_{VDD(off)}$ threshold when it detects an overvoltage.

2.7.1 Output Voltage Trigger OVP at Zero Load

Phenomenon: When probing on the output voltage, the output voltage exceeds the regulation level and the voltage reflected to the VS pin exceeds the overvoltage threshold V_{OVP}.

Potential Solutions: Decrease the capacitance of the drain node, which mainly includes the C_{OSS} of the MOSFET and input capacitance of the transformer;

- To decrease the preload resistor value
- To check if the turn-off of the MOSFET is too slow which may cause too large of a series resistor in the gate

2.7.2 The Shape on the VS Pin Affects the Detection

The PSR controller does not sense the output directly like a traditional optocoupler feedback. It is more sensitive by its working scheme of detecting the auxiliary winding voltage. The shape of the voltage on the VS pin is very important to avoid mis-detection and OVP. Because probing on the VS pin could also affect the detection, estimate the waveform of the VS pin by probing the auxiliary winding.

See the respective datasheet for the needed shapes.

However, snubber adjusting especially on the damping resistor can affect the waveforms. A leakage inductance of the transformer that is too high would make the detection less accurate. The layout of the VS relative circuit should also be done correctly. The trace between the VS dividers and the VS pin should be as short as possible to reduce EMI coupling[4].

3 Issue 2: Output Voltage Ripple and Noise is Quite High at Certain Load

First of all, check if the converter is in V_{DD} UVLO reset and restart sequence. If the V_{DD} crosses between $V_{VDD(on)}$ and $V_{VDD(off)}$, which will cause ripple issues, the protection is triggered. From issue 1, you could get clues to find out and solve the root cause. If the V_{DD} does not hiccup between $V_{VDD(on)}$ and $V_{VDD(off)}$ thresholds, then proceed to debug with one of the following tips:

3.1 Is That a Line Frequency Ripple?

Figure 9 is a typical waveform of high ripple with line frequency. When V_{BLK} is at a lower point, the converter cannot provide enough power to the output, so the “Dip” ripple may be seen. To solve this problem, increasing the bulk cap or decreasing the Np/Ns ratio can be used. However, as changing the Np/Ns also affects other performance, checking the calculation according to the datasheet is the root way to solve this issue.

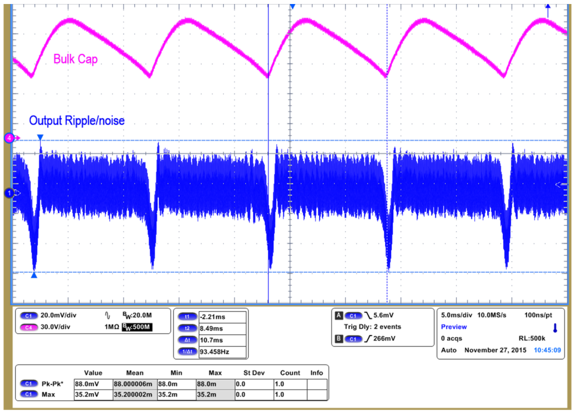


Figure 9. Line Frequency Ripple in Output Voltage

3.2 Is that a low frequency oscillation (loop unstable for TI PSR)?

The closed-loop of PSR is not as apparent as it is of opto-feedback. So if there is unexpected ripple with several kHz frequency (not the line frequency) as shown in Figure 10, investigate the following points:

- Check if there is a missing *valley switching*, as mentioned in Issue 5: Missing Valley Switching. The abnormal *valley switching* could cause some oscillation on the ripple.
- The loop instability could cause high ripple. As it is difficult to measure the closed loop response in PSR parts, the way to mitigate it is to increase the output capacitor and increase the working frequency at full load.
- Noise on the VS and CS pin can also have an effect on the instability.

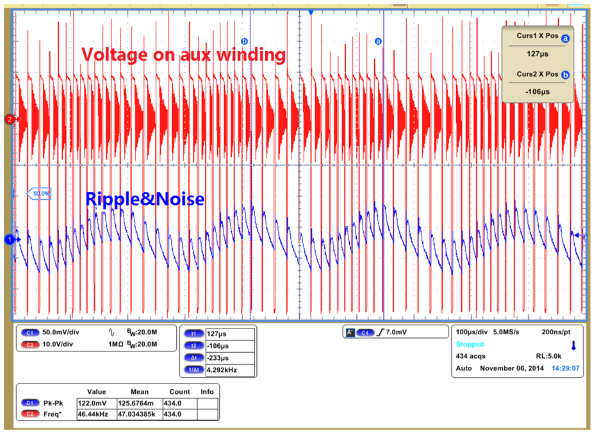


Figure 10. Higher Output Ripple With Approximate kHz Oscillation

4 Issue 3: Transient Response Worse

4.1 PSR Limitation

The PSR has a limitation of the transient response, especially when the load is switched from light load to half load or full load. This is because the switching frequency is very low at light load.

For special cases which need better transient response when the load switches from zero load to a certain load, increasing the working frequency of zero load and increasing the output capacitor can work. But, increasing the working frequency of a zero load also means a higher preload requirement which deteriorates standby power.

Another choice is using the UCC28730+UCC24650 chipset solution, which brings both very low standby power and a good transient response performance.

5 Issue 4: Constant Current Mode

5.1 CC Value Varies With High or Low Line Input

Phenomenon: The CC greatly varies with different line input voltage.

Potential Solutions: Adjusting the R_{LC} resistor should mitigate the difference. See the respective datasheet for the function of the R_{LC} resistor.

6 Issue 5: Missing Valley Switching

The PSR controllers and switchers from TI operate in discontinuous conduction mode with valley-switching to minimize switching losses. However, improper design could make the valley switching disappear, which could cause increased switching loss and higher ripple or higher noise.

6.1 Cause 1 - LC Resonant Period Too Long

Phenomenon: The LC resonant tank exceeded the t_{ZTO}. t_{ZTO} is defined as zero crossing timeout delay and is specified in datasheet. For UCC2870X, UCC2871X and UCC2891X, the minimum value of t_{ZTO} is 1.8 µs, for the UCC28730 it is 1.6 µs. As the resonant frequency is decided by the primary inductance of the transformer and equivalent capacitor on the drain node $C_{SW} = C_{OSS} + C_W$ (where C_{OSS} is the output capacitance of primary MOSFET and Cw is the transformer capacitance), the resonant $\text{period} = 2\pi\sqrt{L_{PRI} \times Csw}$.

Potential Solutions: Decrease the primary inductance I_{PRI} or capacitance on the drain node to solve this issue.

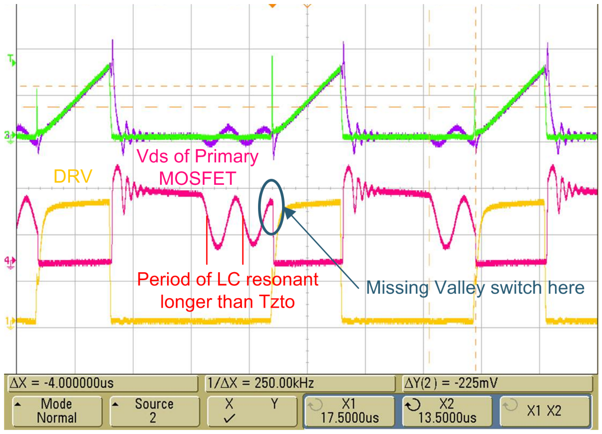


Figure 11. Long LC Resonant Period Causes Missing Valley Switching

6.2 Cause 2 - Very Quick Resonant Decay With TVS Snubber

Phenomenon: When very low standby power is required and switching frequency is very low, a TVS snubber must be used. With a TVS snubber, improper selection of slow clamp diode will cause a very quick decaying as shown in Figure 12. For a detailed explanation of this issue, see *Choosing Standard Recovery Diode or Ultra-Fast Diode in Snubber* (SNVA744).

Potential Solutions: An R2CD snubber is suggested to replace the TVS snubber for those which do not need very low standby power applications; If a TVS snubber is a must, using ultra-fast diode in a snubber circuit or paralleling small capacitor on TVS.

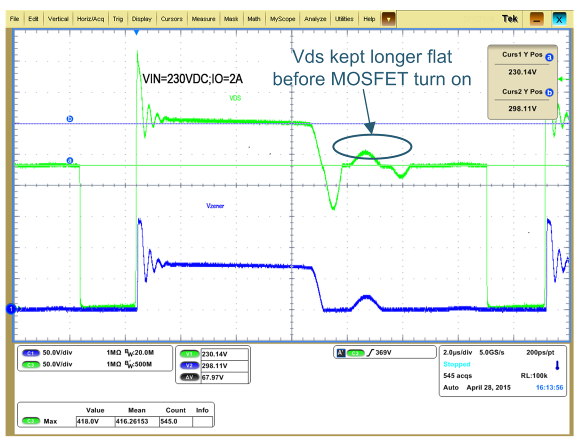


Figure 12. Very Quick Resonant Decay Caused by Improper Snubber Design

7 Issue 6: Audible Noise

The audible noise of flyback is usually caused by ceramic capacitors or the ferrite transformer because of mechanical vibration.

If replacing the ceramic capacitors, which have high dv/dt swings (such as snubber cap), with a metal-film capacitor and dip-varnishing the transformer does not work, an improper design must be considered as the problem. Engineers should check the output stability (*Issue 2: Output Voltage Ripple and Noise is Quite High at Certain Load*) .

Another way to mitigate the audible noise is to make the converter work in the highest frequency allowed by the part's datasheet.

8 Device Nomenclature

Device Terms

$V_{VDD(off)}$	UVLO turn-off voltage (see the electrical characteristics table of the respective datasheet)
$V_{VDD(on)}$	UVLO turn-on voltage (see the electrical characteristics table of the respective datasheet)
VDD_{CLP}	V_{DD} voltage clamp (see the electrical characteristics table of the UCC28910, UCC28911 datasheet (SLUS769))
$V_{CST(min)}$	CS pin minimum current-sense threshold (see the electrical characteristics table of the respective datasheet)
$V_{CST(max)}$	CS pin maximum current-sense threshold (see the electrical characteristics table of the respective datasheet)
V_{OCP}	Overcurrent threshold (see the electrical characteristics table of the respective datasheet)
V_{CCR}	Constant-current regulating voltage (see the electrical characteristics table of the respective datasheet)
V_{OVP}	Overvoltage threshold (see the electrical characteristics table of the respective datasheet)
$F_{SW(min)}$	Minimum switching frequency (see the electrical characteristics table of the respective datasheet)
$F_{SW(max)}$	Maximum switching frequency (see the electrical characteristics table of the respective datasheet)
$I_{VSL(run)}$	VS line-sense run current (see the electrical characteristics table of the respective datasheet)
$I_{VSL(stop)}$	VS line-sense stop current (see the electrical characteristics table of the respective datasheet)
I_{DRS}	DRV source current (see the electrical characteristics table of the respective datasheet)
$t_{ONMAX(max)}$	Maximum FET on time at high load (see the electrical characteristics table of the UCC28910, UCC28911 datasheet (SLUS769))
$t_{ONMAX(min)}$	Maximum FET on time at low load (see the electrical characteristics table of the UCC28910, UCC28911 datasheet (SLUS769))
t_{ZTO}	Zero-crossing timeout delay (see the electrical characteristics table of the UCC28910, UCC28911 datasheet (SLUS769))

BJT Terms

V_{CE}	Collector-emitter voltage
h_{FE}	DC current gain
I_B	Base current

Transformer Terms

Na/Ns	Auxiliary-to-secondary turns ratio
Na/Np	Auxiliary-to-primary turns ratio
Np/Ns	Primary-to-secondary turns ratio
L_{PRI}	Primary inductance
B_{SAT}	Saturation flux density

Other Terms

R_{IPK}	UCC28910, UCC28911 primary current programming resistance
R_{LC}	Line compensation resistor
R_{S1}	High-side VS pin resistance
R_{CS}	Primary current programming resistance
C_{OSS}	Output capacitance of MOSFET
Cw	Total capacitance on the switching node
T_{ON}	On-time of MOSFET / BJT
I_{PRI}	Peak primary current

9 Other Support Resources

More help is available from TI's E2D forum:
https://e2e.ti.com/support/power_management/isolated_controllers/

10 References

1. Robert Taylor, Ryan Mannack, *Debugging power-supply startup issues*, Analog Applications Journal, 3Q-2015
2. UCC28910, UCC28911 datasheet (SLUS769)
3. Kening Gao, Ulrich B. Goerke, *Choosing Standard Recovery Diode or Ultra-Fast Diode in Snubber*, TI application note (SNVA744)
4. UCC2870x datasheet (SLUSB41)

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265