

Zero-Voltage-Switching Flyback Using UCC28780 Controller and UCC5304 Isolated Synchronous-Rectifier Driver



ABSTRACT

This application report describes how the UCC28780 Active-Clamp Flyback controller can be paired with the isolated driver UCC5304 to implement a Zero-Voltage-Switching Flyback (ZVSF) power supply, delivering high efficiency and high power-density at a competitive cost compared to the conventional Quasi-Resonant (QR) flyback topology.

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1 Introduction

Conventional fixed-frequency and quasi-resonant (QR) flybacks are limited in their power density and upper switching frequency capability due to the switching loss and the dissipation of the transformer leakage inductance energy. The active-clamp-flyback (ACF) overcomes these limitations by achieving zero-voltage-switching (ZVS) and recycling of the leakage energy to the output. However, these benefits do not come for free, the ACF requires some extra components to achieve the benefits – a second primary high-side switch, high-side driver/level-shifter, bigger clamp capacitors, and so forth.

An alternative ZVS flyback (ZVSF) topology is introduced in this application note. This ZVSF topology achieves ZVS only – that is, the leakage energy is not recovered. The power-loss saving realized by ZVS allows for increased switching frequency and therefore smaller transformer size and higher power-density compared to QR and fixed-frequency designs. This offers a simpler, lower component-count, moderate-performance alternative to the ACF, that sits somewhere in between QR and ACF in terms of both performance and component-count complexity.

The ZVSF topology is a good alternative to consider for medium-density high-volume applications, and this application note shows how the ACF controller UCC28780 can be combined with an isolated driver UCC5304 to implement ZVSF using secondary-side synchronous rectification (SR).

2 Topology Overview

Figure 2-1 shows the overall topology architecture along with some typical waveforms.

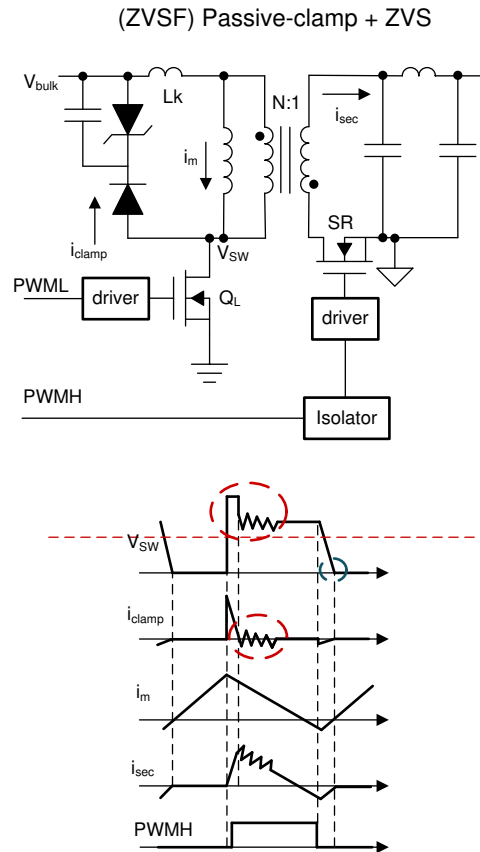


Figure 2-1. ZVSF Topology Block Diagram and Waveforms

In the same way as conventional QR or fixed-frequency flyback, the primary side uses a clamp snubber to limit the V_{ds} stress on the primary FET due to the leakage inductance, and much of the leakage inductance energy is dissipated in the clamp. The clamp can be a TVS type, as Figure 2-1 shows, or an RCD snubber.

The ZVSF controller operates in transition-mode (TM) at heavy load, where the primary FET and secondary synchronous rectifier (SR) are driven in complement to each other, with adaptive dead-time in between. The primary on-time is adjusted by the control loop to adjust the peak primary magnetizing current, in order to regulate the output voltage. The secondary SR on-time is extended beyond the normal zero-current point to allow some negative magnetizing current to build up in the transformer. The energy associated with the negative current discharges the total drain-node capacitance when the SR is turned off, and the next turn-on point for the primary FET occurs when the drain voltage has dropped close to zero, for ZVS turn-on.

3 Topology Differences vs. ACF and QR

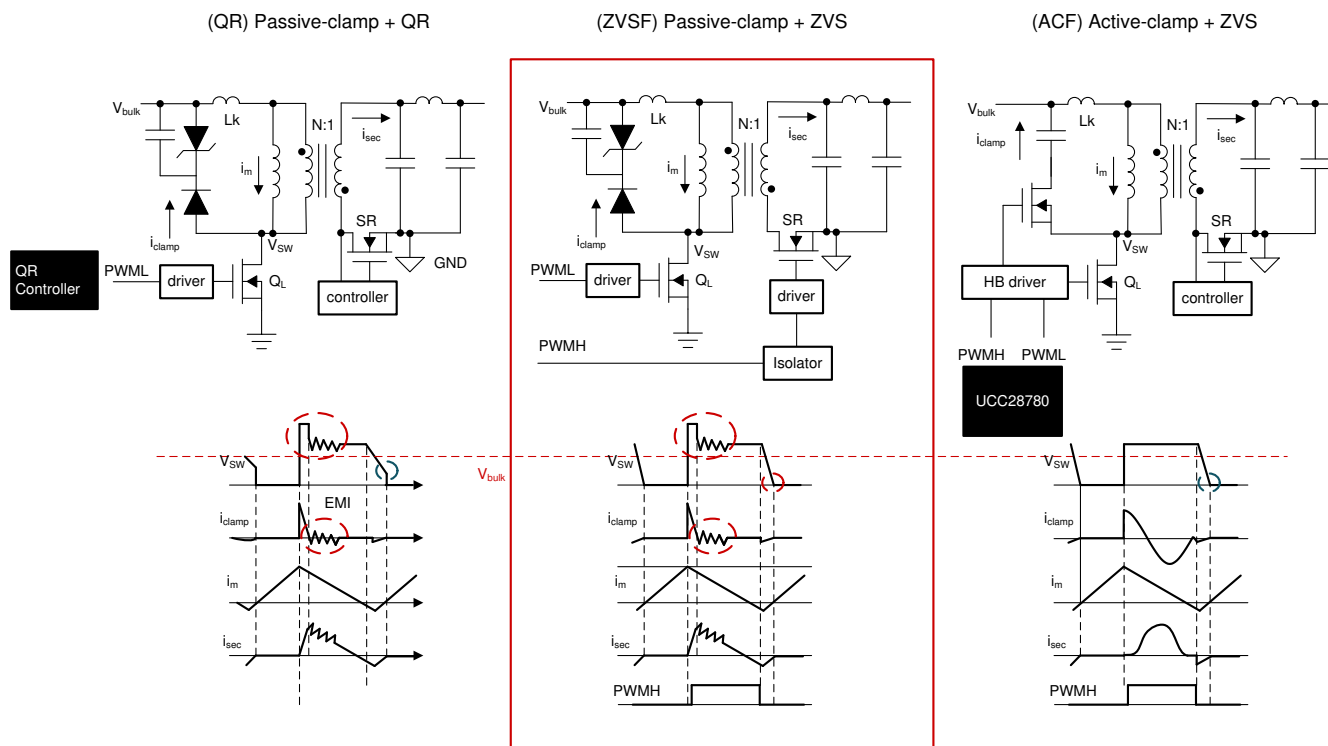


Figure 3-1. ZVSF Topology Block Diagram and Waveforms vs QR and ACF

Figure 3-1 shows that the ZVSF power circuit and waveforms are more similar to QR than to ACF. For both QR and ZVSF, the leakage inductance energy is not recycled, but is instead mostly dissipated in the primary clamp. At minimum input voltage and maximum rated-output voltage, a QR design would usually already operate close to ZVS due to the natural resonant ringing between the magnetizing inductance and the equivalent switch node capacitance – assuming that the transformer turns ratio is designed for a reflected voltage approximately equal to the minimum input voltage (typical QR design target).

However, at high-line input voltages, even when switching on the first valley of the resonant ring, the instantaneous voltage is non-zero and actually quite significant. As a result, QR design can only achieve ZVS at minimum input voltage (V_{IN}). For wide output-voltage range applications, such as USB-C PD and PPS chargers, ZVS can only be achieved at minimum V_{IN} and maximum V_{OUT} – at lower V_{OUT} levels, the reflected voltage is also lower – so valley-switching will occur at a finite non-zero voltage level, with no ZVS.

An existing QR design can be converted to ZVSF by transitioning from the QR controller to UCC28780, and by changing the local secondary-side SR controller to the isolated SR driver UCC5304. The PWMH output of the UCC28780 takes the place of the SR controller through the isolated driver. By building up just enough negative current, depending on V_{IN} and V_{OUT} levels, the ZVSF topology can achieve ZVS across the full range of V_{IN} and V_{OUT} , enhancing any QR stage into a ZVSF stage over the full operating range.

4 Simplified Application Diagram

Figure 4-1 shows a simplified application diagram using the UCC28780 primary-side controller and UCC5304 isolated SR driver.

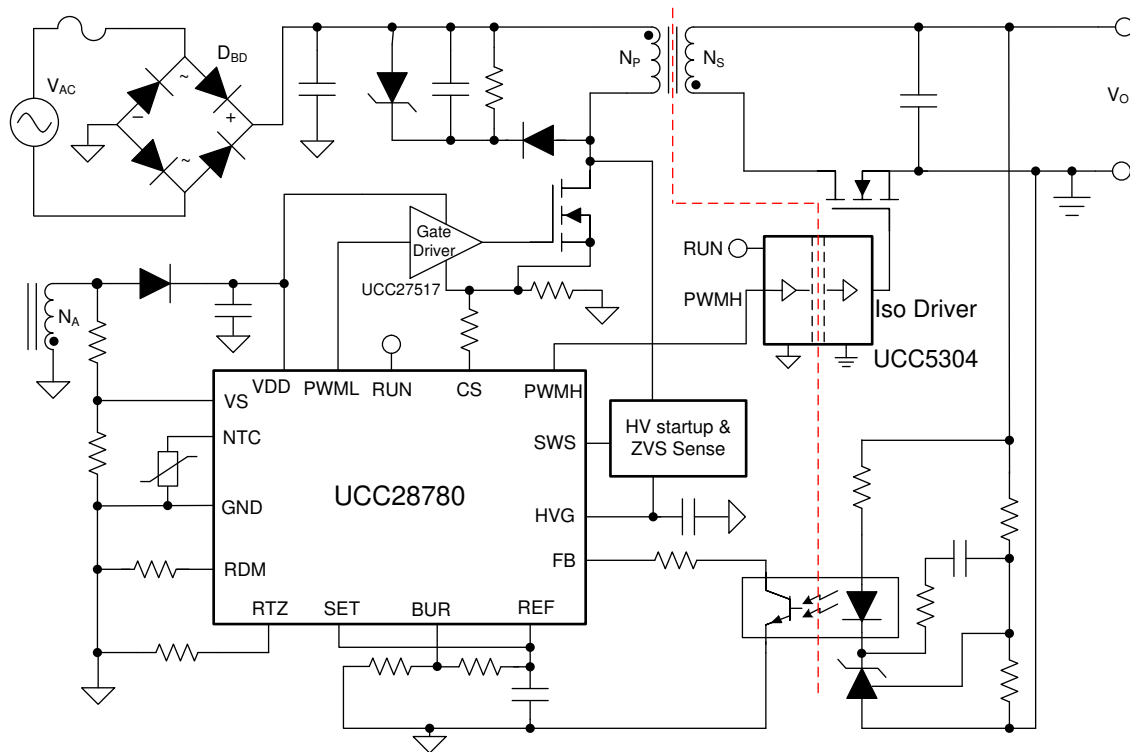


Figure 4-1. ZVSF Simplified Application Diagram

The UCC28780 SWS pin indirectly senses the primary FET drain voltage, and the SR on-time extension is auto-adjusted with changes in load current and bulk-capacitor voltage to achieve ZVS with minimal excess negative magnetizing current, to maximize efficiency. A primary-side RCD snubber is used to clamp the primary FET V_{DS} . An external low-side driver is used to interface the logic-level PWML drive signal to the primary FET gate.

The UCC5304 isolated driver is used to drive the SR across the reinforced isolation barrier between primary and secondary. The short propagation delay (28 ns typical) ensures short SR FET body-diode conduction time, to help improve efficiency.

5 ZVSF Advantages and Benefits

Table 5-1 summarizes the ZVSF benefits and advantages over QR in key applications.

Table 5-1. Summary of ZVSF Benefits and Advantages Over QR in Certain Key Applications

End Equipment/Application	Value of ZVSF over QR	Demonstrated Benefit/Result
Wide-input-range adaptor	Better high-line efficiency with high-frequency, small-size transformer due to ZVS benefit	QR @ 230 Vac 91.5~92% ZVSF @ 230 Vac ~93%
High-line-only or PFC front-end	Better efficiency from ZVS vs. QR 1 st -valley switching	QR @ 230 Vac ~93% ZVSF @ 230 Vac ~94% ACF-GaN @ 230 Vac ~95%+
Wide- V_{OUT} PD or PPS	Achieve ZVS across full V_{OUT} range	Commercial QR @ 230 Vac, 5 Vdc@15 W ~88% Commercial ZVS-Aux IPD2105 @ 230 Vac, 5 Vdc@10W ~82% ZVSF @ 230 Vac, 5 Vdc@15 W ~90%
Moderate-to-high-frequency designs for moderate density	High-frequency QR designs → efficiency/thermal limit at high-line ZVSF higher frequency and smaller transformer → same 90-V efficiency as QR, but better high-line efficiency Enables high frequency and medium power density WITHOUT need for GaN	Low-frequency 65-W QR ~60 kHz needs RM10-size (or similar) transformer ZVSF 65 W @ 180–200 kHz can use RM8-size transformer

6 Use of UCC28780 + UCC5304 to Implement ZVSF

As Figure 6-1 shows, the combination of UCC28780 controller and UCC5304 driver allows a ZVSF to be readily implemented using available ICs. As already noted, an existing QR design can readily be converted to ZVSF, using the schematic example.

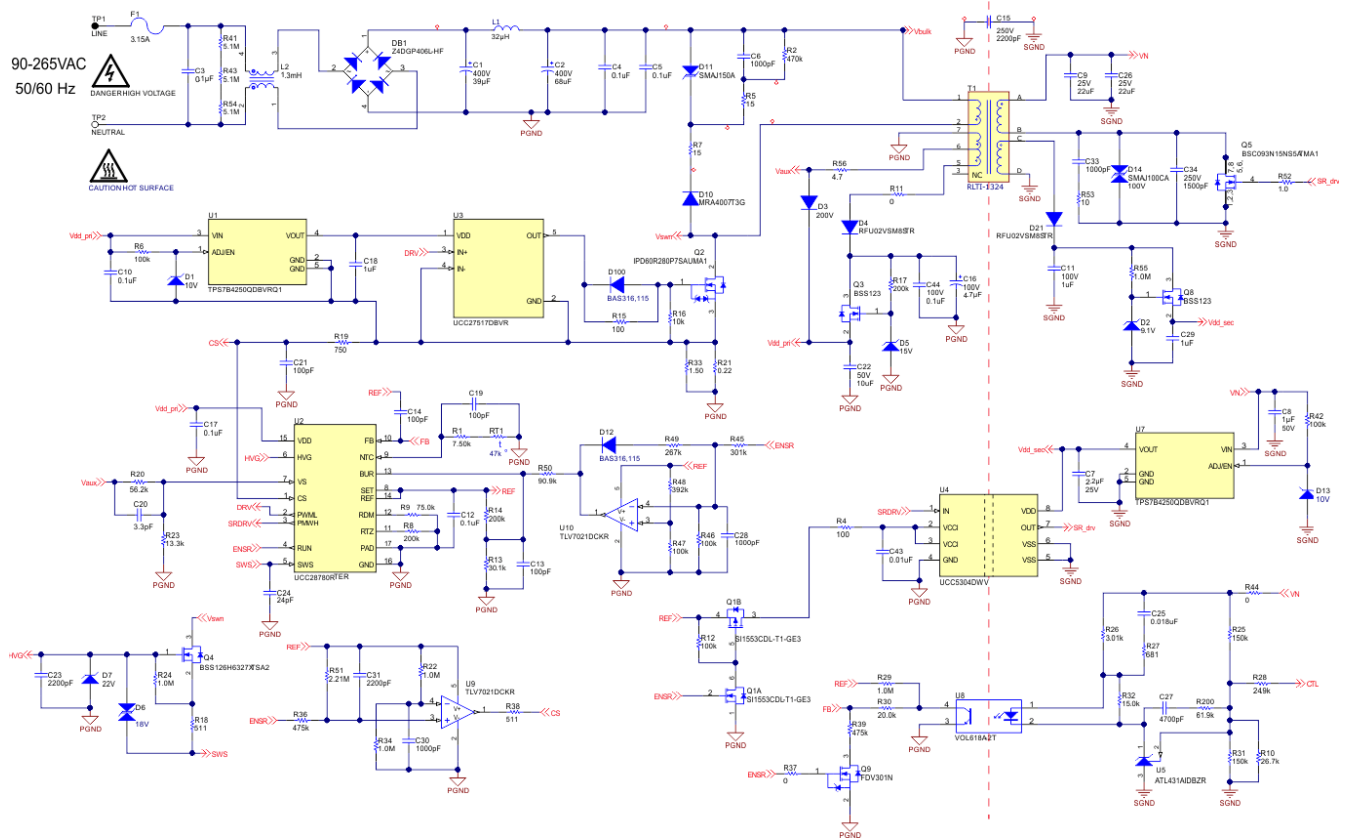


Figure 6-1. PMP2152 65-W ZVSF Schematic (Partial) Using UCC28780 + UCC5304

6.1 UCC28780 Key Features

- Adaptive ZVS control
- Adjustable timing via RDM and RTZ for different size power FETs
- Programmable burst-mode threshold via BUR pin
- Input Brownout detection and protection
- Extensive protections – overpower, overtemperature, output overvoltage, overcurrent, short-circuit and pin-faults
- RUN pin to allow the external iso-driver to be power-managed in stand-by and light load

6.2 UCC5304 Key Features

- Reinforced isolation to 7 kV_{peak}, 5 kV_{RMS}
- Single-channel SOIC-8 wide-body package for > 8.5 mm creepage distance
- Fast propagation delay 28 ns typical, 40 ns maximum
- Common-Mode-Transient-Immunity (CMTI) > 100 V/ns
- 4-A/6-A peak source/sink for fast SR turn on and turn off
- Wide operating range on secondary-side VDD, 5-18 V

6.3 Key Specifications

Table 6-1 lists the PMP21552 key specification parameters.

Table 6-1. PMP21552 Key Specification Parameters

PARAMETER	SYMBOL	VALUE	UNIT
Minimum input voltage (on bulk capacitor)	VDCin _{min}	75	V
Maximum input voltage (on bulk capacitor)	VDCin _{max}	375	V
Output Voltage (maximum of PD range)	V _{OUT}	20	V
Output load current (maximum)	I _{OUT}	3.25	A
Efficiency (target)	η	93	%
Secondary rectifier forward voltage drop	V _d	0.1	V
Maximum allowed primary FET V _{DS} stress (90% of 600-V rating)	V _{DS_max_pri}	540	V
Maximum allowed SR FET V _{DS} stress (90% of 150-V rating)	V _{DS_max_pri}	135	V
Target minimum switching frequency (at full load, VDCin _{min})	f _{sw_min}	110	kHz
Duty-cycle loss for resonant voltage transitions	K _{RES}	8	%

6.4 Power Stage Parameters

Choose N_{ps} = 5 — this gives approximately 100-V reflected voltage, and achieves a good compromise for the maximum V_{DS} stress targets for both primary FET and secondary SR.

$$N_{ps} := 5$$

$$D_{MAX} := \frac{N_{ps} \times (V_{OUT} + V_d)}{VDCin_{min} + N_{ps} \times (V_{OUT} + V_d)} = 0.573$$

$$L_M := \frac{D_{MAX}^2 \times VDCin_{min}^2 \times \eta}{2 \times V_{OUT} \times I_{OUT}} \times \frac{1}{f_{sw_min}} \times (1 - K_{RES}) = 110.366 \mu\text{H} \quad (1)$$

6.5 Schematic Detailed Description

6.5.1 EMI Filter

Differential-mode (DM) filtering is provided by C3 and the PI-filter formed by C1 + L1 + C2, C4, C5.

Common-mode (CM) filtering is provided by CM-choke L2 and Y-cap C15.

A shield/CM-balance layer inside transformer T1 also helps reduce the CM noise.

A grounded transformer flux-band (to PGND) and a Copper shield around the EMI filter and over the primary switch-node also help to reduce the EMI.

6.5.2 Power Stage

Transformer T1 uses an interleaved structure with secondary winding sandwiched between two half-primary windings; magnetizing inductance approximately 110 μH , $N_{ps} = 5$, leakage inductance approximately 1.8 μH (approximately 1.65%).

Primary MOSFET Q2 = IPD60R280P7S is chosen for a reasonable trade-off between $R_{DS(on)}$ and gate charge/capacitance. The reflected voltage is set to 100 V (at 20-V output) and the RCD snubber is damped to allow use of a 600-V FET and still achieve 90% derating margin.

Secondary-side SR Q5 = BSC093N15 150-V FET, again to give more than 90% derating margin.

6.5.3 RCD Snubber

R2, C6, and D10 are the main RCD-clamp snubber components. D10 is chosen to be a slow-recovery type to help reduce the leakage energy consumed by the snubber. Damping resistors R5 and R7 are added to damp out the leakage ring (see V_{DS} waveforms in [Section 8.6](#)), to improve EMI and reduce the maximum V_{DS} spike slightly. TVS D11 is added to help clamp transient V_{DS} spikes under short-duration transient events.

6.5.4 Low-Side Driver

A low-side driver U3 is used to level shift the TTL-level PWML signal from the controller to the higher level required to drive FET Q2. LDO U1 provides a regulated rail at ~ 10 V to U3 to clamp the gate drive level when V_{dd_pri} is too high.

6.5.5 HV Start-up and SWS Sensing

High-voltage depletion-mode FET Q4 (BSS126) is used to charge V_{dd_pri} at start-up; this eliminates the typical start-up bleed-resistor chain, saving stand-by power and allowing much faster start-up time. Associated components D6, D7, C23, C24, R18 and R24 provide various protections for Q4 under the various possible operating modes (start-up, pin/component faults, and so forth.)

After start-up is complete, Q4 performs an additional function of sensing the switched-node voltage to detect ZVS for the SWS input of the UCC28780, while blocking the high voltage.

6.5.6 I_{pk} Adjust Circuit

As shown in the [schematic diagram](#), the peak of the magnetizing current i_M is adjusted in order to regulate the output voltage as load power and input voltage vary.

At lighter loads, there is an efficiency benefit if the peak of the magnetizing current (I_{pk}) is increased somewhat, because higher I_{pk} at light load increases the per-cycle efficiency, reduces the number of cycles required (average switching frequency), and so increases overall efficiency in light load and reduces stand-by power.

U9 and associated components C30, C31, R22, R34, R36, and R51 provide an I_{pk} increase function in light-load and stand-by modes by forming a switched divider on the CS pin.

6.5.7 Burst-Mode Hysteresis Circuit

Optional U10 and associated components D12, R45, R46, R47, R48, R49, R50, and C28 add additional hysteresis to the BUR pin thresholds to help reduce possible audible noise at the burst-mode transitions.

6.5.8 Switched Supply Rail to UCC5304

Q1B, R12, R4, and C34 implement a switched supply rail for the isolated SR driver U4 – when the ENSR/RUN signal goes low for longer intervals in SBP/LPM mode, the VCCI rail to U4 is effectively disconnected to save bias and standby power.

6.5.9 Dual-Winding Aux Bias

Two primary-side auxiliary windings are used on the transformer to cope with the wide V_{OUT} range more efficiently. The tap at pin 6 connects directly to V_{dd_pri} through D3, R56, and provides V_{dd_pri} power when V_{OUT} is set to 12–20 V (lower auxiliary ratio to main secondary is 1:1). The upper tap at pin 5 (approx. 3:1 net

ratio to main secondary) provides power to Vdd_pri when V_{OUT} is < 12 V, with the higher ratio chosen to boost the auxiliary rail to ~ 12 V when V_{OUT} is as low as 4 V.

The LDO Q3, R17, D5, C44, C16, and C22 is needed to limit the aux rail generated by the upper rail when V_{OUT} is > 12 V. D5 is chosen to set the LDO regulated voltage low enough to be back-biased by the direct feed from the lower aux when V_{OUT} is high enough, to increase overall efficiency.

6.5.10 Active-Ripple-Cancellation Circuit

Q9, R37, and R39 are used to add hysteresis to the FB pin in burst-mode, to help stabilize the burst-mode operation and deliver consistent burst lengths.

6.5.11 Secondary-Side Aux Bias for UCC5304

A secondary-referenced aux winding C-D connects to D21, C11 and to LDO Q6, R55, D2 and C29 to generate a secondary bias rail VDD for the isolated driver's output. The turns ratio of 2:1 with respect to the main secondary ensures adequate gate-drive level for the SR FET when V_{OUT} is at the 5-V level. LDO Q6/D2 limit the VDD rail at higher V_{OUT} levels. To improve efficiency at high V_{OUT} levels 15-20 V, a second LDO U7 is used to power VDD directly from V_{OUT} .

6.5.12 ATL431 Feedback Regulation and USB Type-C™ PD Interface

The feedback regulation circuit U5, C27, R32, R26, R25, and R31 is used to closed-loop control the current pulled from the FB pin in order to regulate V_{OUT} at the desired level. R27 and C25 are added to provide phase-boost for control-loop stability. R28 connects to the USB-C PD controller, which controls how much current is pulled through R28 in order to set the required PD voltage that is commanded by the USB Type-C load device.

7 PMP21552 EVM

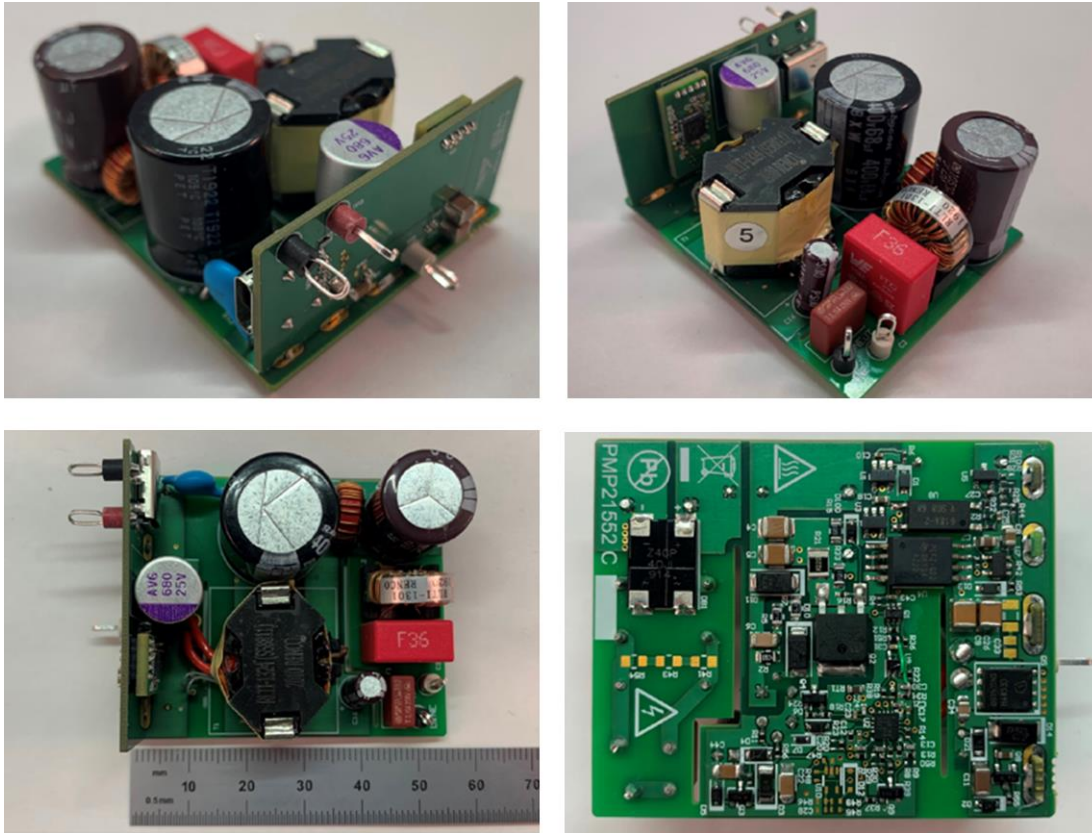


Figure 7-1. PMP21552 65-W ZVSF Reference Design PCB Assembly Using UCC28780 + UCC5304

PMP21552 is a released reference design for a 65-W USB-C PD adapter, using the UCC28780 and UCC5304 chipset in a ZVSF topology. The design supports 5 V/3 A, 9 V/3 A, 15 V/3 A and 20 V/3.25 A in a compact 62-cc size (open-frame dimensions 45 × 55 × 25 mm). Full-load efficiency is over 92.5% across the full universal 90-265 V AC range. The primary-side switch uses a Si super-junction FET, the transformer size is RM8, and the design passes EN55022 level-B conducted and radiated emissions with margin.

8 PMP21552 Performance Results

Full details of the PMP21552 design and performance are available online in the [65-W USB Type-C ZVS-Flyback Reference Design](#). Selected performance highlights are shown here. Efficiency data does not include the USB Type-C cable loss.

8.1 Efficiency

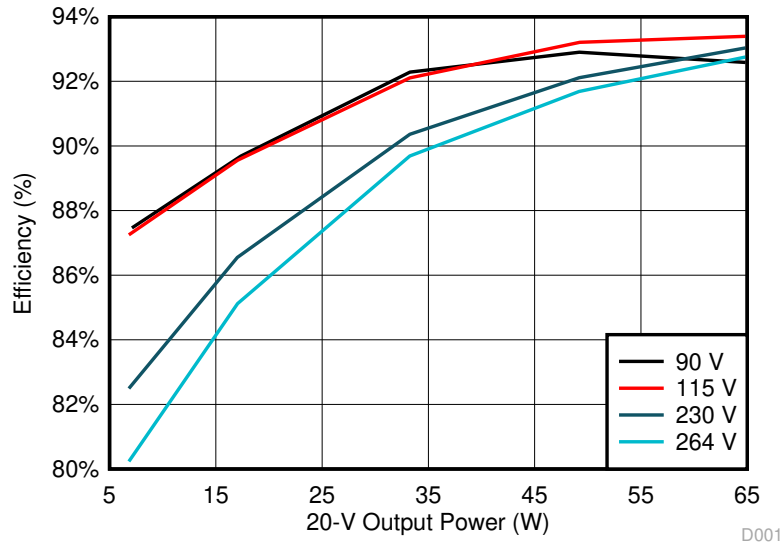


Figure 8-1. PMP21552 65-W ZVSF Efficiency vs Load/Line at 20-V Output

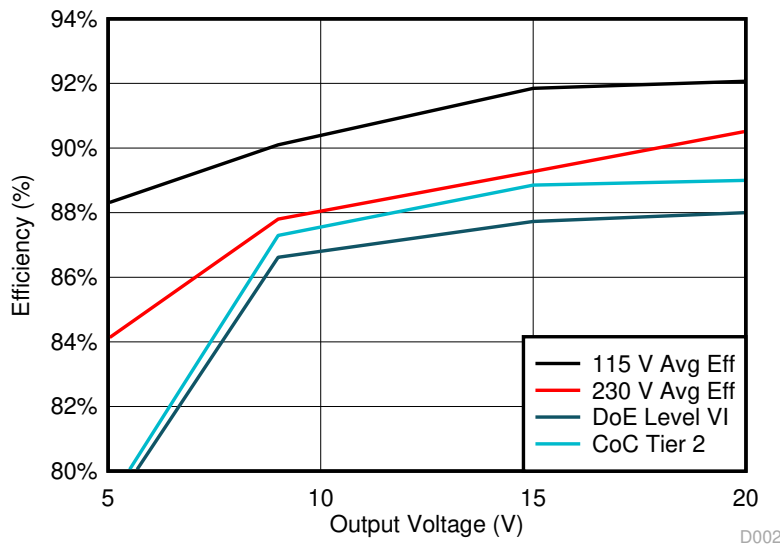


Figure 8-2. PMP21552 65-W ZVSF Average Efficiency vs V_{OUT} and Line

8.2 Stand-by Power

Table 8-1 lists the stand-by power measurement results.

Table 8-1. Stand-by Power Measurement Results

Stand-by Power (5 V, no Load)	
115 Vac	230 Vac
26 mW	30 mW

8.3 “Tiny-Load” (0.25 W) Efficiency

Table 8-2 lists the “tiny-load” measurement results.

Table 8-2. “Tiny-Load” Measurement Results

“Tiny Load” 250-mW Output Power at 20 V		
	115 Vac	230 Vac
Input power	370 mW	394 mW
Efficiency	68%	63%

8.4 Conducted EMI

8.4.1 Passes EN55032 Level-B QP and AVG With Margin

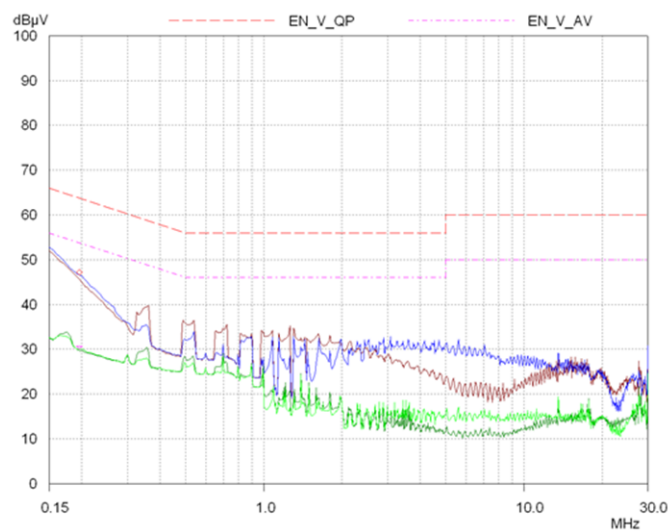


Figure 8-3. PMP21552 65-W ZVSF QP and AVG Conducted Emissions at 115 V, 20-V, 65-W, Earthed Load; L1 (L) and L2 (N)

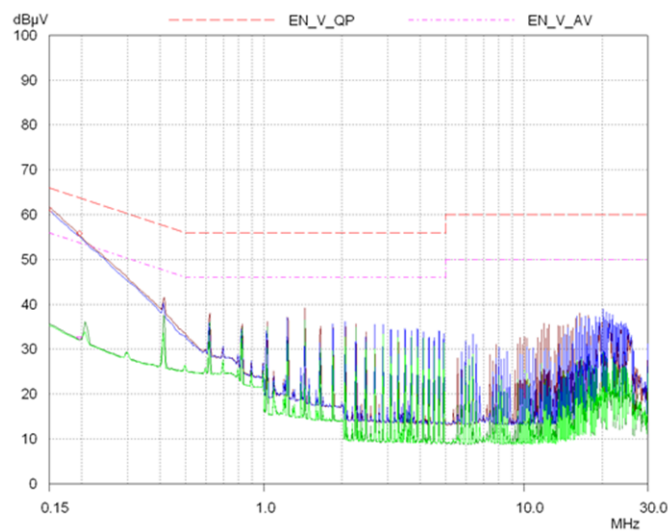


Figure 8-4. PMP21552 65-W ZVSF QP and AVG Conducted Emissions at 230 V, 20-V, 65-W, Earthed Load; L1 (L) and L2 (N)

8.5 Radiated EMI

8.5.1 Passes EN55032 Level-B Vertical and Horizontal Polarization With Margin

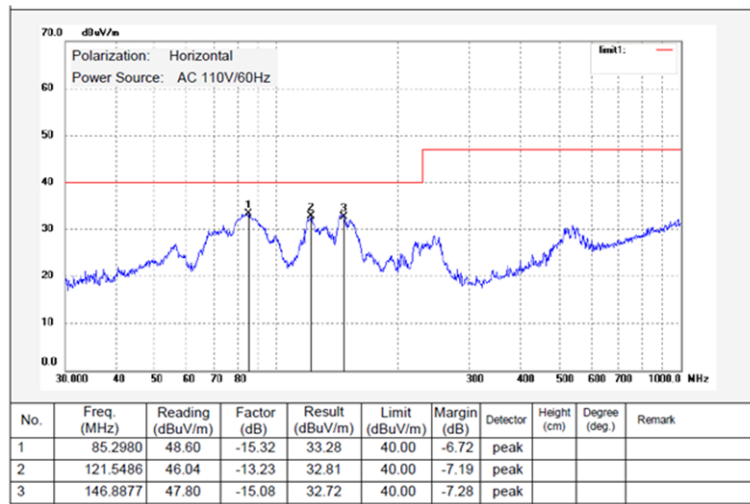


Figure 8-5. PMP21552 65-W ZVSF Radiated Emissions at 115 V, 20-V, 65-W, Earthed Load, Horizontal Polarization

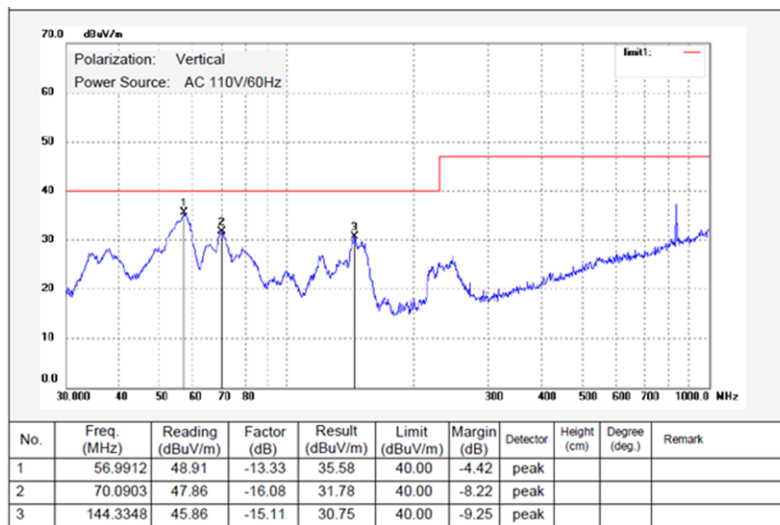


Figure 8-6. PMP21552 65-W ZVSF Radiated Emissions at 115 V, 20-V, 65-W, Earthed Load, Vertical Polarization

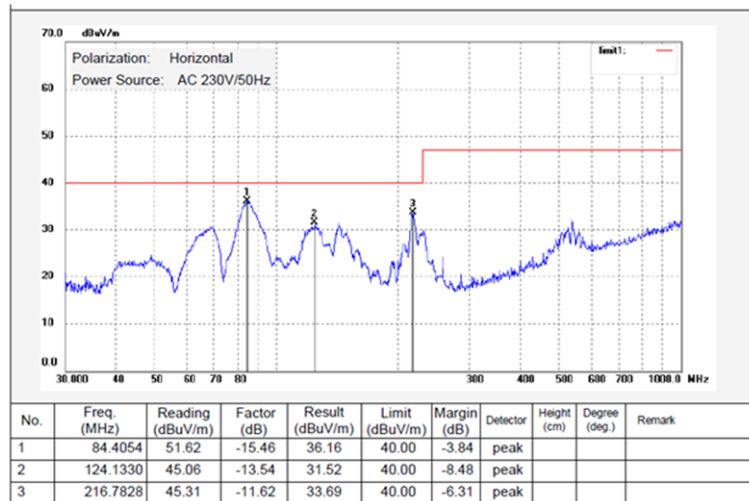


Figure 8-7. PMP21552 65-W ZVSF Radiated Emissions at 230 V, 20-V, 65-W, Earthed Load, Horizontal Polarization

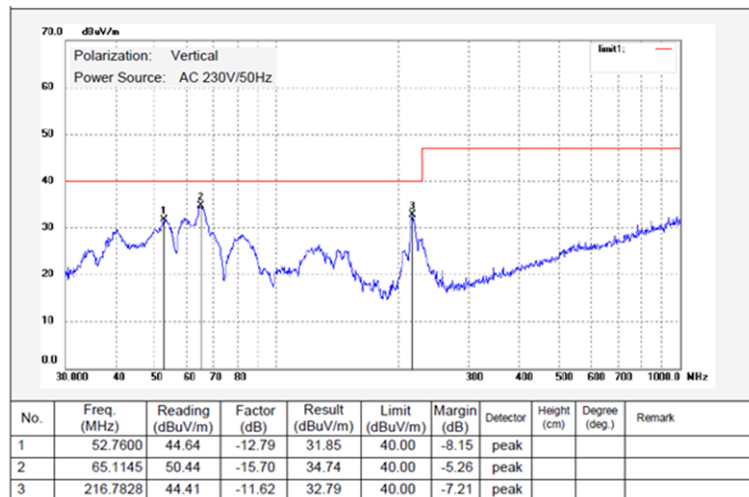


Figure 8-8. PMP21552 65-W ZVSF Radiated Emissions at 230 V, 20-V, 65-W, Earthed Load, Vertical Polarization

8.6 Switching Waveforms

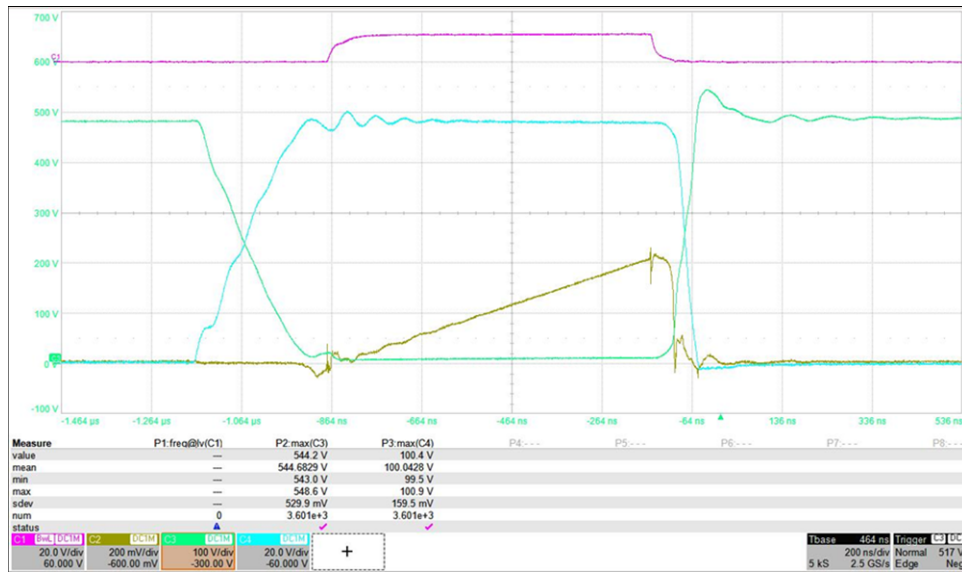


Figure 8-9. PMP21552 65-W ZVSF Waveforms at 264-V Input, 20-V, 65-W Output; Ch1: Pri Vgs; Ch2: Pri Vrcs; Ch3: Pri Vds; Ch4: sec SR Vds

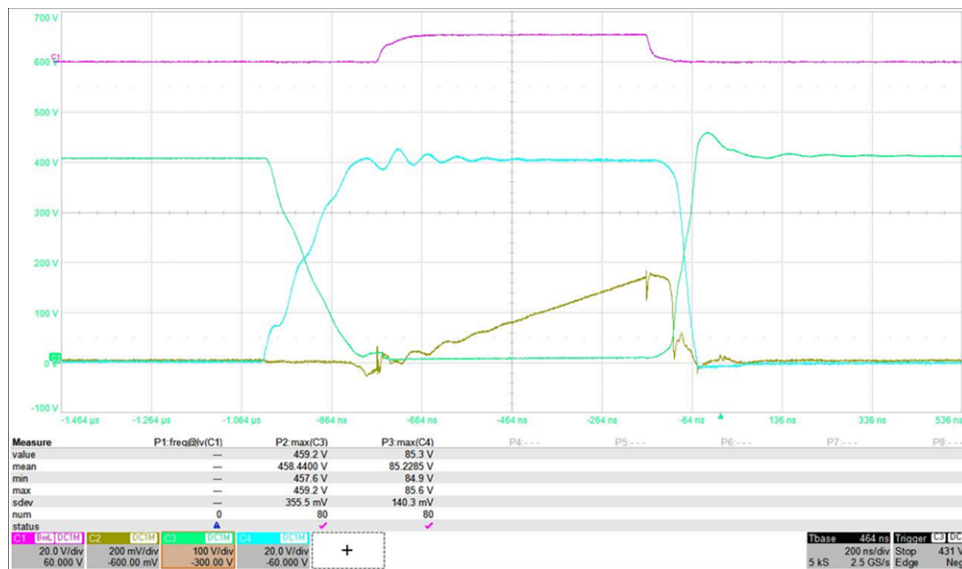


Figure 8-10. PMP21552 65-W ZVSF Waveforms at 264-V Input, 5-V, 15-W Output; Ch1: Pri Vgs; Ch2: Pri Vrcs; Ch3: Pri Vds; Ch4: sec SR Vds

9 Summary

For high-volume applications where higher efficiency and power-density are required, or higher switching frequency and smaller size are required, the ZVSF topology is worth considering. It offers performance advantages over QR and fixed-frequency single-switch flyback topologies. While it cannot deliver the same efficiency and power-density performance as ACF, it does offer a simpler, lower component-count alternative.

The chipset of UCC28780 and UCC5304 are available from TI to implement the topology, along with a reference design PMP21552 to help users get started.

10 References

- UCC28780 product folder: <http://www.ti.com/product/UCC28780>
- UCC5304 product folder: <http://www.ti.com/product/UCC5304>
- ZVSF reference design PMP21552 folder: <http://www.ti.com/tool/PMP21552>
- ACF-Si reference design PMP21479 folder: <http://www.ti.com/tool/PMP21479>

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