APPLICATION NOTE U-164

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THE UCC3884 FREQUENCY FOLDBACK PULSE WIDTH MODULATOR

UNITRODE

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by Philip Cooke

ABSTRACT

This application note focuses on the UCC3884 frequency foldback peak current mode controller. The UCC3884 provides a solution to the current tail problem often seen in high frequency converters under overload fault conditions. Intended primarily for single-ended converters, other features such as a maximum duty-cycle clamp and an accurate volt-second clamp are also included. The block diagram and the main features of the UCC3884 will be presented in the theory of operation section. Following that a derivation of the oscillator, frequency foldback, and volt-second clamp equations are given. Finally, design details and test results for an example RCD clamp forward converter operating at 400kHz are shown.

INTRODUCTION

The output VI characteristic of high frequency, buck-derived, peak current mode converters can exhibit a current tail during current overload conditions. This overload may be caused by a short circuit condition or a low impedance at the power stage output. The current tail is actually a gradual increase in the average output current as the average output voltage decreases toward zero. The peak current limit in a PWM controller commands the power stage switch off during overcurrent conditions which should limit the maximum average output current. However, the propagation delay inherent in the controller and in the power switch during turn-off limits the minimum attainable duty cycle [1]. This minimum duty cycle limit can produce a current tail during overloads. Upon close inspection one finds that this propagation delay exists collectively between the current sense (CS pin) and the output (OUT pin) of the integrated circuit (IC) and the turn-off delay of the power stage switch. The reduction of the propagation delays for a given IC and power stage design can help, but tends to increase system cost. An alternate method is needed to reduce the delays and thus the excessive currents during a fault. One possible technique is implemented in the oscillator section of the UCC3884. During a fault condition as the output voltage approaches zero the operating frequency also decreases. By reducing the frequency during overload conditions the duty-cycle is permitted to decrease below the value previously limited by propagation delay in the constant frequency converter. The UCC3884 reduces the frequency smoothly as the load impedance approaches a short circuit, thus preventing possible latch-up with nonlinear loads [1]. This effectively diminishes the current tail in the output VI characteristic.

The UCC3884 is intended for high performance, peak current mode, single-ended applications that can benefit from frequency foldback. This frequency reduction only operates when the output voltage is below a user programmable value. More specifically, the oscillator runs at constant frequency and only folds back when the output voltage drops below a given value (e.g., 4.2V for a 5V output). A volt-second clamp circuit is also included that allows accurate duty-cycle clamping under transient line and load conditions providing an extra level of circuit protection from transformer saturation. For example, if a sudden increase in load power occurs while the input voltage increases, the applied volt-seconds could be enough to saturate the transformer, which could cause the power switch to fail. In this case, the volt-second clamp circuit could be used to prevent the failure of the power switch by overriding the control loop and limiting the applied volt-seconds. This controller also features a depletion-mode n-channel MOSFET gate drive intended to be used in the bias supply during start up. A reduction in both the size of the start up storage capacitor and turn-on time can be achieved by using an external depletion-mode device.

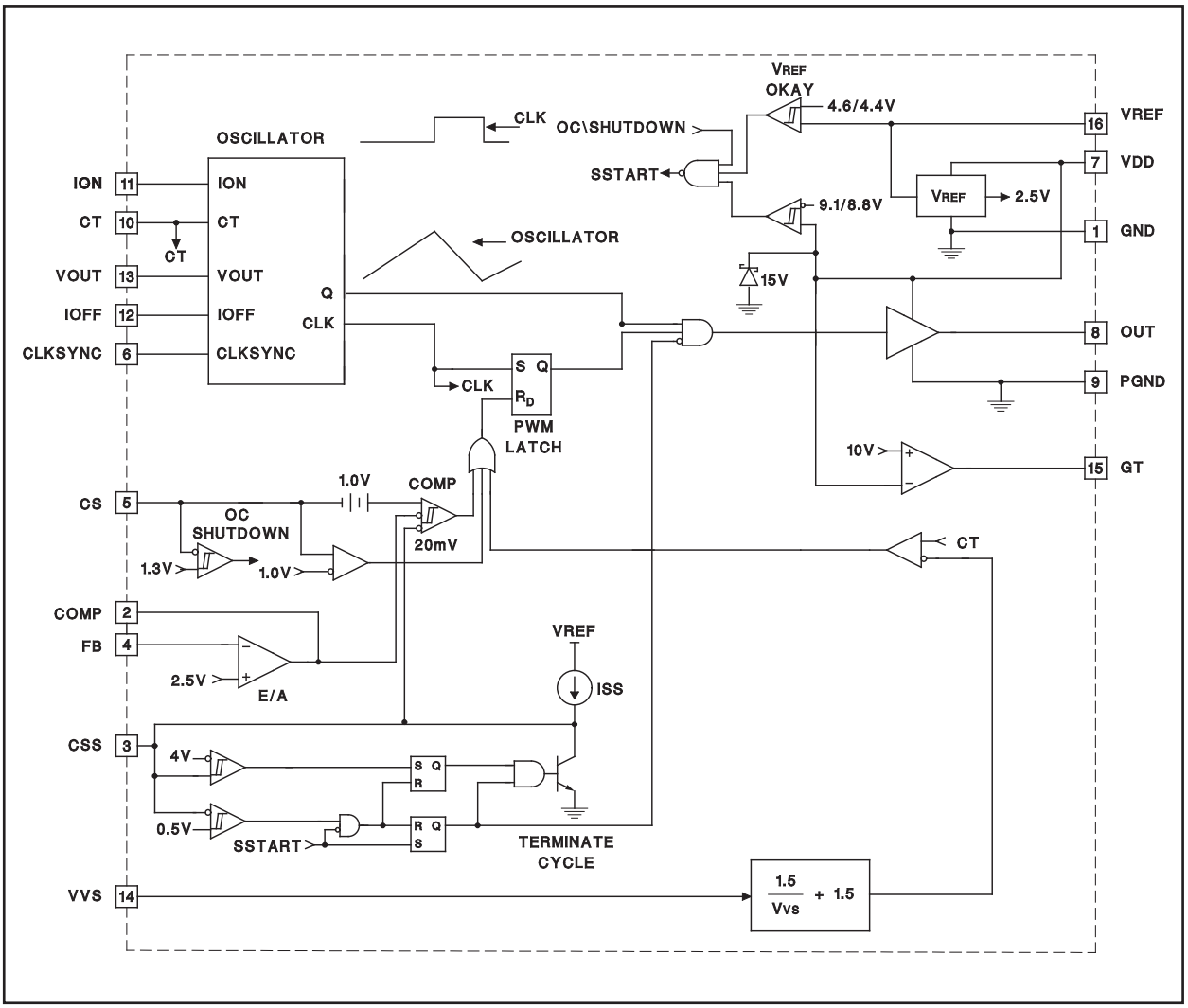

Figure 1. UCC3884 Block Diagram

THEORY OF OPERATION

The UCC3884 current mode controller, shown in Figure 1, contains a programmable oscillator section which includes the ability to synchronize multiply PWMs. The positive and negative sloped portions of the oscillator waveform (measured at CT, the connection point for the timing capacitor) have time intervals that are set by external resistors at ION and IOFF as shown in Figure 2. The nominal operating frequency is determined by the timing capacitor during non-frequency foldback conditions, that is, with the output voltage at its regulated value. The positive sloped portion of the oscillator waveform has a fixed time duration and is set by a resistor connected to ION. In a similar fashion the off-time is set by a resistor at IOFF. However, the negative sloped portion of the oscillator waveform is extended in time as the measured output voltage decreases providing protection during output faults. When the voltage at VOUT decreases below 3.5V, due to an output short circuit, the operating period increases and the IC is in frequency foldback operation. It should be emphasized that normal converter operation, except during start up, is at a fixed frequency.

The power supply output voltage and the voltage from VREF can be fed back into VOUT with summing resistors. This ensures a minimum frequency at startup and during short circuit conditions when the output voltage is zero. Figure 3 shows computer simulated VI curves for a 417kHz forward converter, one with frequency foldback and one without frequency foldback. The total propagation delay was set to 150ns in this computer model of a forward converter with 48V input (8:2 turns ratio). Power stage component values were L = 1.3µH with a DCR of 0.01Ω and C = 10000µF with an ESR of 70mΩ [1]. It can be seen that the current tail is reduced with frequency foldback. Figure 4 further details the effect of the propagation delay. Two simulations were done at the same operating frequency both without frequency foldback. The simulation with the current tail approaching 22A had a 150ns delay and the other

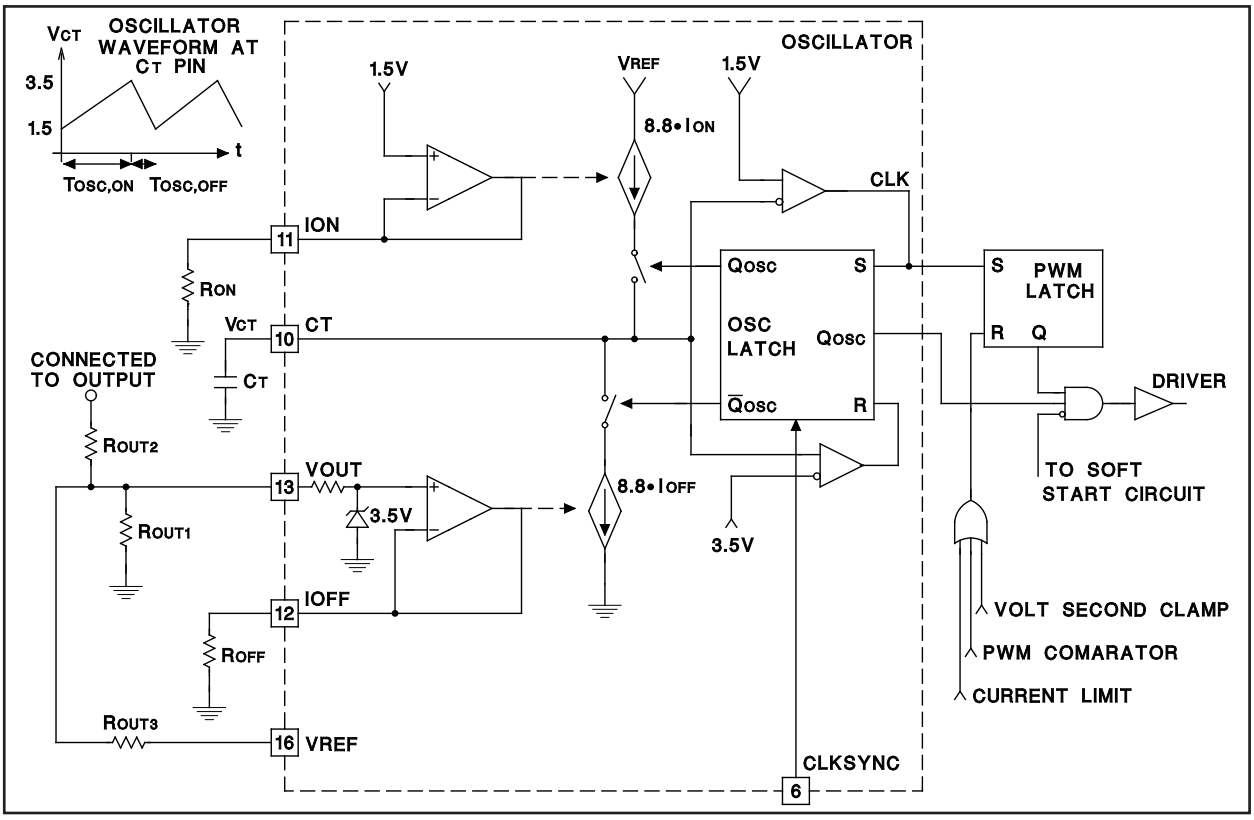

Figure 2. Functional Block Diagram of the UCC3884 Oscillator

had an unrealistic, nearly zero, 1.0ns delay. It is clear that the propagation delay can cause significant overcurrents and frequency foldback is a practical way to reduce the current tail effect.

Another feature included in the UCC3884 is an interface to drive an external depletion-mode MOSFET during power supply startup until the bootstrap winding exceeds a 10V threshold. At which time the depletion-mode MOSFET is turned-off. The internal amplifier controlling this MOSFET has 300mV of hysteresis to avoid oscillation during power-up.

An accurate programmable volt-second method to clamp the duty-cycle is implemented. It is configured so that the duty-cycle limit is inversely proportional to input voltage and a resistor divider network is used to program the proportionality constant. At a given input voltage and constant load, assuming regulation, the operating duty-cycle is a fixed value. The volt-second clamp duty-cycle may then be set somewhat higher than this operating duty-cycle. Since the volt-second duty-cycle limit is inversely proportional to V_{IN} at any other constant input voltage level, the volt-second clamp will still exceed

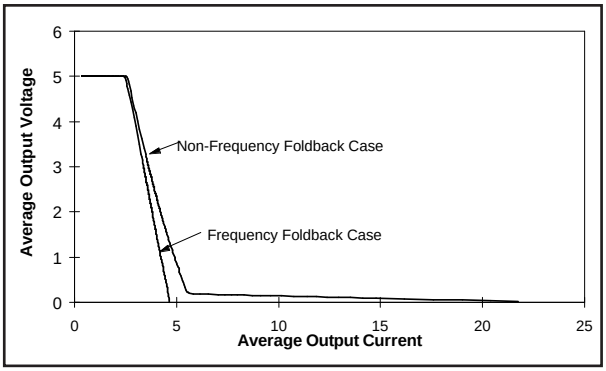

Figure 3. Frequency and Non-Frequency Foldback Comparision

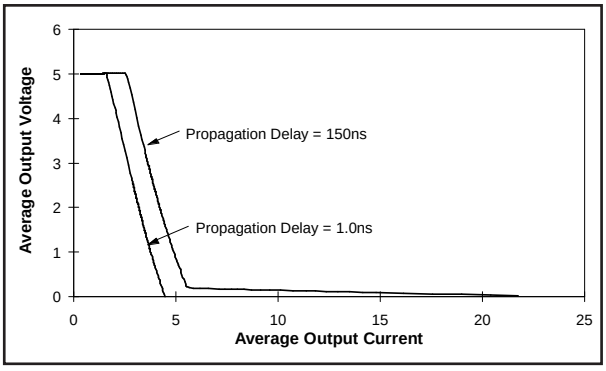

Figure 4. Non-Frequency Foldback with 1.0ns and 150ns Propagation Delays

the steady state operating duty-cycle as shown in Figure 5. This allows normal current-programmed closed-loop operation of the converter without the volt-second duty-cycle limit interfering with the control. For example, during a load transient and possibly an input voltage transient the volt-second clamp can accurately limit the maximum applied volt-seconds by limiting the duty-cycle. This ensures that the transformer does not saturate during a fault which could otherwise fail the power supply. After the fault passes the converter will go back into regulation.

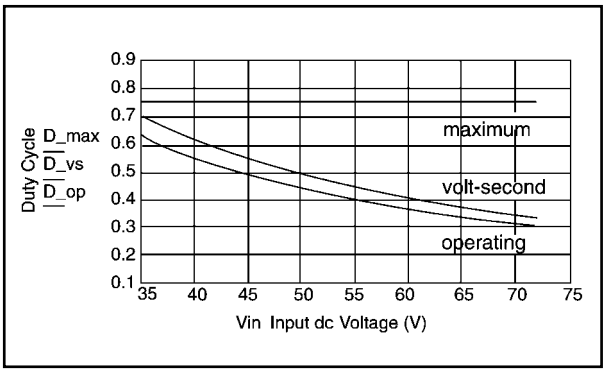

Figure 5. Various Duty Cycles

An external capacitor may be connected to CSS which provides for a soft-start and also allows the IC to be disabled with an external transistor. The frequency foldback and the soft-start functions will both be in effect during power-up since the output voltage fed back to the VOUT pin is less than 3.5V and the voltage on CSS is less than 4V. The increasing on-time at the OUT pin during soft-start is controlled by C_{SS} and the period is controlled by the frequency foldback circuitry. When an overload or short circuit occurs the frequency foldback circuit and possibly the volt-second clamp circuit is activated (assuming the overcurrent is not triggered). In each design the steady state VI characteristic produced by the frequency foldback circuit should be compared to the load VI curve to be certain that the converter will start under load.

The current sense feedback pin has an over current protection feature which forces a soft-start cycle only if the IC is not currently in a soft-start cycle. A voltage bias of 1.0V is added to the voltage sensed on the CS pin in order to facilitate zero duty-cycle when the error amplifier's output is less than 1.0V. The PWM latch is reset dominant so that if the error amplifier output is below 1.0V the output of the latch is not driven high.

The error amplifier is unity gain stable and has a wide gain-bandwidth product for accuracy. Its non-inverting input is internally set to 2.5V.

DETAILED DESCRIPTION AND DESIGN EQUATIONS

A description of the UCC3884 BiCMOS pulse width modulator and design equations will be presented followed by an example RCD Clamped Forward Converter design using the UCC3884 peak current mode controller [2,3,4].

Oscillator and Frequency Foldback Section:

The oscillator section has an independently programmable frequency and a maximum duty-cycle clamp. A single resistor sets the timing capacitor (CT) charge current which creates the positive slope portion of the oscillator waveform. A second resistor sets the timing capacitor discharge time. With reference to Figure 2 the oscillator waveform increases linearly from 1.5V to 3.5V and decreases linearly back to 1.5V completing one cycle. If T_{OSCon} represents the charge time and T_{OSCoff} is the discharge time then the frequency of the converter is given by

$$f = \frac{1}{T_{OSCon} + T_{OSCoff}} . \quad (1)$$

The output of the modulator can only be asserted during the positive slope portion of the oscillator waveform. With this limitation the maximum duty-cycle is given by the ratio of T_{OSCon} to $T_{OSCon} + T_{OSCoff}$;

$$D_{MAX} = \frac{T_{OSCon}}{T_{OSCon} + T_{OSCoff}} . \quad (2)$$

The oscillator off-time is a function of the main output voltage only if the VOUT pin drops below 3.5V. The VOUT pin may exceed 3.5V in which case the off-time is calculated using 3.5V. Note that the IC does not internally clamp this voltage to 3.5V. If the output is short circuited or a low impedance load is applied the feedback voltage to the VOUT pin decreases which causes T_{OSCoff} to increase. This will increase the period and therefore decrease the frequency.

Recall that the oscillator on-time (T_{OSCon}) is constant and does not vary with output voltage. Under nominal operating conditions the frequency is constant and equation 1 can be expanded to

$$f = \frac{1}{\frac{C_T \bullet (3.5 - 1.5)}{8.8 \bullet I_{ON}} + \frac{C_T \bullet (3.5 - 1.5)}{8.8 \bullet I_{OFF}}} = \quad (3)$$

$$\frac{1}{0.227 \bullet C_T \bullet \left(\frac{1}{I_{ON}} + \frac{1}{I_{OFF}}\right)} =$$

$$\frac{4.4}{C_T \bullet \left(\frac{R_{ON}}{1.5} + \frac{R_{OFF}}{3.5}\right)}$$

where C_T is the timing capacitor, R_{ON} sets the value of the C_T charging current, (8.8 • I_{ON}), and R_{OFF} sets the value of the C_T discharging current, (8.8 • I_{OFF}). The maximum current sourced from the ION and IOFF pins is limited to approximately 800µA.

To avoid start up problems, a resistor can be added from VREF to VOUT which provides a voltage bias to VOUT even when the output voltage is zero. The choice of value also sets the minimum operating frequency during frequency foldback, as will be reviewed in the example design section below.

Designs using an isolation transformer can derive a dc voltage level proportional to the output by using a peak detector circuit off of the bootstrap winding of the power transformer (Figure 8). This bias supply is normally required for isolated converters and therefore requires only a minimum of components.

Figure 6 shows the oscillator and frequency foldback portions of the UCC3884, where V_X is found by assuming no limiting action within the VOUT pin (see also Figure 2). V_X is given as

$$V_X = \frac{R_{OUT1} \| R_{OUT2}}{R_{OUT1} \| R_{OUT2} + R_{OUT3}} \bullet V_{REF} + \frac{R_{OUT1} \| R_{OUT3}}{R_{OUT1} \| R_{OUT3} + R_{OUT2}} \bullet V_O \quad (4)$$

where V_{REF} = 5V, V_O is the output voltage, and || represents parallel resistors. If equation 4 yields a V_X greater than 3.5V it would then be replaced with 3.5V. One possible design approach would be to ignore the loading of R_{OUT3} and set V_X slightly below the output voltage minus one-half of the maximum ripple voltage. With R_{OUT1} and R_{OUT2} known, set V_O = 0 and R_{OUT3} may be calculated based upon the minimum operating frequency desired.

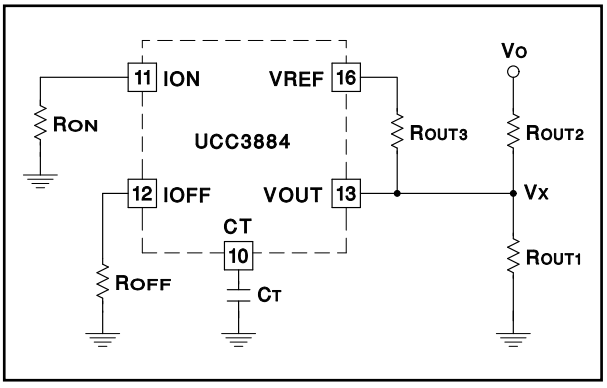

Figure 6. Oscillator and Frequency Foldback Connections to the UCC3884

Synchronization of Multiple ICs:

A CLKSYNC pin is provided which is used to synchronize two or more UCC3884 ICs. Multiple ICs are synchronized in frequency by connecting their CLKSYNC pins with capacitors to the CLKSYNC bus as shown in Figure 7. Each free running oscillator is designed with the same base frequency and the same maximum duty-cycle and is connected to the CLKSYNC bus with a capacitor and a pull-down resistor. A negative edged pulse from any IC will initialize all the ICs to start the upslope of their oscillator waveforms. For a given oscillator on the down-slope, if it receives a negative synchronization pulse before it reaches the 1.5V threshold, an internal MOS switch will quickly discharge its C_T down to 1.5V. After soft-start synchronization for each controller may take one or two cycles to come into lock. During frequency foldback under an output fault condition, the synchronization in the overloaded IC is inhibited and the converters can become unlocked. This is necessary since the overloaded ICs frequency is in foldback. The oscillators will resynchronize when the fault is removed. Due to tolerances, each free running oscillator frequency may be slightly different; therefore the CLKSYNC bus synchronizes to the highest frequency. For multiple PWM converters, synchronization to other controllers is only possible when the VOUT pin is greater than 3V.

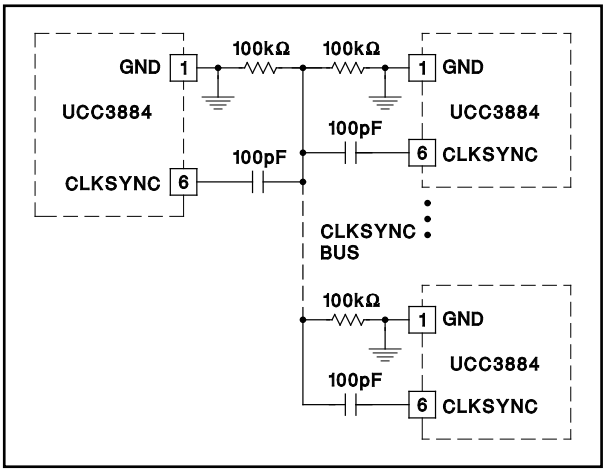

Figure 7. Oscillator Synchronization Connection Diagram

Volt-Second Clamp:

The volt-second duty-cycle clamp operates by taking the reciprocal of the voltage on VVS (see Figure 1) which is directly proportional to the input voltage and uses this signal to limit the duty-cycle. As V_{IN} increases, to maintain constant operating volt-seconds for a forward converter, the duty-cycle

decreases based upon

$$D_{OP} = \frac{V_O + V_D}{(V_{IN} - V_{DSon}) \bullet \frac{N_S}{N_P}}; \quad (5)$$

where D_{OP} is the operating duty-cycle, V_{DSon} is the on-state drain-to-source primary switch voltage, N_S is the secondary turns, N_P is the primary turns, and V_D is the voltage drop of the secondary rectifier diode [5]. In a similar fashion, the maximum duty-cycle clamp due to this volt-second function will also decrease and is given by

$$D_{VS} = \frac{K}{V_{VS}} \bullet \frac{T_{OSCon}}{T_{OSCon} + T_{OSCoff}} \quad (6)$$

$$= 1.1 \bullet \frac{D_{MAX}}{V_{VS}}$$

where D_{VS} is the duty-cycle clamp based upon applied volt-seconds to the transformer, V_{VS} is the voltage on the VVS pin, and K was calculated from

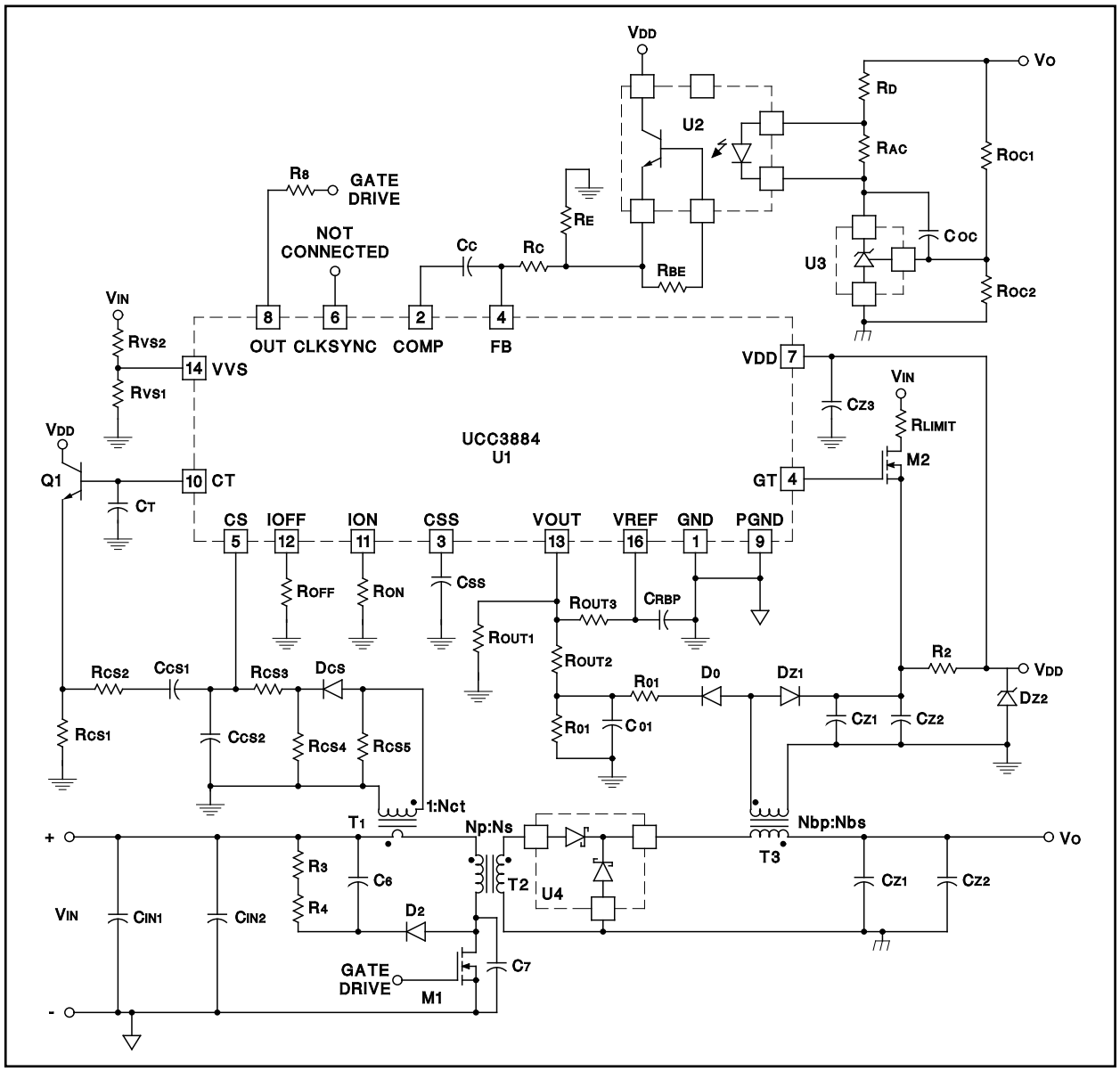

Figure 8. RCD Clamp Forward Converter with Frequency Foldback

the UCC3884 data sheet. The volt-second clamp is set by an external resistor divider network from the input voltage to the VVS pin. Normally, D_{VS} is chosen to exceed D_{OP} by some fixed percentage, say 10%. It may be necessary to put a small ceramic capacitor at the VVS pin to filter switching noise.

This feature allows for an accurate volt-second clamp within the input voltage range under load transient conditions. It is accurate since the timing capacitor tolerance does not effect equation 6. The voltage at VVS can be provided by 1% resistors and the internal accuracy is maintained to 3% (for the 0°C to 70°C temperature range). To limit the on-time at the minimum input voltage the maximum possible duty-cycle is clamped by D_{MAX}. The converters' actual duty-cycle can be limited by either the volt-second clamp or the maximum programmable duty-cycle clamp depending on operating conditions.

Soft-Start Operation:

A constant current source ISS, set internally to 20µA, charges C_{SS} to a clamped voltage level of typically 5.0V. The soft-start time is given by $3.5 \bullet C_{SS}/I_{SS}$. During start up the PWM comparator selects the minimum of either the error amplifier output or the soft-start capacitor voltage. The output duty-cycle is therefore slowly increased as the voltage at CSS increases. At some point the error amplifier voltage is lower and the voltage loop is closed. An overcurrent fault will initiate a soft-start cycle by first discharging C_{SS} and then slowly recharging the capacitor until the voltage returns to 4V. Soft-start discharge can only be activated when the voltage at C_{SS} exceeds about 4V.

Under Voltage Lockout Features:

The converter is disabled until VREF exceeds 4.6V and VDD exceeds 9.1V. Once these levels are reached the converter will begin the soft-start sequence. If VREF falls below 4.4V or VDD decreases below 8.8V the converter will immediately discharge C_{SS} and then start up again when VREF exceeds 4.6V and VDD exceeds 9.1V.

DESIGN EXAMPLE

A forward converter with an RCD clamp and a maximum of 75% duty-cycle at 400kHz was designed as shown in Figure 8 [1,2,3,4,6]. The input voltage range is 35V to 72Vdc with a 5V output. The highest operating duty-cycle is set to about 65% and will occur at the minimum input voltage during normal conditions. A maximum duty-cycle limit ensures reset of the transformer at low line.

Power Circuit Design:

A high frequency forward converter topology is often used in telecommunications applications requiring battery input from 35V to 72V DC with 48V nominal. A common output voltage is 5V and in this design a large capacitor, 10000µF, will be used to smooth the low frequency ripple components in order to more accurately measure average load currents during overload conditions. The output inductor was selected to be 1.3µH with a coupled winding for the bootstrap circuit (5:2 turns ratio). The transformer primary to secondary turns ratio is 8:2 and a RCD clamp is used to reset the transformer during the switch off-time. The laboratory prototype was built using higher rated components than necessary (maximum of 178W). This was done since constant measurement of short circuit fault currents without frequency foldback could cause excessive power dissipation.

Oscillator Design:

The oscillator on-time can be found, assuming D_{MAX} and f is known, by solving

$$D_{MAX} = \frac{T_{OSCon}}{T_{OSCon} + T_{OSCoff}} = T_{OSCon} \bullet f \quad (7)$$

for T_{OSCon} yielding

$$T_{OSCon} = \frac{D_{MAX}}{f} = \frac{C_T \bullet (3.5 - 1.5)}{8.8 \bullet I_{ON}} = \frac{C_T}{4.4 \bullet I_{ON}} \quad . \quad (8)$$

From equation 1, T_{OSCoff} becomes

$$T_{OSCoff} = \frac{1}{f} - T_{OSCon} \quad (9)$$

The oscillator operating frequency is given by

$$f = \frac{1}{2 \bullet 10^4 \bullet C_T} \quad . \quad (10)$$

Solving for C_T yields

$$C_T = \frac{1}{2 \bullet 10^4 \bullet f} \quad . \quad (11)$$

With T_{OSCon} and C_T known, I_{ON} may be found from equation 8

$$I_{ON} = \frac{C_T}{4.4 \bullet T_{OSCon}} \quad . \quad (12)$$

Now R_{ON} is given by

$$R_{ON} = \frac{1.5}{I_{ON}} \ . \qquad (13)$$

The next step is to calculate the maximum value of I_{OFF} which occurs during non-frequency foldback conditions. A portion of equation 3, repeated below,

$$f = \frac{1}{0.227 \bullet C_T \bullet \left(\frac{1}{I_{ON}} + \frac{1}{I_{OFF}}\right)} \qquad (14)$$

may be solved for I_{OFF} yielding

$$I_{OFF} = \frac{0.227 \bullet C_T \bullet f \bullet I_{ON}}{I_{ON} - 0.227 \bullet C_T \bullet f} \ . \qquad (15)$$

Finally, the R_{OFF} resistor value is

$$R_{OFF} = \frac{3.5}{I_{OFF}} \qquad (16)$$

These equations are used in a Mathcad spreadsheet listed in Appendix I [7].

Frequency Foldback Design:

The three resistors associated with frequency foldback may now be calculated. A useful approach is to first ignore the loading from the VOUT pin and ignore the R_{OUT3} connection. To allow for a small decrease in the output voltage before frequency foldback kicks in (this is not a requirement, but can be used to guarantee constant frequency operation under the expected output voltage ripple) set V_X = 4V and from Figure 6 one can write

$$V_X = 4 \approx \frac{R_{OUT1}}{R_{OUT1} + R_{OUT2}} \bullet V_O \qquad (17)$$

where V_O is the actual output voltage. By arbitrarily selecting R_{OUT1}, the value of R_{OUT2} can be determined. Now, the selection of R_{OUT3} determines the minimum frequency of operation. Rewriting equation 16 for the general case (when the VOUT pin is less than 3.5V)

$$V_X = R_{OFF} \bullet I_{OFF} \ . \qquad (18)$$

Setting V_O equal zero in equation 4 one solves

$$V_X = \frac{R_{OUT1} \| R_{OUT2}}{R_{OUT1} \| R_{OUT2} + R_{OUT3}} \bullet V_{REF} \qquad (19)$$

for R_{OUT3}. With R_{OUT1}, R_{OUT2}, and R_{OUT3} known, equation 4 can be used in a Mathcad spreadsheet to plot operating frequency of the converter as a function of the output voltage. Listed in Appendix I is an example of the spreadsheet which includes the calculations and graphs of the steady state volt-second clamp and frequency foldback characteristics.

Volt-Second Clamp Design:

The voltage at the VVS pin is given by

$$V_{VS} = \frac{R_{VS1}}{R_{VS1} + R_{VS2}} \bullet V_{IN} \qquad (20)$$

once R_{VS1} is selected R_{VS2} can be solved for after D_{VS} is chosen. From equation 6

$$V_{VS} = K \bullet \frac{D_{MAX}}{D_{VS}} \qquad (21)$$

as an example D_{VS} may be set to 110% of D_{OP}. For this case, after solving for R_{VS2} in equation 20 with V_{VS} replaced using equation 21, one finds

$$R_{VS2} = R_{VS1} \bullet \left(V_{IN} \bullet \frac{D_{OP}}{D_{MAX}} - 1\right) . \qquad (22)$$

Control Loop Component Calculations:

The concentration of this application note is to show the characteristics of the frequency foldback and volt-second clamp features of the UCC3884. Details of the small-signal modeling of the modulator and power circuit can be found in [8] and [9]. Integral compensation was used to set the crossover frequency to 9kHz with a gain of about 7dB needed at this frequency.

EXPERIMENTAL RESULTS

The RCD clamp forward converter was prototyped in the laboratory and relevant results are presented in the following section.

Frequency Foldback Data:

The primary current sense resistor in Figure 8 was increased to 32Ω from 16Ω (16Ω was used in the computer model that generated Figures 3 and 4) in order to limit the average load currents to reasonable values for easy measurement. The previous simulation results showed the basic phenomena of the current tail with and without frequency foldback. Due to effects not included in the computer model the experimental data differs from the simulated data. The computer model is a powerful tool to gain a fundamental understanding of the large signal VI characteristics as shown in Figures 3 and 4. It may be possible to take into account ignored complications so that the simulated results match

more closely the experimental data. It is thought that some of these effects could be the saturation of the magnetics (output inductor), errors in estimating the finite turn-off time of the MOSFET power stage switch and possible saturation of the primary current sense transformer. Despite these measurement inaccuracies the frequency foldback operation does reduce the current tail as compared to non-frequency foldback operation and this can be seen in the simulation results and the actual circuit measurement data.

Figure 9 shows normal operation at constant frequency with about a 4A average load current. The top waveform is the output voltage (5V, channel 3) followed by the oscillator waveform measured at

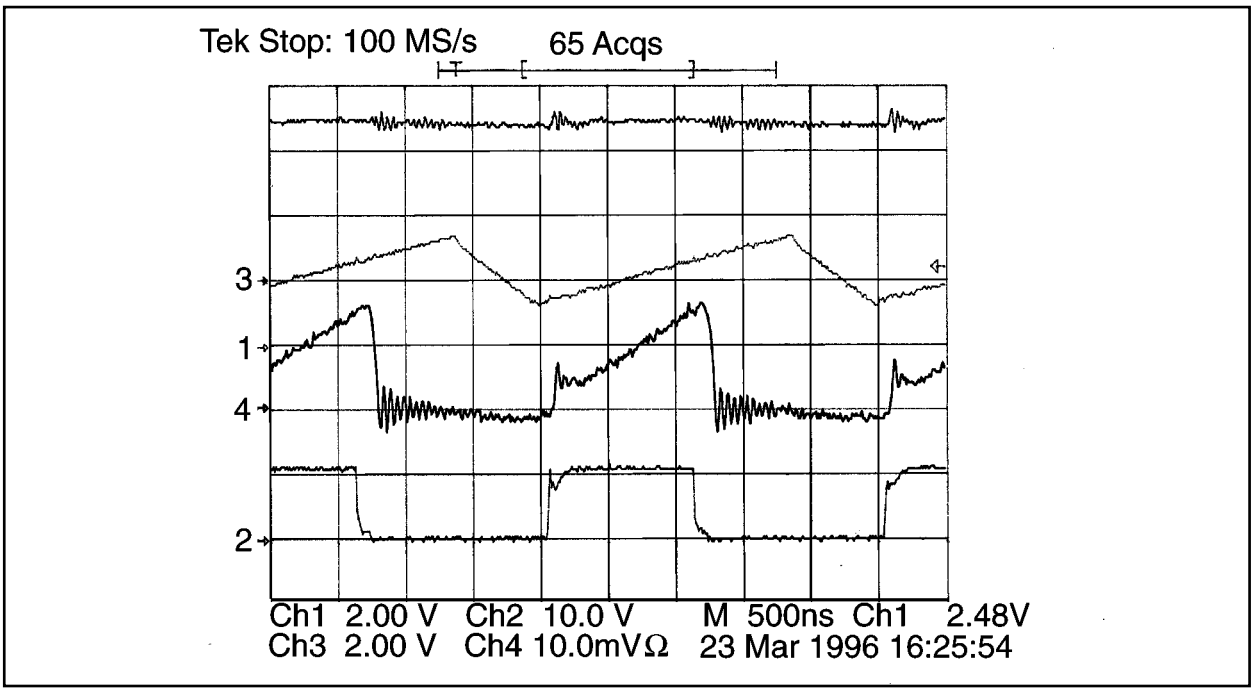

Figure 9. Converter Output Voltage, Oscillator Waveform, Primary Side Current During Normal Operation, and MOSFET Gate Voltage

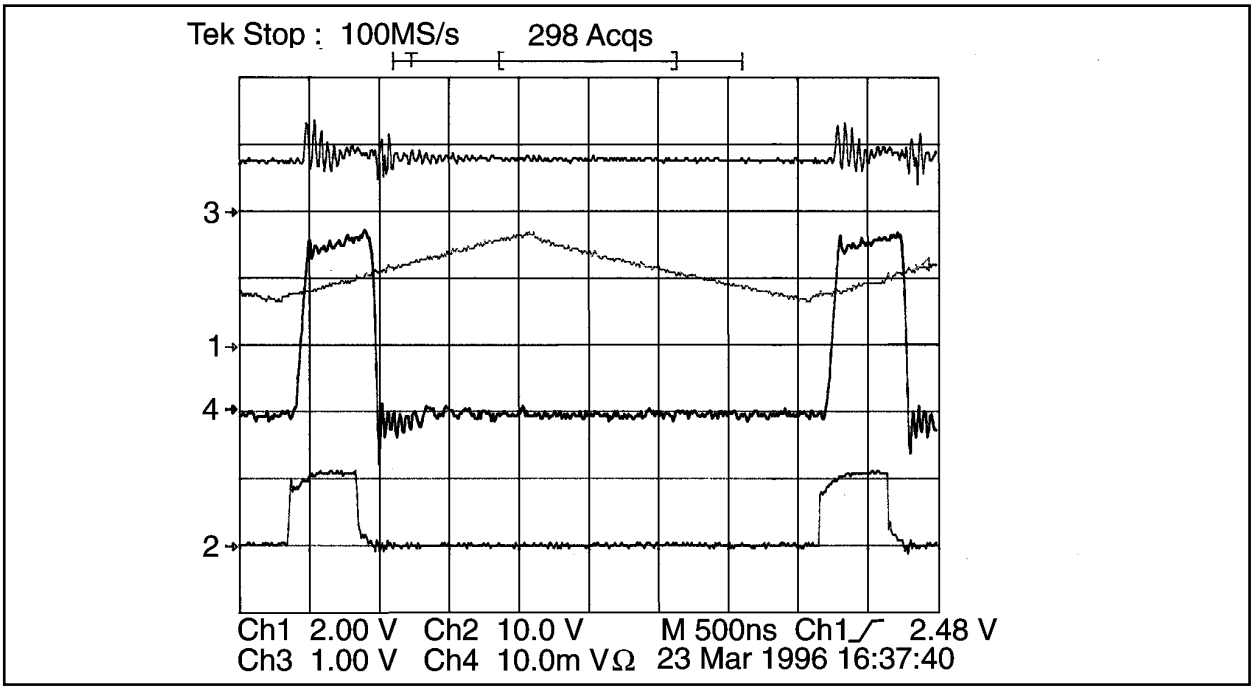

Figure 10. Converter Output Voltage, Oscillator Waveform, Primary Side Current During a Low Impedance Load Fault, and MOSFET Gate Voltage

pin 10 (CT, channel 1). Note that for small values of C_T the scope probe capacitance on pin 10 can decrease the frequency. The third from the top is the primary side current at 1A/div (channel 4). Note that there is a 470pF capacitor in parallel with the MOSFET primary switch to reduce clamp loss [2]. The bottom trace is the gate voltage at pin 8 (OUT, channel 2) which drives an IRF630 through a 13Ω resistor.

A low impedance load was applied and the resulting converter waveforms are shown in Figure 10 with the same scales as used in Figure 9 except the output voltage scale was decreased and the primary current scale on the AM503B was increased from 1A/div to 2A/div (channel 4). The average load current was 17.4A and the frequency was reduced from 403kHz to 267kHz. The output voltage decreased from 5.016V to 0.880V.

A toggle switch was used to change from frequency foldback to non-frequency foldback operation. This allowed direct comparison between frequency foldback and non-frequency foldback operation as the load resistance decreased. Figure 11 shows the data taken under the same conditions with and without frequency foldback. It was found that a fan was helpful in keeping the sense resistors cool in order to avoid drift during current measurement. The shape of the curves in Figure 11 differ from Figure 3, obviously the computer model has not taken into account all of the parasitic and saturation effects. The value of R_{OUT3} calculated in Appendix I was increased to 33.1k to generate the frequency foldback curve shown in Figure 11. The actual measured frequency versus output voltage is shown in Figure 12.

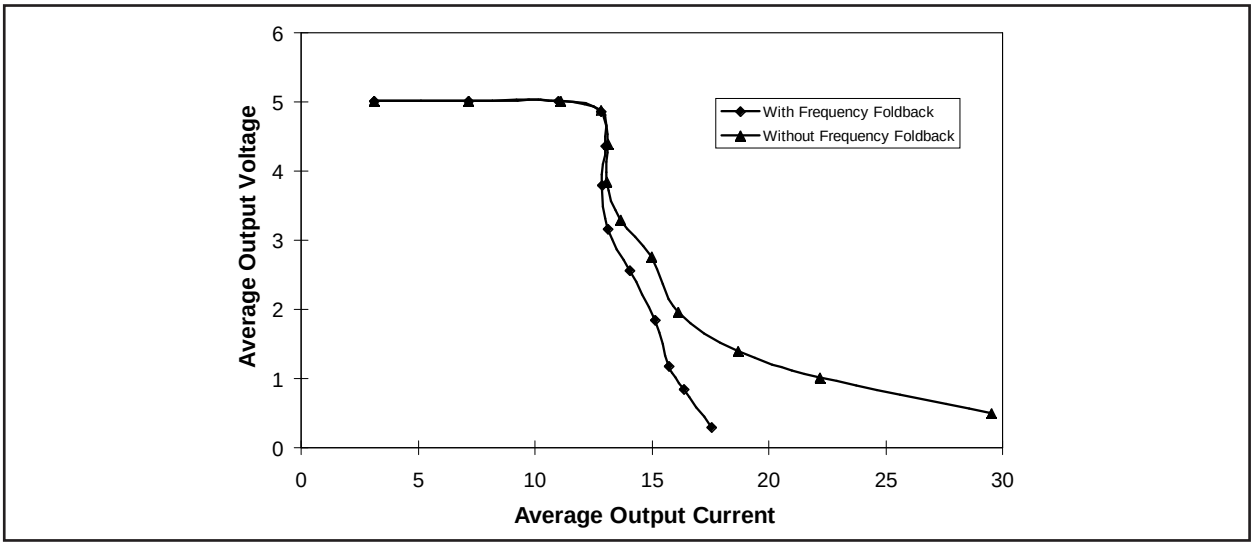

Figure 11. VI Characteristics with and without Frequency Foldback

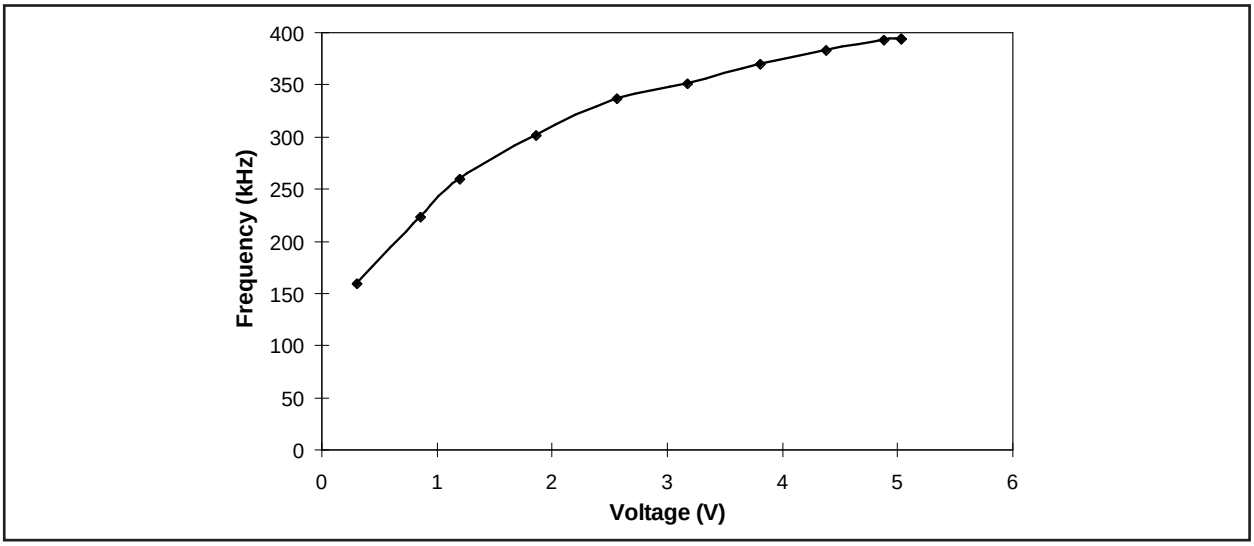

Figure 12. Measured Frequency versus Measured Output Voltage

SUMMARY

The UCC3884 peak current mode controller provides the designer a frequency foldback scheme to reduce the current tail often seen in high frequency buck derived converters. A possible practical design approach in the prototype circuit is to set the minimum frequency to about 1/3 of the nominal frequency and to use the simplified analysis outlined above to give first pass circuit values for the frequency foldback resistors R_{OUT1}, R_{OUT2}, and R_{OUT3}. During testing of the power converter low impedance loads can be applied for final adjustment of the frequency foldback resistors and to verify desired operation. The maximum duty-cycle clamp and volt-second clamp may be used to enhance performance and reliability of the power converter system. The undervoltage lockout, clock synchronization, depletion-mode MOSFET driver, and soft-start functions are all provided to complete a feature rich peak current mode controller within a 16 pin DIL package.

REFERENCES:

[1] Philip Cooke, “Analysis of a Voltage Controlled Frequency Foldback Technique that Improves Short Circuit Protection for Buck Derived Converters”, Intelec, October 1996, page 749-755.

[2] Leu, Hua, Lee, and Zhou, “Analysis and Design of RCD Clamp Forward Converter”, VPEC, Virginia Tech and Delta Power Electronics Lab, Blacksburg, VA.

[3] Bill Andreycak, “Active Clamp and Reset Technique Enhances Forward Converter Performance”, Unitrode Seminar SEM-1000, page 3-1.

[4] Clemente, Pelly, Ruttonsha, “A Universal 100kHz Power Supply Using a Single HEXFET”, International Rectifier Application Note 939A.

[5] Abraham I. Pressman, “Switching Power Supply Design”, McGraw-Hill, Inc. 1991.

[6] Larry Hayes, Warren Schultz, “Optoisolators for Switching Power Supplies”, Motorola Optoelectronics Device Data Book, DL118/D REV 4.

[7] Mathcad User’s Guide, Mathcad PLUS 6.0, Mathsoft Inc., 1995.

[8] Lloyd H. Dixon, “Control Loop Cookbook”, Unitrode Power Supply Design Seminar, SEM-1100, 1996.

[9] Ridley, Raymond B, “A New Small Signal Model For Current Mode Control”, Dissertation, November 27, 1990, VPEC, Blacksburg, VA.

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Appendix I: Oscillator and Volt-Second Calculations

High Performance UCC3884 PWM with Frequency Foldback and Volt-Second Clamp
Mathcad design worksheet. by Philip Cooke

Specifications:

Input Votage	35V<Vin<72V
Output voltage	5V dc
Operating frequency	400 kHz

$f := 400 \cdot 10^3$ Estimated operating frequency (for non-frequency foldback conditions).

$D\_max := 0.75$ Maximum duty-cycle.

$N := \frac{8}{2}$ Primary transformer turns ratio.

$Vt := 3.5$ Peak oscillator voltage.

$Vb := 1.5$ Minimum oscillator voltage.

$Vd := 0.5$ Estimated voltage drop on secondary forward diode.

$Kon := 8.8$ Ion multiplier to charge Ct.

$Koff := 8.8$ Ioff multiplier to discharge Ct.

$K := 1.1$ Volt-second constant.

$Vds\_on := 0.15$ Approximate voltage drop of primary switch.

$Vout := 5$ Output dc voltage.

$Vref := 5$ Output of on-board UCC3884 regulator.

$Vin\_min := 35$ Minimum input voltage.

$Vin\_max := 72$ Maximum input voltage.

Oscillator Calculations:

Calculate the timing capacitor from the frequency:

$Ct := \frac{1}{2 \cdot 10^4 \cdot f}$ which gives $Ct = 1.25 \cdot 10^{-10}$ select $Ct := 120 \cdot 10^{-12}$

Recalculate operating frequency, $f := \frac{1}{2 \cdot 10^4 \cdot Ct}$ so that $f = 4.167 \cdot 10^5$

The oscillator on time is given by equation 8 $Tosc\_on := \frac{D\_max}{f}$ $Tosc\_on = 1.8 \cdot 10^{-6}$

Now from equation 12, calculate Ion

$Ion := \frac{Ct}{4.4 \cdot Tosc\_on}$ so that $Ron := \frac{Vb}{Ion}$ $Ron = 9.9 \cdot 10^{4}$

Ioff is found from equation 15 $Ioff := \frac{0.2273 \cdot Ct \cdot f \cdot Ion}{Ion - 0.2273 \cdot Ct \cdot f}$ $Ioff = 4.548 \cdot 10^{-5}$

Finally, Roff is $Roff := \frac{Vt}{Ioff}$ $Roff = 7.696 \cdot 10^{4}$

Checking the Kon*Ion and Koff*Ioff values to be sure they don't exceed 800 mA:

$Kon \cdot Ion = 1.333 \cdot 10^{-4}$

$Koff \cdot Ioff = 4.002 \cdot 10^{-4}$

Frequency Foldback Calculations:

Set Rout1 to 4.99 kW. $Rout1 := 4.99 \cdot 10^{3}$

Rearranging equation 17 to solve for Rout2: $Rout2 := \frac{Rout1}{4} \cdot Vout - Rout1$ $Rout2 = 1.248 \cdot 10^{3}$

The minimum frequency is selected to be 1/3.3 of the nominal frequency; now Ioff minimum can be calculated from equation 15:

$$Ioff := \frac{0.2273 \cdot Ct \cdot \frac{f}{3.3} \cdot Ion}{Ion - 0.2273 \cdot Ct \cdot \frac{f}{3.3}} \qquad Ioff = 4.457 \cdot 10^{-6}$$

With Ioff equation 18 is used to find the minium value of Vx

$$Vx := Roff \cdot Ioff$$

With $Vx = 0.343$ V Rout3 is given by (equation 19):

$$Rout3 := \frac{Rout1 \cdot Rout2}{Rout1 + Rout2} \cdot \left(\frac{Vref}{Vx} - 1 \right) \qquad Rout3 = 1.355 \cdot 10^{4}$$

Volt-Second Calculations:

Choose 10 kW for Rvs1 and set D_vs = 1.467*D_max; $Rvs1 := 10 \cdot 10^3$

Calculate the operating duty-cycle at Vin_min. $Dop := \frac{Vout + Vd}{(Vin\_min - Vds\_on) \cdot \frac{1}{N}}$

From equation 22 $Rvs2 := Rvs1 \cdot \left(\frac{Vin\_min \cdot Dop}{D\_max} - 1 \right)$ $Rvs2 = 2.846 \cdot 10^5$

Final Selection of Components:

$Rout1 := 4.99 \cdot 10^3$ $Rout2 := 2.00 \cdot 10^3$ $Ron := 100 \cdot 10^3$ $Roff := 76.8 \cdot 10^3$

$Rout3 := 13.7 \cdot 10^3$ $Ct := 120 \cdot 10^{-12}$ $Rvs1 := 10 \cdot 10^3$ $Rvs2 := 287 \cdot 10^3$

Recalculate Ion, Ioff, f, Tosc_on, and Tosc_off:

$Ion := \frac{Vb}{Ron}$ $Ion = 1.5 \cdot 10^{-5}$ $Kon \cdot Ion = 1.32 \cdot 10^{-4}$

$Ioff := \frac{Vt}{Roff}$ $Ioff = 4.557 \cdot 10^{-5}$ $Koff \cdot Ioff = 4.01 \cdot 10^{-4}$

$f := \frac{1}{2 \cdot 10^4 \cdot Ct}$ $f = 4.167 \cdot 10^5$

$Tosc\_on := \frac{Ct}{4.4 \cdot Ion}$ $Tosc\_on = 1.818 \cdot 10^{-6}$

$Tosc\_off := \frac{1}{f} - Tosc\_on$ $Tosc\_off = 5.818 \cdot 10^{-7}$

Derive Equations to Plot:

$i := 0, 1 .. 100$ Set up a range variable.

$Vin_i := Vin\_min + \left(\frac{Vin\_max - Vin\_min}{100} \right) \cdot i$ Use i as a parameter to vary Vin.

$$Vo_i := Vout \cdot \left(1 - \frac{i}{100}\right)$$

Vary Vo parametry with i.

$$D\_op_i := \frac{Vout + Vd}{\left(Vin_i - Vds\_on\right) \cdot \frac{1}{N}}$$

Calculate the steady state operating duty-cycle as a function of input voltage.

The Vx voltage is calculated assuming no clamp or load of the VOUT pin:

$$Vx_i := \frac{\frac{Rout1 \cdot Rout3}{Rout1 + Rout3}}{\left(\frac{Rout1 \cdot Rout3}{Rout1 + Rout3} + Rout2\right)} \cdot Vo_i + \frac{\frac{Rout1 \cdot Rout2}{Rout1 + Rout2}}{\left(\frac{Rout1 \cdot Rout2}{Rout1 + Rout2} + Rout3\right)} \cdot Vref$$

Next, the 3.5V limit is taking care of by the Mathcad conditional if statement:

$$Vout_i := if\left(Vx_i > 3.5, 3.5, Vx_i\right)$$

Now the Ct discharge current, Tosc_off, and f can be found as a function of Vout;

$$Ioff_i := \frac{Vout_i}{Roff} \qquad Tosc\_off_i := \frac{(Vt - Vb) \cdot Ct}{Koff \cdot Ioff_i} \qquad f_i := \frac{1}{Tosc\_on + Tosc\_off_i}$$

A temporary variable is used to calculate the voltage at the VVS pin as the input voltage varies. Stop gaps of 0.6V and 4.5V are assumed.

$$Vtemp_i := \frac{Rvs1}{Rvs1 + Rvs2} \cdot Vin_i$$

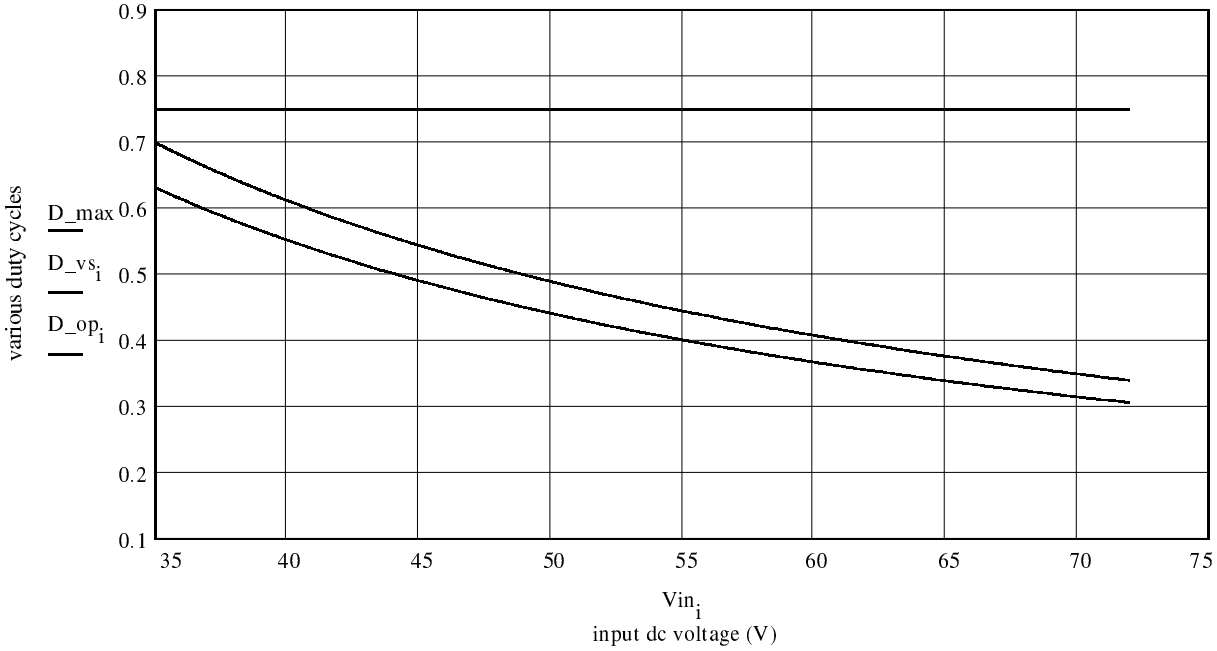
$$Vvs_i := if\left(Vtemp_i < 0.6, 0.6, if\left(Vtemp_i > 4.5, 4.5, Vtemp_i\right)\right)$$

Finally, the effective volt-second duty-cycle clamp is calculated;

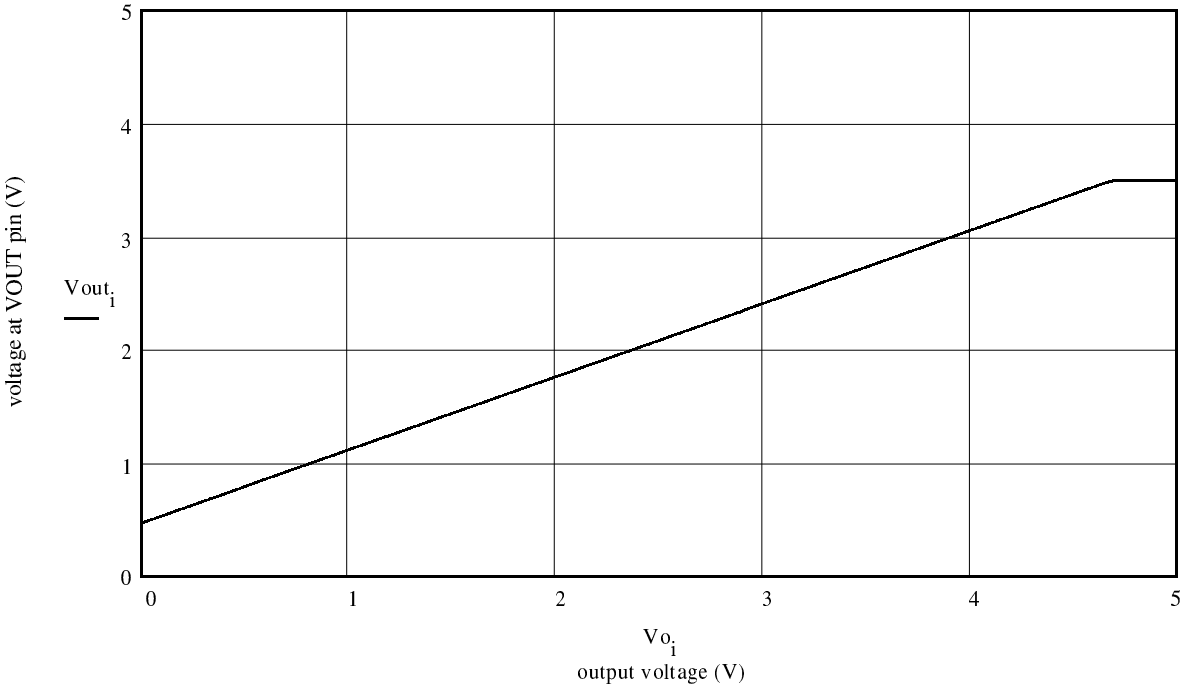
$$D\_vs_i := K \cdot \frac{D\_max}{Vvs_i}$$

Plot Expected Results:

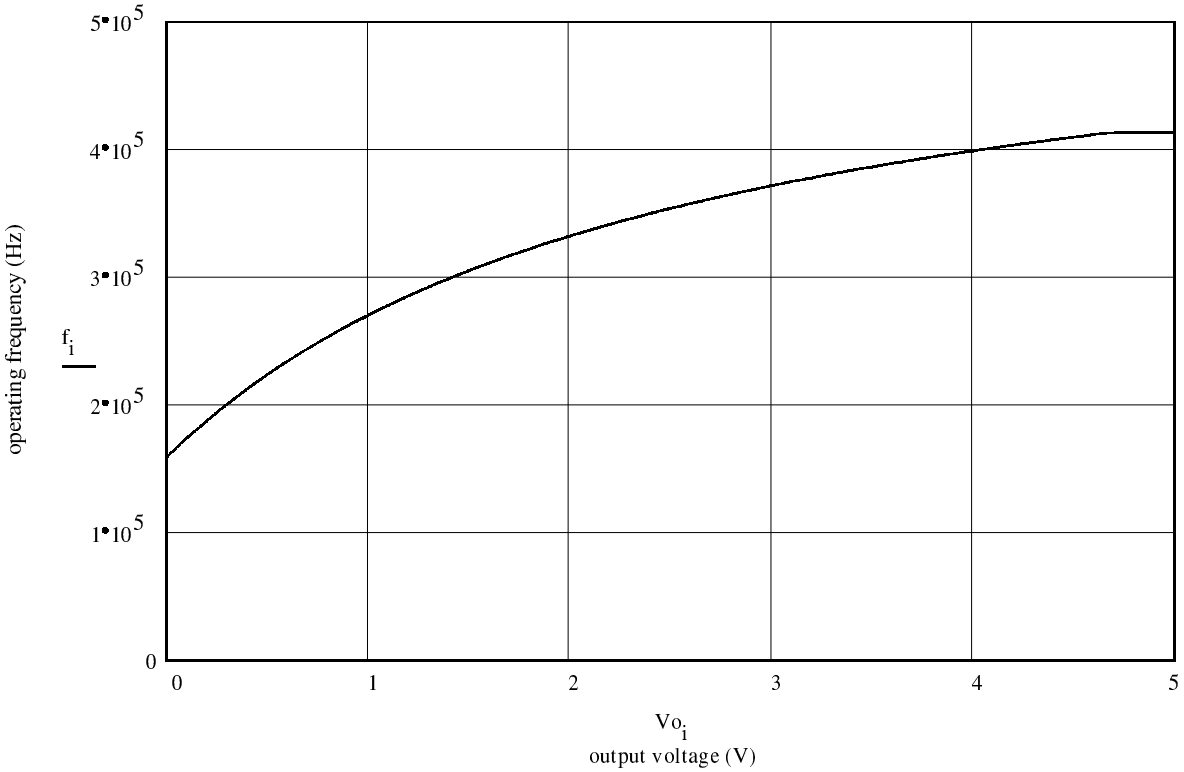
Waveforms from top to bottom; maximum duty cycle, volt-second clamp, and operating duty cycle



Voltage at the VOUT pin as the actual output voltage varies.



Frequency foldback characteristics: as the output voltage decreases the converters operating frequency decreases.



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