Application Report
SLUA737B–March 2015–Revised October 2015

Using UCD7138 and UCD3138A for Advanced Synchronous Rectification Control

ABSTRACT

The UCD7138 low-side MOSFET driver is a high-performance driver for secondary-side synchronous rectification (SR), with body-diode conduction sensing. The device is suitable for high-power, high-efficiency, isolated-converter applications requiring dead-time optimization. The UCD7138 gate driver is a companion device to the UCD3138A, a highly-integrated digital controller for isolated power. The UCD3138A has an advanced dead time control interface which accepts UCD7138 output signals and optimizes SR gate driver signals accordingly. This application report provides the setup guide for advanced synchronous rectification control of the two devices. The hardware connection, layout example, and firmware example are provided.

Topic **Page**

1 Introduction

The state-of-the-art, LLC-resonant converter SR driving strategies fall in two categories: the first is the MOSFET Rdson voltage-drop sensing-based method; the other is the SR-pulse width-clamp method, which is usually used in digitally-controlled LLC converters.

In the first method, the MOSFET is turned on after a large negative voltage on the MOSFET body diode is detected on the MOSFET drain terminal. The MOSFET is turned off when the voltage drop on the MOSFET Rdson rises above a small negative voltage. Some commercial products in this category also try to vary the gate drive voltage to enable fast turnoff. This method requires turnon and turnoff blanking times, does not require a gate driver input, and works for both analog and digital solutions. One of the drawbacks of this method is that the voltage drop on Rdson is too small to detect, and varies with layout parasitic and the type of MOSFETs used. Also, in high-current applications with several MOSFETs in parallel, the Rdson is so small that the MOSFETs are turned off when the current is still large.

In the second method, the SR gate drive signal comes from the digital controller. The turn-on edge is usually fixed. The turn-off edge changes based on operation modes. When above or equal to resonant frequency, the turn-off edge varies based on the switching frequency, and keeps a fixed dead time relative to the primary-side gate drive signal. When below resonant frequency, the SR pulse width is clamped to half of the resonant period, minus some dead time. This method is easy to implement with digital power controllers. The drawback is that this method requires resonant tank information for programming the pulse width clamp value, and thus requires calibration in production.

Table 1. State of the Art LLC SR Control Methods

Method	Advantages	Disadvantages
Rdson voltage drop sensing	Does not require gate drive signal input	Not suitable for high current applications with several MOSFETs in parallel Layout parasitic concern
SR pulse width clamp	Digital controller friendly Simple system configuration	Requires calibration in production No SR turn-on edge optimization

To overcome the previously mentioned drawbacks of the existing solutions, a novel body-diode conduction time, sensing-based adaptive SR control method is proposed and implemented in UCD7138 and UCD3138A. The drain-to-source voltage on the MOSFET Rdson can vary with package, layout parasitic, and load current. However, when the body diode conducts, the voltage drop on the body diode is relatively constant, regardless of parasitic and load conditions. The UCD7138 gate driver senses the body diode conduction of the SR and reports to UCD3138A. UCD3138A then uses this information to adjust SR on time for the next cycle. A configurable body-diode conduction detection window is introduced in UCD3138A to determine whether the SR on time is too long or too short. The body-diode conduction time can be regulated to a desired length. A negative current prevention mechanism is also included to improve system reliability. In addition, UCD7138 can optimize the SR turn on edge timing. Compared with a conventional solution, the benefits of the proposed method are:

- Achieves high efficiency in a wider load range
- Automatically compensates for power stage component parameter variations; no calibration is required
- Large signal detection, easy layout, no parasitic concern
- No minimum on or off time, or blanking time constraints
- Better noise immunity compared with competitive solutions
- Good performance for both low-current applications and high-current applications with MOSFETs in parallel

1.1 Optimal SR Operation

The optimal SR operation is as follows. At below or equal to resonant frequency, the SR turn-on edge follows closely to the primary-side turn-on edge; the SR turn-off edge is determined by approximately half of the resonant period. At above resonant frequency, the SR turn-on edge is delayed, compared with the primary-side turn-off edge; the SR pulse width is always equal to approximately half of the switching period, thus the turn-off edge of the SR can pass that of the primary side.

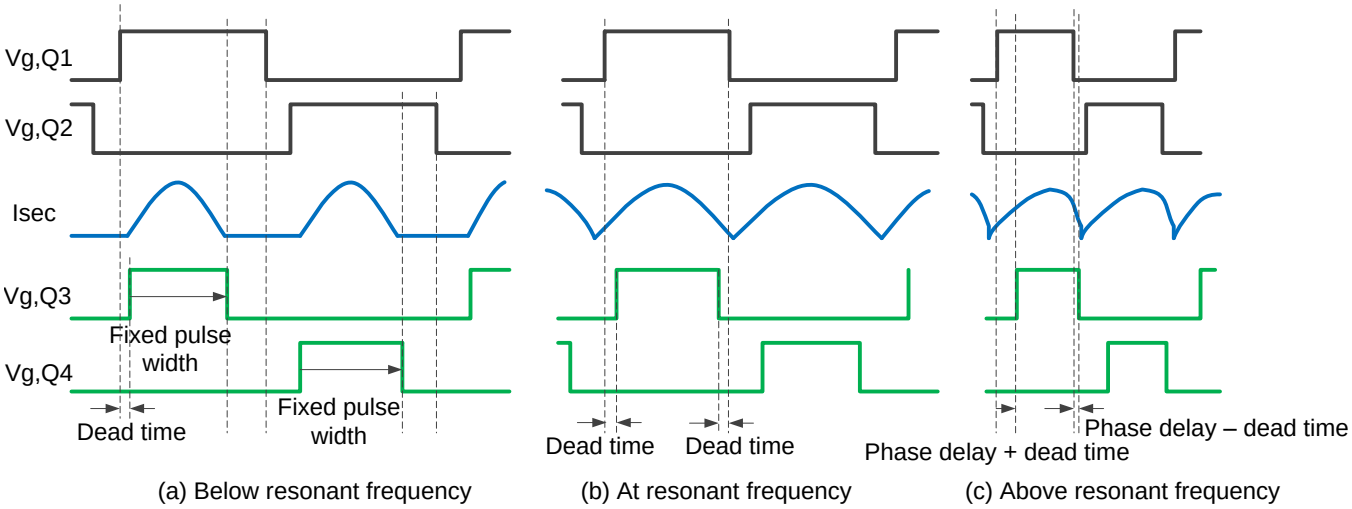


Figure 1. Optimal SR Operations

1.2 Body-Diode Conduction Detection

The body-diode conduction detector is a comparator with a –150 mV threshold. Comparator output is blanked when SR is on. Comparator output is active low when body-diode conduction is detected. When SR gate drive is high, the comparator output is blanked and always high to improve noise immunity.

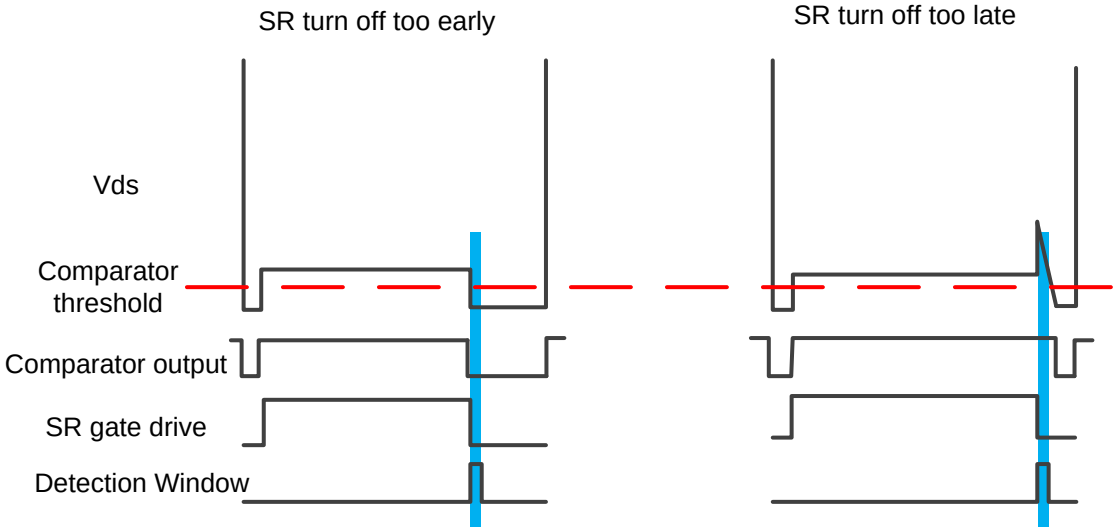


Figure 2. Body-Diode Conduction Detection

Figure 2 shows that in two cases the body diode of the SR MOSFET conducts:

1. MOSFET turns off too early, positive current flow, body diode conducts immediately after SR turning off
2. MOSFET turns off too late, negative current flow, drain to source voltage shoot-up first, then body diode conducts.

In two cases, SR on time should be adjusted in different directions, using a detection window generated for this purpose. The detection window starts right after the SR gate drive turns off; the length of the detection window is configurable, based on the delay in the circuit.

If, during the detection window, there is comparator low detected, the window indicates that the SR turns off too early. If, during the detection window, there is no comparator low detected, it indicates that the SR turns off too late.

1.3 Turn-On and Turn-Off Edge Optimization

In the proposed method, the SR gate drive signal is determined by both the primary-side gate-drive signal, and the body-diode conduction-detector output. The digital controller outputs a calculated SR-gate drive signal IN, based on the primary side pulse width, switching frequency, and the body-diode conduction time of the previous period.

The actual gate turning on is controlled by both the digital controller output IN and body-diode conduction-detector output DTC. OUT is the resulting digital controller SR-gate drive output. The OUT can only be turned on when IN is high. If DTC is already low at IN rising edge, turn on the gate driver output immediately; if DTC is still high at IN rising edge, turn on the gate driver output as soon as the DTC falling edge is received.

The gate turn-off edge is determined by IN only. The gate is turned off immediately at the IN falling edge.

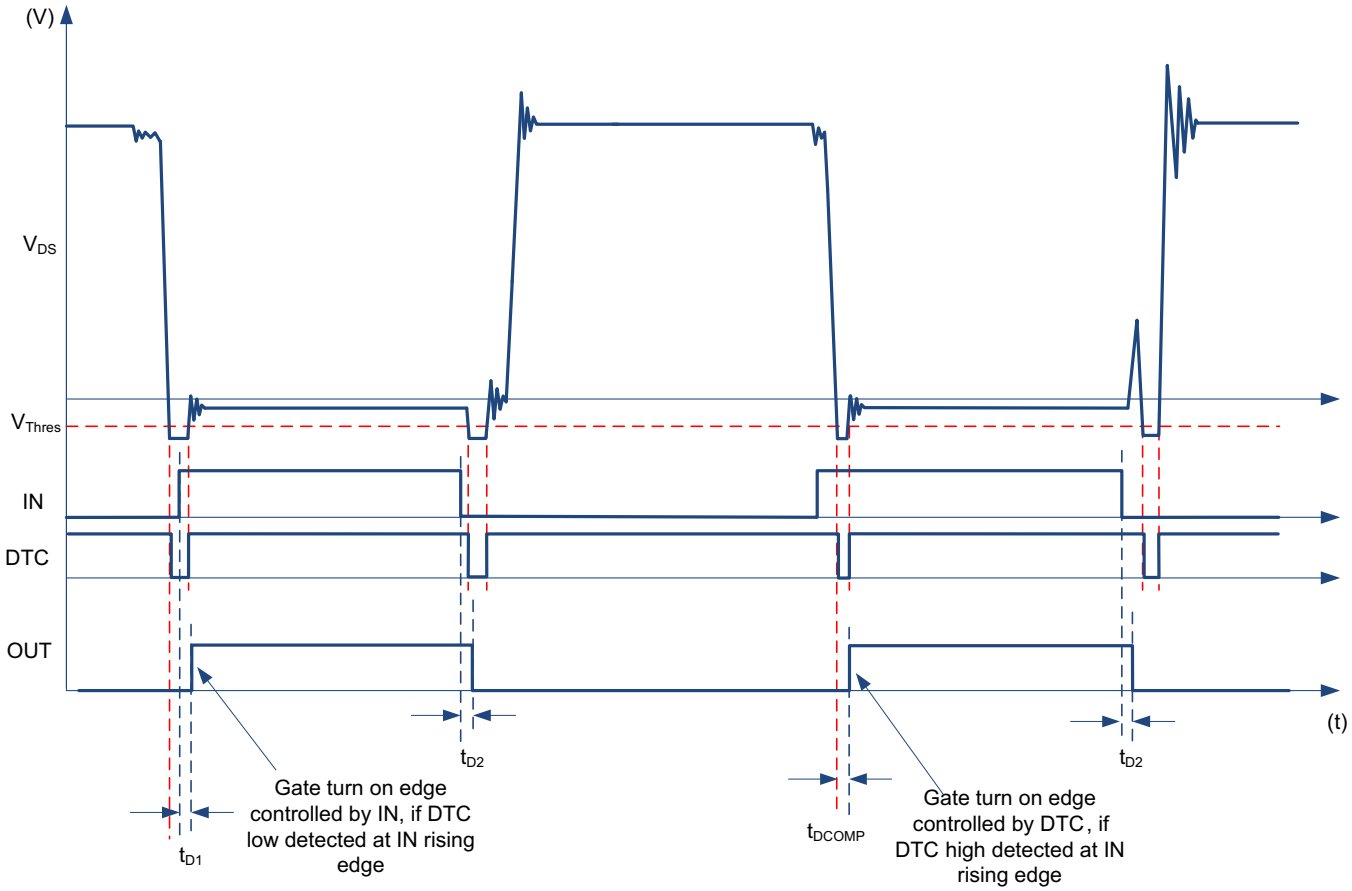


Figure 3. Turn-On Edge Optimization

The turn-on edge optimization is illustrated in Figure 3. The turn-off edge optimization is explained by Figure 2. During the detection window, the digital controller counts the DTC low time, and thus calculates the body-diode conduction time. If the time is too long, the digital controller increases the SR on time in the next cycle. If the time is too short, the digital controller reduces the SR on time in the next cycle.

1.4 Negative Current Prevention

As shown in Figure 4, when the SR pulse is on for too long, the drain-to-source voltage rises up.

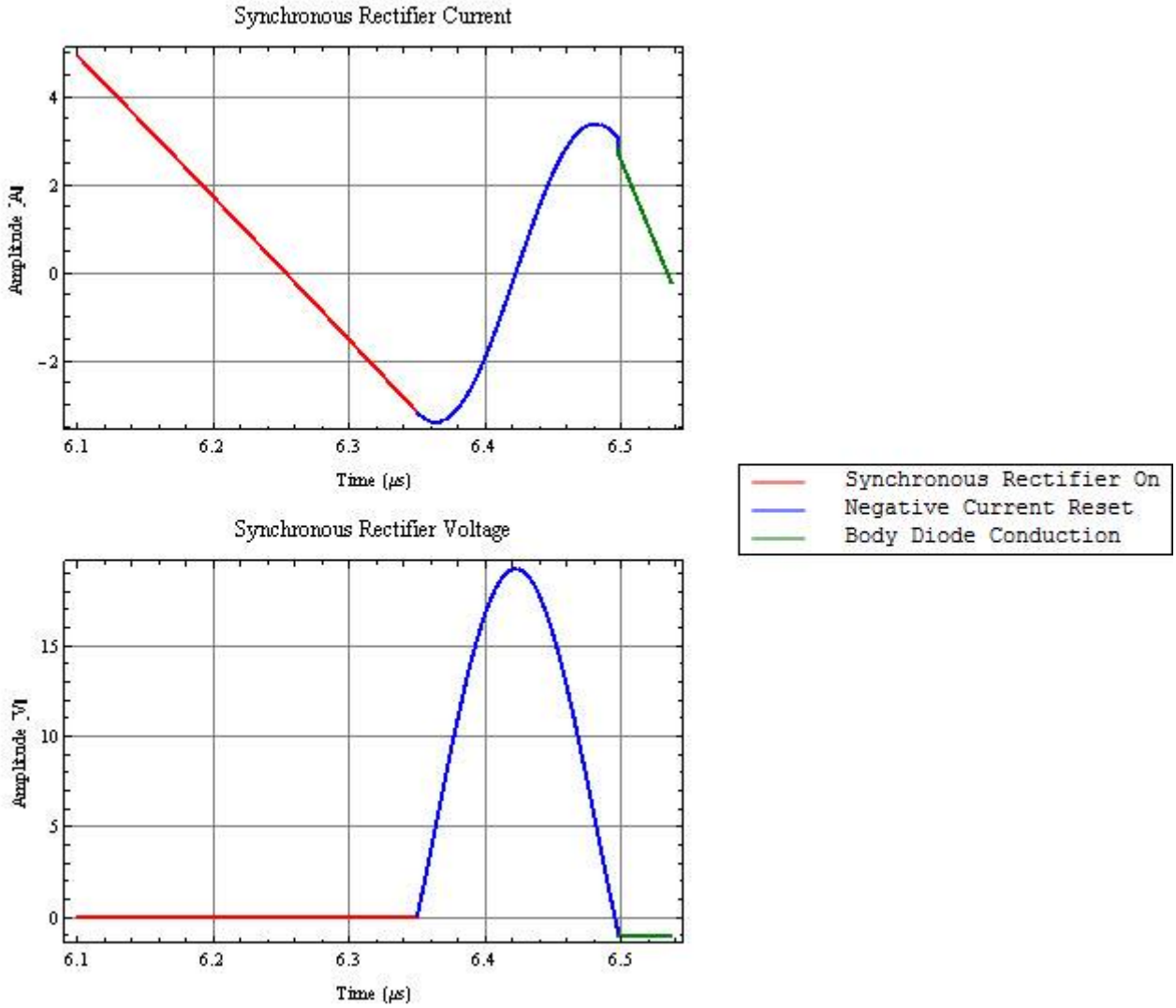


Figure 4. LLC Converter SR Drain to Source Voltage Shoot Up when there is Negative Current Flow

There are two ways to detect this situation: to set a positive threshold to detect the Vds shoot up, or to use the same detection window and body-diode conduction detector as described in the previous section. When there is no body-diode conduction during the detection window, negative current may have occurred, and the digital controller protects the system from damage. When the body diode conduction time sensed during the detection window is less than a certain threshold, UCD3138A will treat it as a fault and reduce the SR on time by a large pre-programmed amount. An interrupt can be generated, too.

2 Hardware Connection

Figure 5 shows a simplified hardware connection diagram.

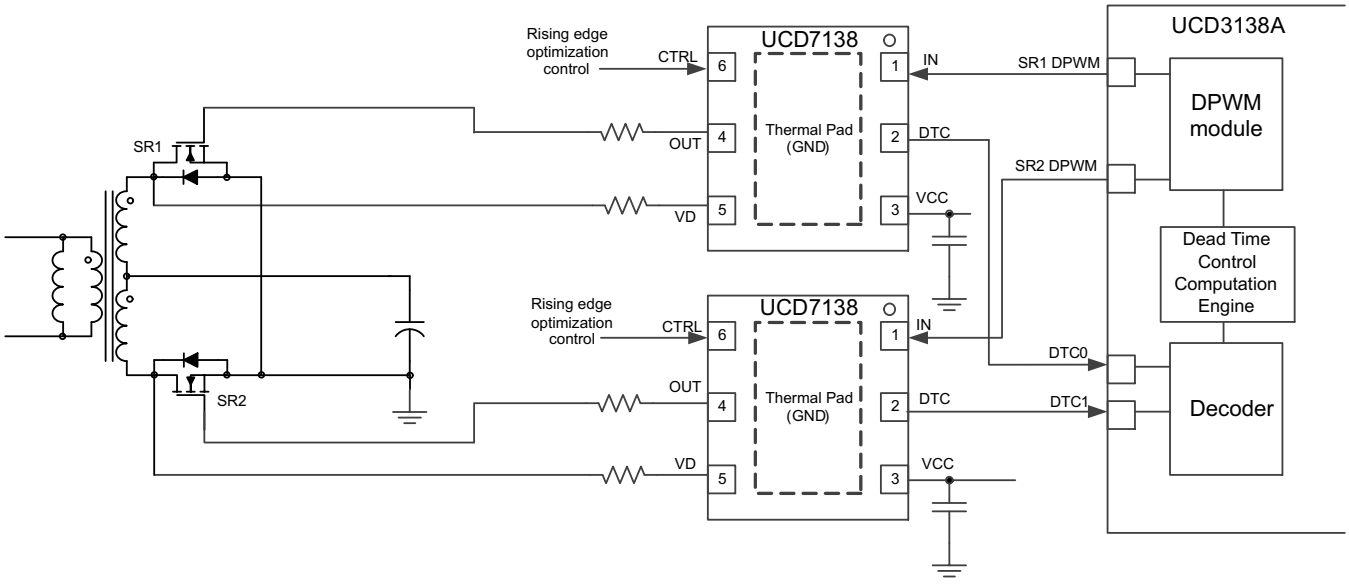


Figure 5. UCD7138 and UCD3138A Hardware Connection

Table 2. Terminal Function and Connection Description

Terminal		Type	Description
Name	No.		
IN	1	I	**Input**: Gate driver input. This pin should be connected directly to one of the UCD3138A DPWM outputs.
DTC	2	O	**Body diode conduction time report**: Standard digital I/O. Pulled high internally. Output low when body diode conducts. This pin should be connected to the DTC0 or DTC1 pin on UCD3138A. Some noise filtering may be needed on this pin at the UCD3138A side.
VCC	3	P	**IC supply**: External bias supply input. Supply range 4.5 V to 18 V. A ceramic bypass capacitor of at least 1 uF should be connected between VCC pin and the GND pad as close as possible.
OUT	4	O	**Gate driver output**: Integrated push-pull gate driver for one or more external power MOSFETs. Typical 4-A source and 6-A sink capability. Output voltage is rail-to-rail with VCC. This pin should be connected to the gate terminal of the SR MOSFETs.
VD	5	I	**Drain voltage**: Connect this pin as close as possible to the controlled MOSFET drain pad. This pin is connected to the diode conduction detection comparators internally. The comparator has a –0.15 V threshold to detect body-diode conduction. A 20-Ω resistor should be connected between VD pin and MOSFET drain terminal to limit the current.
CTRL	6	I	**Rising-edge optimization control**: Connect this pin to ground to disable rising-edge optimization; leave this pin floating or connect to logic high to enable rising-edge optimization.
GND	7	G	**Power Pad/GND:** The exposed pad on the bottom of the package enhances the thermal performance of the device. This pad is device ground reference.

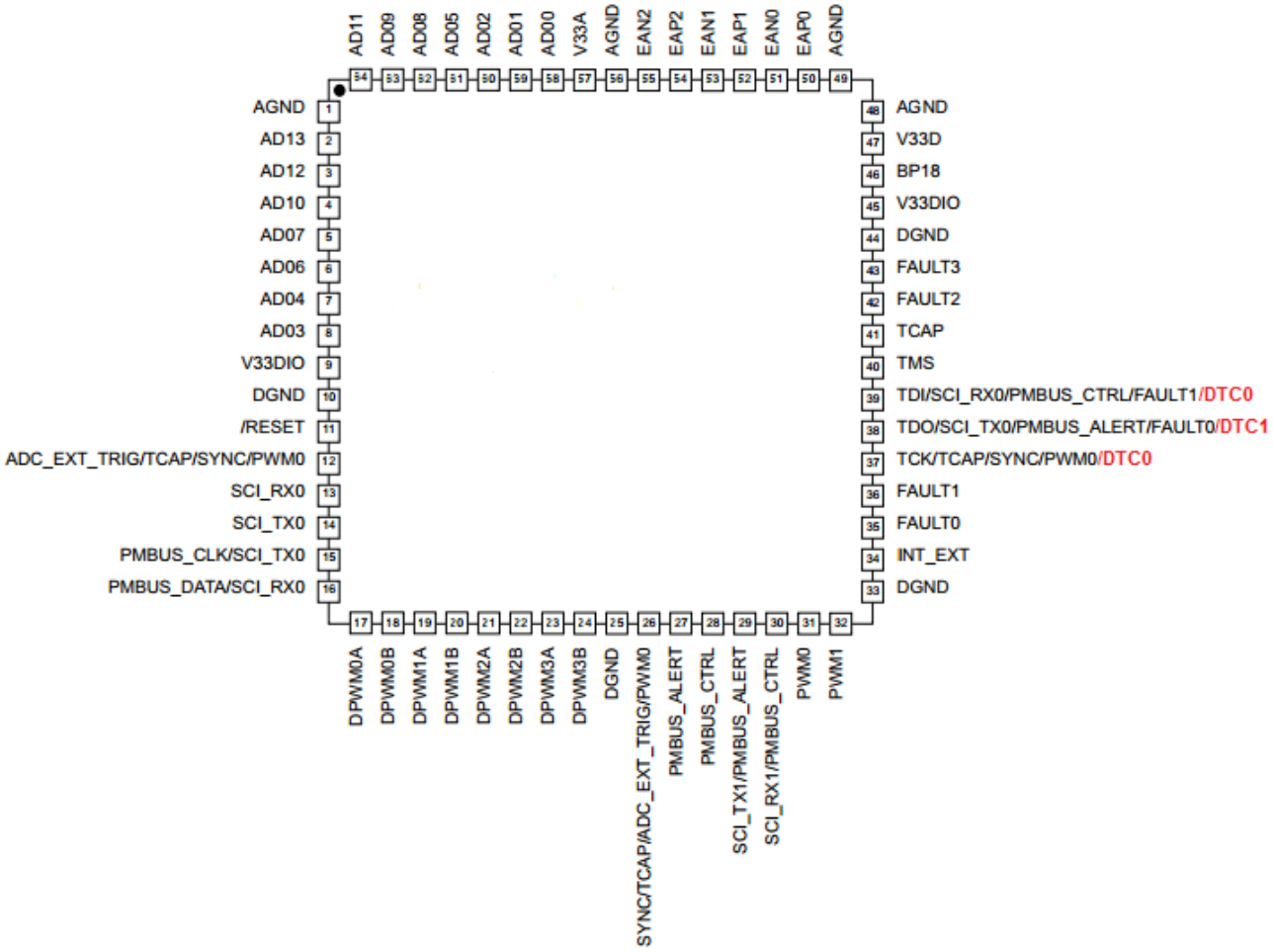


Figure 6. UCD3138A RGC Package Pin Out

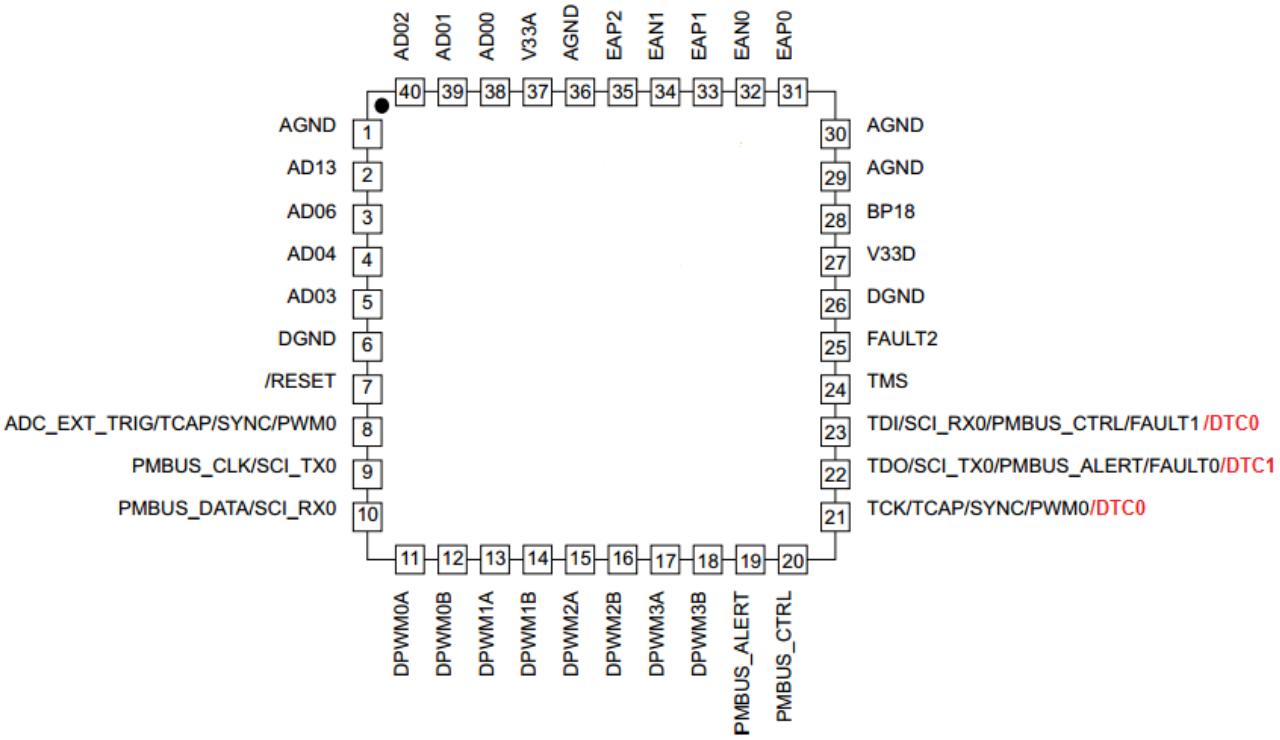


Figure 7. UCD3138A RMH Package Pin Out

3 UCD7138 Layout Example

3.1 LLC Layout Example

Figure 8 and Figure 9 show an LLC layout example where a 40-V leaded MOSFET is used for synchronous rectification.

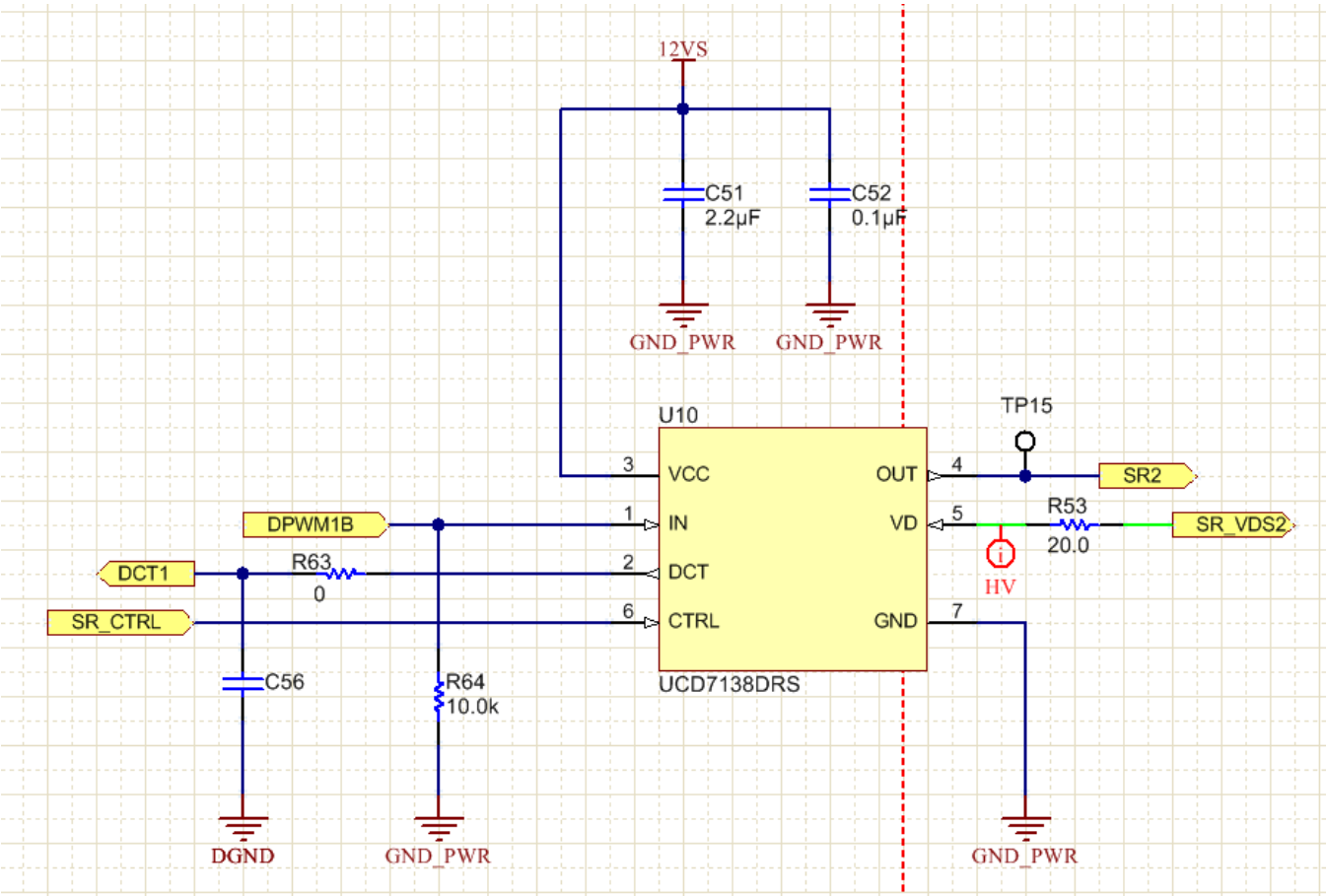


Figure 8. LLC Schematic Example

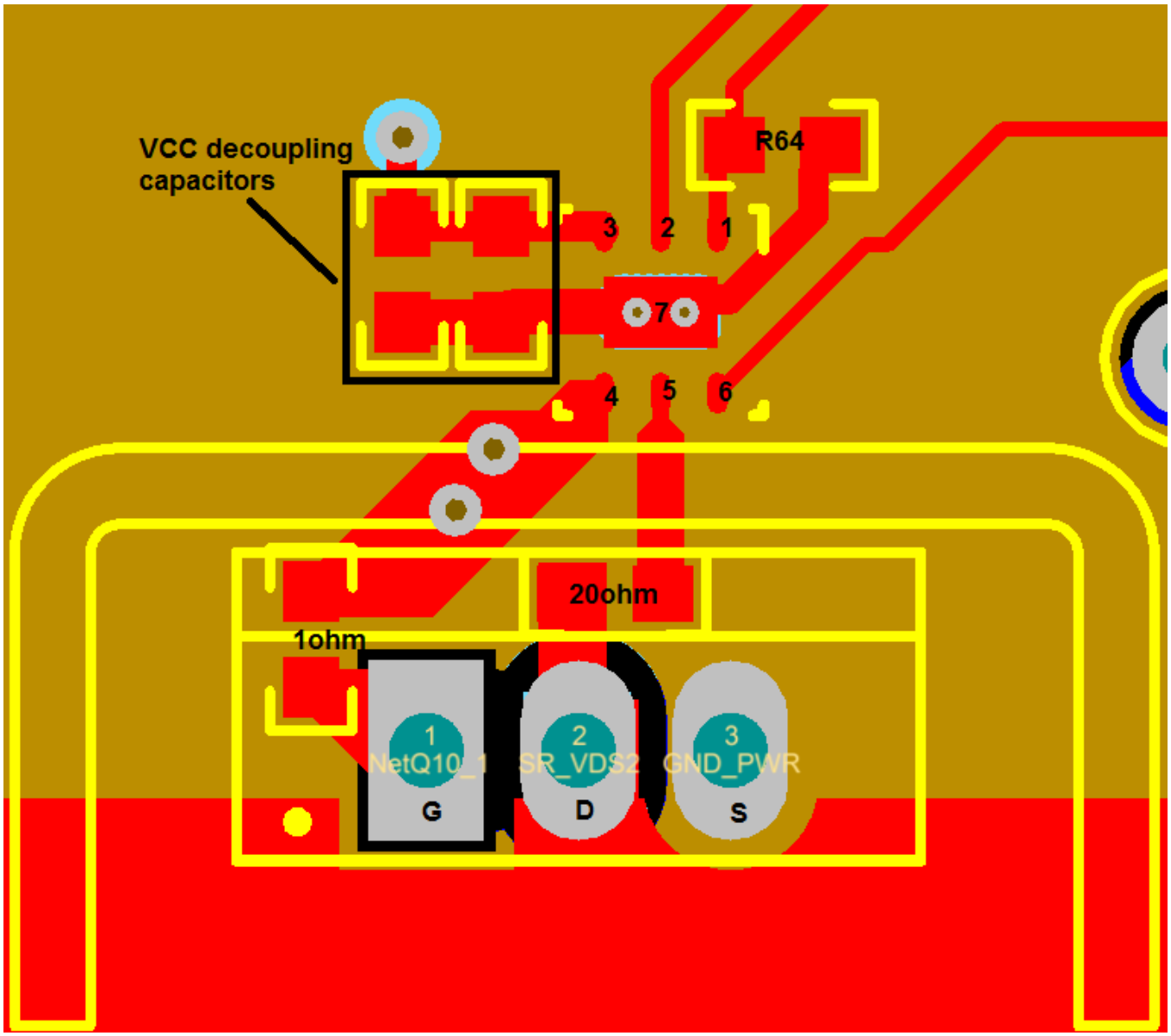


Figure 9. LLC Layout Example

3.2 Hard-Switched Full Bridge (HSFB) Layout Example

Figure 10 and Figure 11 show a HSFB schematic and layout example where an external high-voltage blocking MOSFET in a SOT-23 package is used to extend the VD pin voltage tolerance to 100 V.

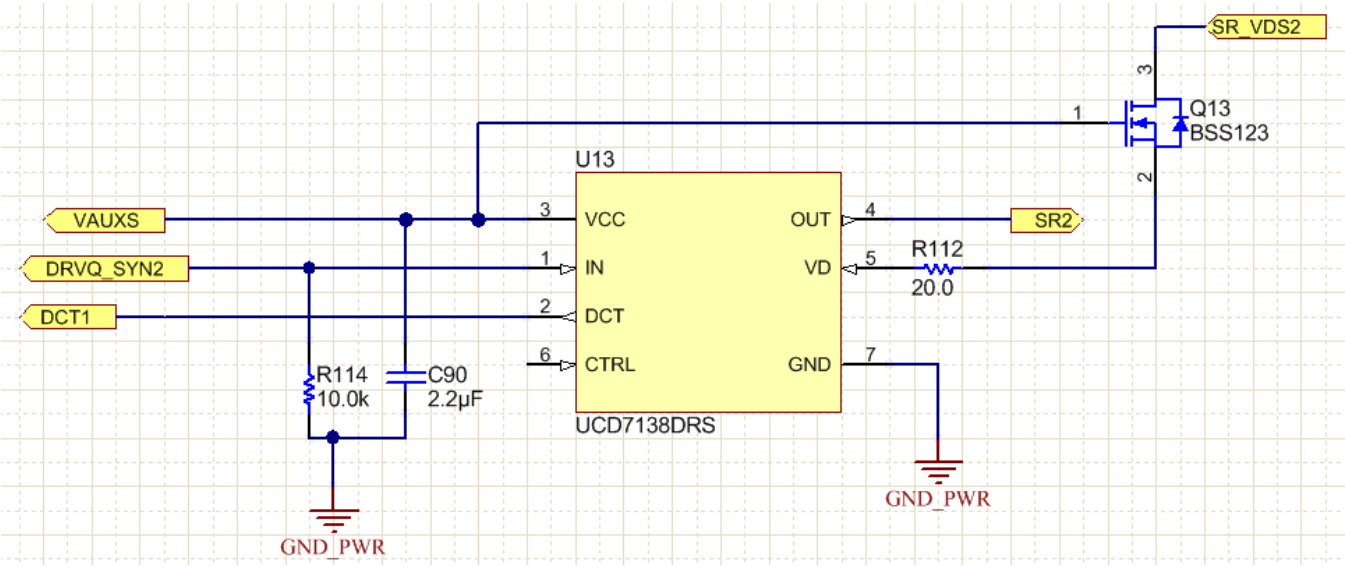


Figure 10. HSFB Schematic Example

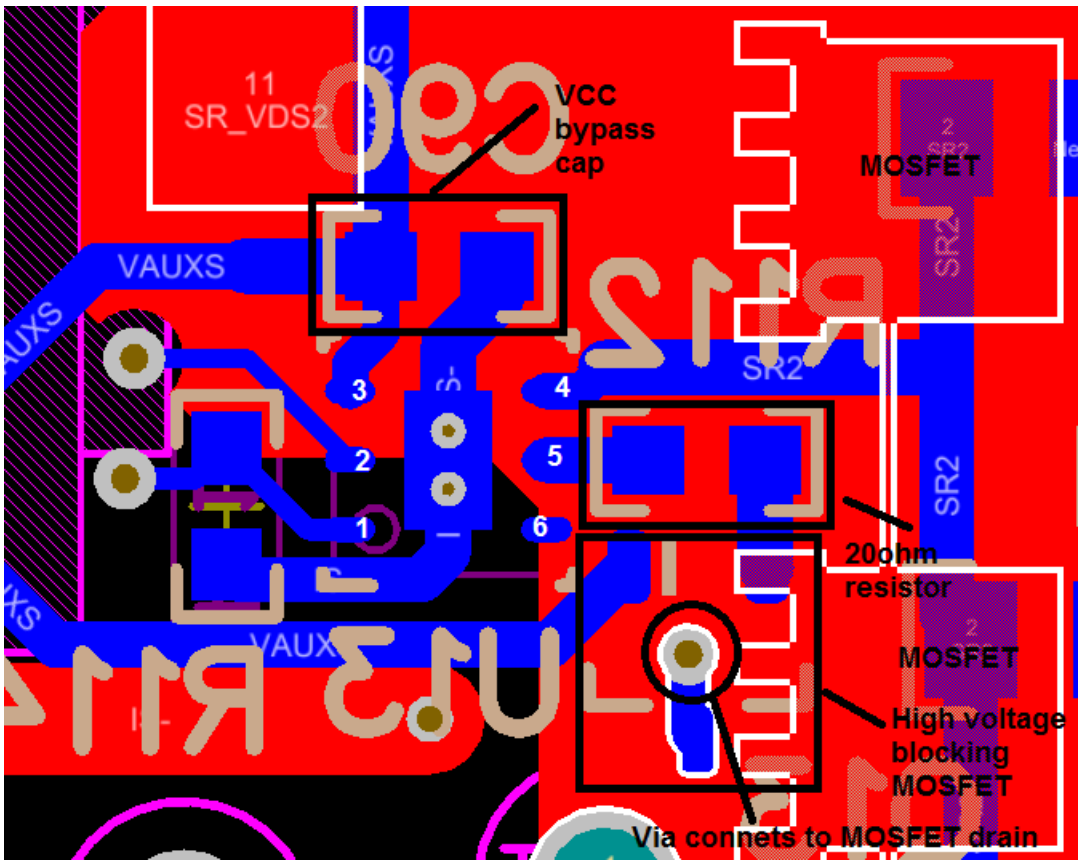


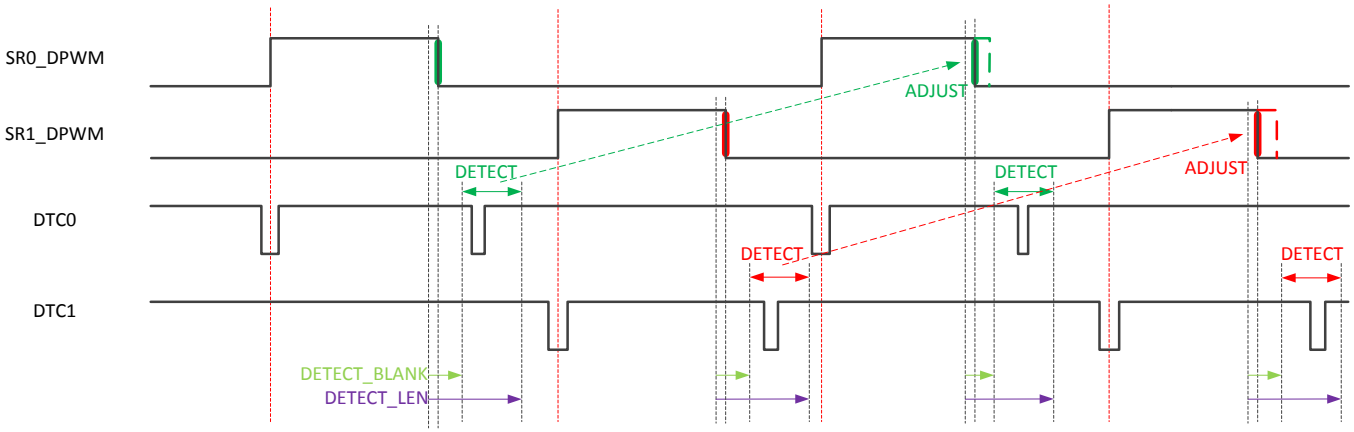
Figure 11. HSFB Layout Example

4 UCD3138A Dead Time Compensation (DTC) Interface

4.1 Overview

UCD7138 and UCD3138A can work together to optimize both the turn-on edge and turn-off edge of the synchronous rectifiers. The turn-on edge optimization is handled by the UCD7138 gate driver. For details about turn-on edge optimization, refer to UCD7138 datasheet (SLVSCS1). The turn-off edge optimization is handled by UCD3138A. Figure 12 is the timing diagram.

DTC0 and DTC1 are received body-diode conduction inputs from UCD7138. SR0_DPWM and SR1_DPWM are the DPWM waveforms for the SRs. The yellow and green edges are moving edges controlled by both the filter output and the DTC interface. In each cycle, a body-diode conduction time detection window is generated after the falling edge of the SR DPWM waveform. The detection window is defined by both DETECT_BLANK and DETECT_LEN registers. During this detection window, a 4-ns timer capture counts how long the body diode conducts. The SR DPWM turn-off edge of the next cycle is then adjusted accordingly.



*** Note: DETECT_BLANK and DETECT_LEN starts 1MCLK (32ns) before the falling edge of SR0_DPWM or SR1_DPWM**

Figure 12. Timing Diagram of the DTC Interface

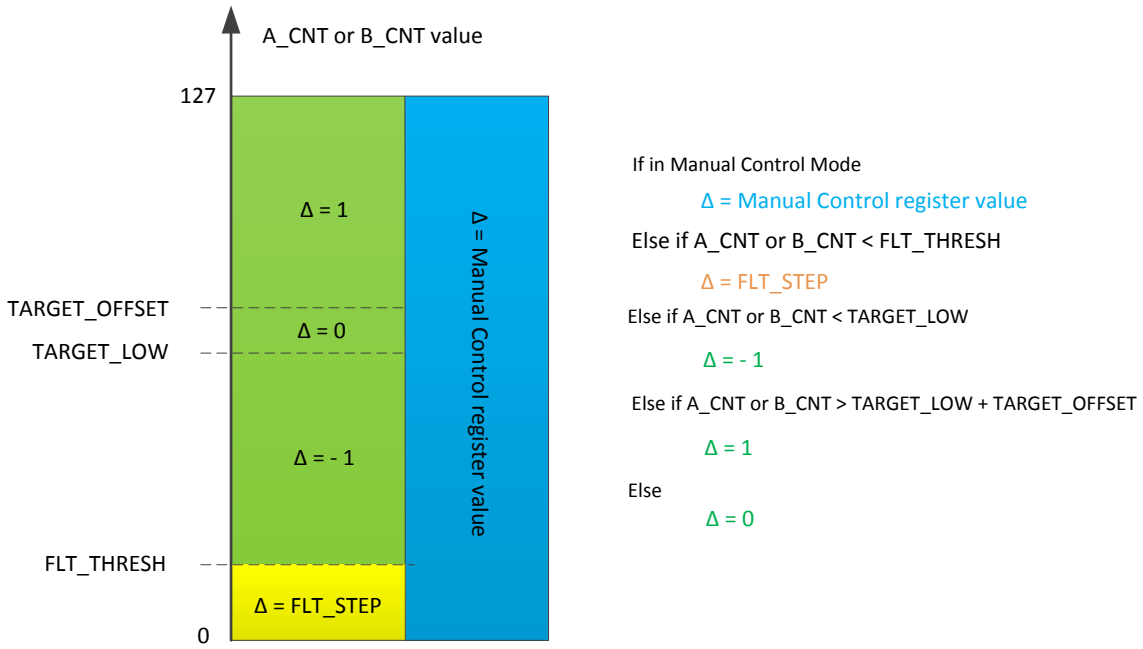


Figure 13. DTC Interface Principle

Figure 13 shows the turn-off edge adjustment based on the DTC measurement of the previous cycle. The A_ADJ and B_ADJ registers in DTCMONITOR are signed accumulators; the default value is 0.

Based on the DTC measured, in the next cycle:

A_ADJ = A_ADJ + A_Δ

B_ADJ = B_ADJ + B_Δ

In each cycle, the A_ADJ and B_ADJ accumulator values are added to the original filter-controlled turn-off edges, to dynamically adjust the dead time. The Δ value changes when the measured body-diode conduction time value changes. A_ADJ and B_ADJ are updated every cycle if in automatic control mode. A_ADJ and B_ADJ are updated only once if in manual control mode.

4.2 I/O Mux

UCD3138A can accept body-diode conduction input (output from the UCD7138 DTC pin) on different I/O pins as shown in Figure 2. This function can be configured through the IOMUX register in Loop Mux. The bit fields are DTC_B_SEL and DTC_A_SEL.

Bit 13: DTC_B_SEL – DTC Phase-B Pin Mux Select

0 = DTC Phase-B input from TDO pin

1 = DTC Phase-B input from SYNC pin

Bit 12: DTC_A_SEL – DTC Phase-A Pin Mux Select

0 = DTC Phase-A input from TDI pin

1 = DTC Phase-A input from TCK pin

4.3 DTC DPWM Mux

Two different DPWM outputs can be controlled by DTC interface independently, Phase A and Phase B. Phase A and Phase B can be selected from different DPWM outputs by configuring PWM_A_SEL and PWM_B_SEL in the DTCCTRL register.

4.4 Single Input or Dual Input Mode

The two phases of the SRs can be controlled symmetrically or unsymmetrically. When controlled symmetrically, the DTC interface only looks at the DTC input on DTC0 pin, and both turn-off edges are adjusted by the same amount in each cycle. When controlled unsymmetrically, the DTC interface looks at both the DTC0 and DTC1 input, and adjusts the Phase A and Phase B DPWM turn-off edge independently. The input mode is configured by the INPUT_MODE bit in the DTCCTRL register.

4.5 Enable DTC Control in DPWM Module

In the DPWMCTRL2 register, the DTC_MODE bit and DTC_EN bit should be configured. If dual input mode is used, set DTC_MODE to 2 (both DTC phase adjust A and B are utilized in the edge adjustments).

Bit 19-18: DTC_MODE – DTC Mode Select

00 = Only DTC phase adjust A is utilized in edge adjustments (default)

01 = Only DTC phase adjust B is utilized in edge adjustments

10 = Both DTC phase adjust A and B are utilized in edge adjustments

11 = Reserved

Bit 17: DTC_EN – Enables dead time compensation mode

0 = Disabled (default)

1 = Enabled

4.6 DTC Polarity

The internal 4-ns DTC timer capture can be configured to be either active low or active high. The A_POL and B_POL in the DTCCTRL register configure the detection polarity of Phase A and Phase B.

4.7 Detection Window and Blanking

The SR body-diode conduction only happens when the MOSFET is turned off, so the body-diode detection window is generated right after the following edge of the SR DPWMs. The DETECT_BLANK and DETECT_LEN registers define the blanking time and detection window length, respectively.

4.8 Manual or Automatic Control

As shown in Figure 9, when the DTC interface is in automatic control mode, the SR turn-off edge is moved backward or forward by one HFO clock at a time. Meanwhile, firmware can overwrite the accumulator values by writing to the DTCMANUAL register. The manual or automatic control selection is made by the bit MODE in the DTCCTRL register.

4.9 Accumulator Clamps

The A_ADJ and B_ADJ are turn-off edge offset accumulators. They set the offsets of the SR turn-off edges from the original calculated value. To ensure sufficient dead time or shoot-through condition, the accumulator clamps ADJ_MIN and ADJ_MAX can be set to limit the minimum and maximum accumulator values.

4.10 Consecutive Fault Counter and Interrupt

When the measured A_CNT or B_CNT is less than the FLT_THRESH, it is considered as a fault. When there are a certain number of consecutive detected faults, a pre-programmed fault step is utilized. The number of consecutive faults is defined by the FLT_MAX register; the fault step size is defined by the FLT_STEP register.

5 Code Example

5.1 DTC Module Initialization

The following code example configures the DTC module in automatic control mode for an LLC converter.

```
//Advandanced Dead Time Compensation (DTC) module initialization (Automatic mode)
void init_DTC(void)
{
    //Enable DTC interrupt
    LoopMuxRegs.DTCCTRL.bit.FLT_INT_EN = 1;
    //Set the number of consecutive detected faults before a fault step utilized
    LoopMuxRegs.DTCCTRL.bit.FLT_MAX_CNT = 3;
    //Set the fault step size to be -75*4ns
    LoopMuxRegs.DTCCTRL.bit.FLT_STEP = 5;
    //Set the fault threshold to be 3*4ns
    LoopMuxRegs.DTCCTRL.bit.FLT_THRESH = 3;
    //Select DPWM1A to be controlled by DTC Phase A
    LoopMuxRegs.DTCCTRL.bit.PWM_A_SEL = 2;
    //Select DPWM1B to be controlled by DTC Phase B
    LoopMuxRegs.DTCCTRL.bit.PWM_B_SEL = 6;
    //Set the signal polarity of DTC pin to be active low
    LoopMuxRegs.DTCCTRL.bit.A_POL = 0;
    LoopMuxRegs.DTCCTRL.bit.B_POL = 0;
    //Phase A and Phase B operates on separate inputs
    LoopMuxRegs.DTCCTRL.bit.INPUT_MODE = 0;
    //Automatic control mode
    LoopMuxRegs.DTCCTRL.bit.MODE = 0;
    //Enable DTC module
    LoopMuxRegs.DTCCTRL.bit.DTC_EN = 1;

    //Set body diode conduction time detection window blanking time
    LoopMuxRegs.DTCTARGET.bit.DETECT_BLANK = 30;
    //Set body diode conduction time detection window length
    LoopMuxRegs.DTCTARGET.bit.DETECT_LEN = 120;
    //Set DTC control target offset. Target offset + target low = target high
    LoopMuxRegs.DTCTARGET.bit.TARGET_OFFSET = 2;
    //Set DTC control target low
    LoopMuxRegs.DTCTARGET.bit.TARGET_LOW = 15;

    //Set maximum accumulator clamp
    LoopMuxRegs.DTCLIMIT.bit.ADJ_MAX = 50;
    //Set minimum accumulator clamp
    LoopMuxRegs.DTCLIMIT.bit.ADJ_MIN = -400;

    //Initialize IOMUX
    //DTC Phase A input from TDI pin
    MiscAnalogRegs.IOMUX.bit.DTC_A_SEL = 0;
    //DTC Phase B input from TDO pin
    MiscAnalogRegs.IOMUX.bit.DTC_B_SEL = 0;

    //Initialize DTC registers in DPWM module
    //Both DTC phase adjust A and B are utilized in edge adjustments
    Dpwm1Regs.DPWMCTRL2.bit.DTC_MODE = 2;
    //Enable DTC in DPWM module
    Dpwm1Regs.DPWMCTRL2.bit.DTC_EN = 1;
}
```

5.2 DTC Interrupt

The DTC interrupt number is 19, and defined by the macro CIMINT_ALL_DTC.

```
disable_interrupt();
    disable_fast_interrupt();
    //Configure IRQ and FIQ
    write_reqmask(CIMINT_ALL_DTC);
    write_firqpr(CIMINT_ALL_DTC);
    //Enable interrupts
    enable_fast_interrupt();
    enable_interrupt();
```

The DTC interrupt is only tripped if a certain number of consecutive faults are detected. The DTCSTAT register has a FLAG bit to indicate each fault condition. If the FLAG bit is 1, it indicates a fault condition.

5.3 Manual Control Mode

If manual control mode is used during initialization, the MODE bit in the DTCCTRL register should be set.

```
//Manual control mode
    LoopMuxRegs.DTCCTRL.bit.MODE = 1;
```

The DTC manual adjust function reads the DTC counter value, then adjusts the accumulator value:

```
//DTC variable definitions
Uint16 DTC_A_count;
Uint16 DTC_B_count;
int32 accumulator_A;
int32 accumulator_B;

//DTC manual control
void DTC_manual_adj(void)
{
    //Read DTC counter values
    DTC_A_count = LoopMuxRegs.DTCSTAT.bit.A_CNT;
    DTC_B_count = LoopMuxRegs.DTCSTAT.bit.B_CNT;
    //Read accumulator values
    accumulator_A = LoopMuxRegs.DTCMONITOR.bit.A_ADJ;
    accumulator_B = LoopMuxRegs.DTCMONITOR.bit.B_ADJ;

    //Adjust Phase A
    if((DTC_A_count > 15)&&(accumulator_A < 511))
        LoopMuxRegs.DTCMANUAL.bit.A_ADJ = accumulator_A + 1;
    else if ((DTC_A_count < 13)&&(accumulator_A -512))
        LoopMuxRegs.DTCMANUAL.bit.A_ADJ = accumulator_A - 1;

    //Adjust Phase B
    if((DTC_B_count > 15)&&(accumulator_B < 511))
        LoopMuxRegs.DTCMANUAL.bit.B_ADJ = accumulator_B + 1;
    else if ((DTC_B_count < 13)&&(accumulator_B > -512))
        LoopMuxRegs.DTCMANUAL.bit.B_ADJ = accumulator_B - 1;
}
```

6 Register List

Table 3 shows the registers used for the DTC interface.

Table 3. Register List

Address	Register Name	Description	Bits	Type	Reset
0x0002_0078	DTCCTRL	DTC Control Register	21	R/W	0x0
0x0002_007C	DTCTARGET	DTC Target Register	24	R/W	0x0
0x0002_0080	DTCLIMIT	DTC Automatic Limit Register	20	R/W	0xE001FF
0x0002_0084	DTCMANUAL	DTC Manual Control Register	20	R/W	0x0
0x0002_0088	DTCMONITOR	DTC Monitor Register	20	R	0x0
0x0002_008C	DTCSTATUS	DTC Status Register	15	R	N/A

6.1 DTC Control (DTCCTRL)

Figure 14. DTC Control (DTCCTRL) Register

	22	21	20	19	18	17	16
	FLT_INT_EN	FLT_MAX		FLT_STEP			FLT_THRESH
	R/W	R/W		R/W			R/W
15	14	13	12	11	10	9	8
FLT_THRESH			PWM_A_SEL				PWM_B_SEL
R/W			R/W				R/W
7	6	5	4	3	2	1	0
PWM_B_SEL			A_POL	B_POL	INPUT_ MODE	MODE	DTC_EN
R/W			R/W	R/W	R/W	R/W	R/W

Address 00120078

Table 4. DTC Control (DTCCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
22	FLT_INT_EN	R/W	0	Enables interrupt generation when a fault flag condition has been met 0 = Interrupt disabled (default) 1 = Interrupt enabled
21-20	FLT_MAX	R/W	0	Sets the number of consecutive detected faults before a fault step is utilized 0 = 1 (default) 1 = 2 2 = 4 3 = 8

Table 4. DTC Control (DTCCTRL) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-17	FLT_STEP	R/W	0	Sets the negative step size when a fault condition is detected that exceeds the fault max value. If the fault_max condition has not been met the step size is -1. Step size is HFO clock increments. 0 = –1 (default) 1 = –5 2 = –10 3 = –25 4 = –50 5 = –75 6 = –100 7 = –125
16-13	FLT_THRESH	R/W	0	Sets the measurement threshold for a fault condition to initiate a fault step.
12-9	PWM_A_SEL	R/W	0	Selects the phase A negative edge reference to begin a measurement window 0 = Disabled (Default) 1 = DPWM-0-A 2 = DPWM-1-A 3 = DPWM-2-A 4 = DPWM-3-A 5 = DPWM-0-B 6 = DPWM-1-B 7 = DPWM-2-B 8 = DPWM-3-B
8-5	PWM_B_SEL	R/W	0	Selects the phase B negative edge reference to begin a measurement window 0 = Disabled (Default) 1 = DPWM-0-A 2 = DPWM-1-A 3 = DPWM-2-A 4 = DPWM-3-A 5 = DPWM-0-B 6 = DPWM-1-B 7 = DPWM-2-B 8 = DPWM-3-B
4	A_POL	R/W	0	Sets the signal polarity of the DTC input to the device 0 = Active Low (Default) 1 = Active High
3	B_POL	R/W	0	Sets the signal polarity of the DTC input to the device 0 = Active Low (Default) 1 = Active High
2	INPUT_ MODE	R/W	0	Sets the input method for the DTC module 0 = Phase A and Phase B input signals occur on separate inputs 1 = Phase A and Phase B input signals occur on the same input
1	MODE	R/W	0	Sets mode control of the DTC phase accumulator values 0 = Automatic Mode. Accumulators A and B are changed by hardware and stay within limits programmed in the DTCLIMIT register. (Default) 1 = Manual Mode. Accumulator A and B set by programmed values in the DTCMANUAL register.
0	DTC_EN	R/W	0	DTC Enable 0 = Dead-time Compensate Module disabled (Default) 1 = Dead-time Compensate Module enabled

6.2 DTC Target (DTCTARGET)

Figure 15. DTC Target (DTCTARGET) Register

23 17	16 9	8 7	6 0
DETECT_BLANK	DETECT_LEN	TARGET_OFFSET	TARGET_LOW
R/W	R/W	R/W	R/W

Address 0012007C

Table 5. DTC Target (DTCTARGET) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-17	DETECT_BLANK	R/W	0	Sets the target measurement window blanking length, in HFO clock increments.
16-9	DETECT_LEN	R/W	0	Sets the target measurement window length, in HFO clock increments.
8-7	TARGET_OFFSET	R/W	0	Target Threshold Offset. Target upper threshold = target low + target offset 0 = 0 (default) 1 = 2 HFO clocks 2 = 4 HFO clocks 3 = 8 HFO clocks
6-0	TARGET_LOW	R/W	0	Target Lower Threshold, in HFO clock increments

6.3 DTC Auto Control Limit (DTCLIMIT)

Figure 16. DTC Auto Control Limit (DTCLIMIT) Register

19 10	9 0
ADJ_MAX	ADJ_MIN
R/W	R/W

Address 00120080

Table 6. DTC Auto Control Limit (DTCLIMIT) Register Field Descriptions

Bit	Field	Type	Reset	Description
19-10	ADJ_MAX	R/W	01_1111_1111	Sets the signed integer upper clamp for the accumulators. The integer range is (-512 to 511)
9-0	ADJ_MIN	R/W	10_0000_0000	Sets the signed integer lower clamp for the accumulators. The integer range is (-512 to 511)

6.4 DTC Manual Control (DTCMANUAL)

Figure 17. DTC Manual Control (DTCMANUAL) Register

19	10	9	0
A_ADJ		B_ADJ	
R/W		R/W	

Address 00120084

Table 7. DTC Manual Control (DTCMANUAL) Register Field Descriptions

Bit	Field	Type	Reset	Description
19-10	A_ADJ	R/W	00_0000_0000	Sets the signed A accumulator value when manual control is enabled.
9-0	B_ADJ	R/W	00_0000_0000	Sets the signed B accumulator value when manual control is enabled.

Register is ignored in automatic mode.

6.5 DTC Monitor (DTCMONITOR)

Figure 18. DTC Monitor (DTCMONITOR) Register

19	10	9	0
A_ADJ		B_ADJ	
R		R	

Address 00120088

Table 8. DTC Monitor (DTCMONITOR) Register Field Descriptions

Bit	Field	Type	Reset	Description
19-10	A_ADJ	R	0_0000_0000	Monitored accumulator A value from the DTC module
9-0	B_ADJ	R	0_0000_0000	Monitored accumulator B value from the DTC module

6.6 DTC Status (DTCSTAT)

Figure 19. DTC Status (DTCSTAT) Register

14	8	7	1	0
A_CNT		B_CNT		FLAG
R		R		

Address 0012008C

Table 9. DTC Status (DTCSTAT) Register Field Descriptions

Bit	Field	Type	Reset	Description
14-8	A_CNT	R	000_0000	Last measurement value for phase A input signal
7-1	B_CNT	R	000_0000	Last measurement value for phase B input signal
0	FLAG	R	0	Flag is set when the fault count exceeds the FLT MAX value programmed in the DTCCTRL register.

Revision History

Changes from A Revision (June 2015) to B Revision	Page
• Updated Timing Diagram of the DTC Interface.	12

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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