UCD3138 Family: Practical Design Guideline

Application Report

Literature Number: SLUA779B

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Introduction

Sean Xu

There are multiple grounds and bias power pins for a digital controller, such as the UCD3138 family products. They are separated from each other because of the digital circuitry and analog circuitry inside the device. Normally, digital circuit draws more current and generates more noise, but the digital signal is not sensitive to the noise; while the analog circuit needs a quiet power and grounding. A deliberate grounding and power separation outside the controller can reduce the interference between analog circuit and digital circuit, and therefore, the controller can have better performance. When they are separated from each other, take care of how the analog circuit and digital circuit are grouped, respectively, and then how and where they are tied together. With improper grounding, the device performance can be negatively impacted including DPWM abnormal, device reset, ADC results, output voltage ripple, and so on.

This document supersedes all older guidelines on UCD family board design and layout. Older EVM designs may not meet all of these guidelines.

In the PCB design, there are two options. One is to have two separate grounds - digital ground and analog ground. The other is to use a single ground plane for both digital ground and analog ground. With two separate ground planes, how to connect digital ground and analog ground is very important, and the PCB must be designed very carefully. With a single ground plane, there is no concern regarding where two grounds are tied together, and it makes the PCB design easier. Here, TI recommends using a single ground plane.

In this document, digital ground is denoted as DGND; analog ground is denoted as AGND; a single ground plane is denoted as SGND. This document covers the UCD3138 family including non-A version UCD family, for example, UCD3138, UCD3138064, and UCD3138128; and A version-UCD family, for example, UCD3138A, UCD3138064A, and UCD3138128A.

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UCD3138 Pin Connection Recommendation

The UCD3138 device is a highly integrated controller with a large number of mixed signals. It is important to group each pin, select good components, have appropriate connections to each pin, and make good component placement on the PCB to reduce noise coupling and to prevent chip mal-function. First, group all digital circuitry and analog circuitry. Second, place digital circuitry close to each other, place analog circuitry close to each other, and then make connections among them by a solid plane(SGND). To achieve a robust design, TI recommends at least a 4-layer board.

Next, layout considerations and examples are provided for some critical pins or signals.

2.1 $\overline{\text{RESET}}$ Pin

The $\overline{\text{RESET}}$ pin must have one at least 2.2 µF low ESL capacitor locally decoupled with SGND plane. As shown in Figure 2-1, this capacitor must be placed very close to the device $\overline{\text{RESET}}$ pin. TI highly recommends using a small resistance (such as 2.2 kΩ) to connect the $\overline{\text{RESET}}$ pin (pin 11 for UCD3138RGC) with V33DIO (pin 9 for UCD3138RGC). The resistor must be placed close to the $\overline{\text{RESET}}$ pin, as well. The grounding point of the capacitor must be tied to SGND plane locally by a ground via, which is generally larger than a signal via.

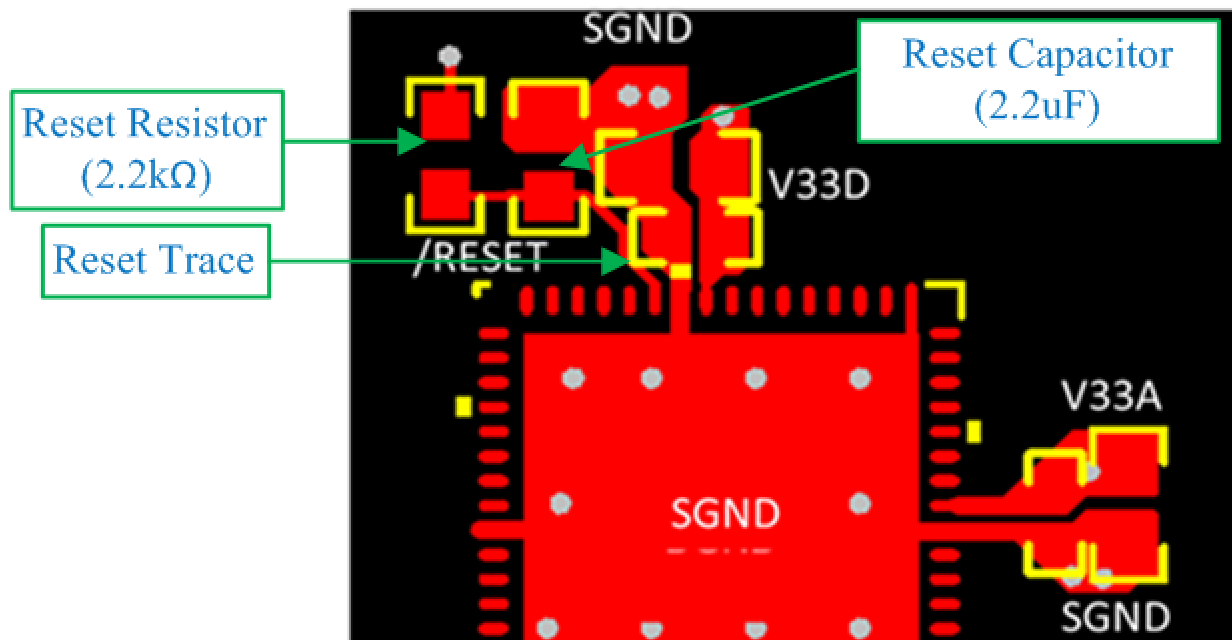

Figure 2-1. $\overline{\text{RESET}}$ Pin Connection

2.2 ADC Pins

Use low ESL and ESR ceramic capacitors on ADC pins to decouple with SGND. The capacitor value is selected such that the cut-off frequency is at least one tenth the sampling frequency if there is no dynamic requirement. This can help reduce noise coupled during signal transmission.

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ADC input is a single-ended signal. If the sensing trace is long, move it away from radiation sources and add ground shielding between the signal and radiation sources. If there exists a resistor between signal output and ADC input, the resistor should be located close to the ADC pin. The resistance needs to be less than 1 kΩ.

For example, the sampling frequency is 10 kHz. The cut off frequency of LPF is 1 kHz. With a 1-kΩ equivalent resistor, select a 0.15-µF capacitor.

2.3 EAP and EAN Pins

There are three front-end ADCs to sense the feedback signals in the UCD family. These ADCs are dual-ended sensing input circuitry with good common mode noise rejection. Keep the distance between the two traces as short as possible when the differential sensing method is used. A local filter close to the EAP and EAN pins is required as shown in Figure 2-2. Because EAP and EAN are used for feedback loop, C must be selected from the range of 100 pF to 1000 pF. R is preferred to use low resistance.

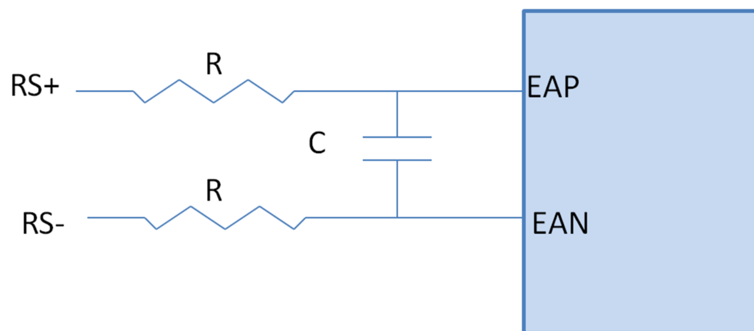

Figure 2-2. Local Filter on EAPx and EANx Pins

2.4 Current Amplifier With EADC Connection

As shown in Figure 2-3, if a current amplifier is used for current sensing, a differential input is recommended to suppress common mode noise. Then it is followed by a local low-pass filter (LPF), LPF should be placed close to the EAP and EAN pins of the UCD device. Both filters must be connected to the same ground plane (SGND).

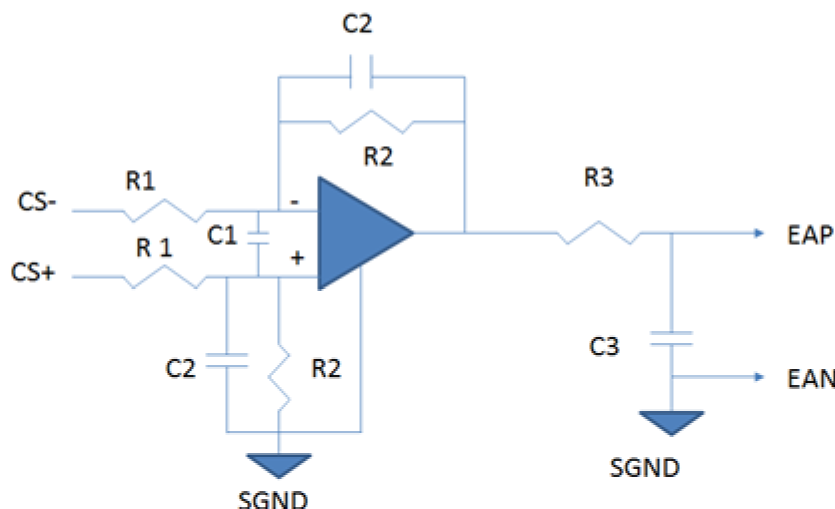

Figure 2-3. Current Amplifier Connected With EADC

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2.5 UART Communication Port

UART is used for communicating between the primary side and secondary side with isolation boundary. Normally, the communication wires are long. These wires can easily be interfered by EMI and pick up noise of switching power supplies. First, the wires must be routed without directly exposing the traces to the switching noise source, and then a termination is needed at the end of the trace, as shown in Figure 2-4. For example, R = 50 Ω, C = 47 pF if they don't significantly slow down the slew rate of the signals. When the pins are not used, tie them to the single ground plane SGND.

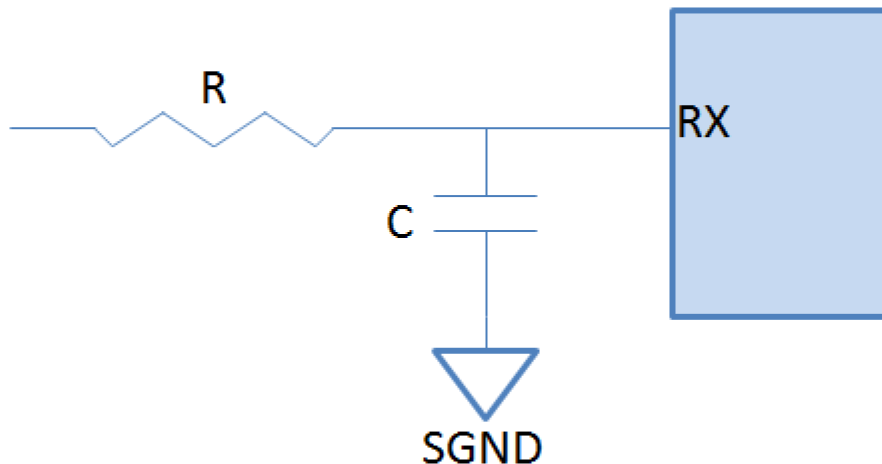

Figure 2-4. Termination for Communication Port (UART)

2.6 DPWM PINS

If DPWMs travel for a longer distance than 3 inches from the control card to a main power stage, a Schottky clamping diode may be needed as shown in Figure 2-5 to prevent electrical overstress on the device during lightning test. The long trace may also pick up the noise from other switching sources. Avoid DPWM signals to cross switching nodes.

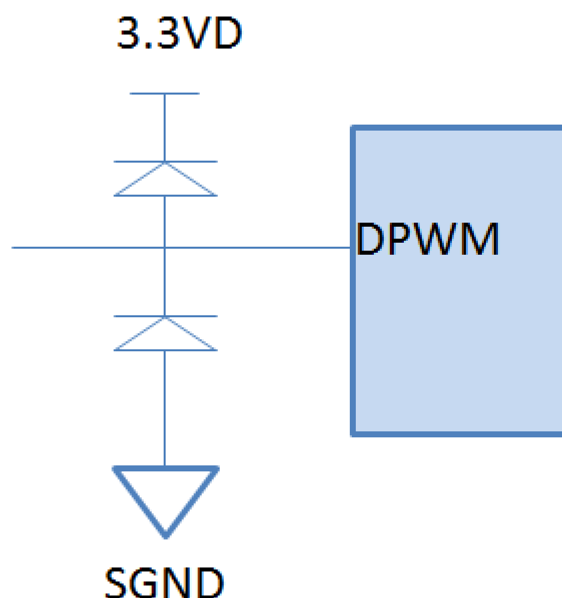

Figure 2-5. Clamping Diodes for DPWM

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2.7 GPIOS

GPIO is referenced to DGND internally. When GPIO pins are not used connect the pins to SGND. Alternatively, they can be configured as output pins and set as low in the firmware. When GPIOs are used to drive other circuit like LED, be aware that traces can pick up noise. A local resistor close to the signal receiver (like LED) is used to terminate the coupled noise. If the big voltage swings, clamping diodes are needed for GPIO inputs, as shown in Figure 2-6.

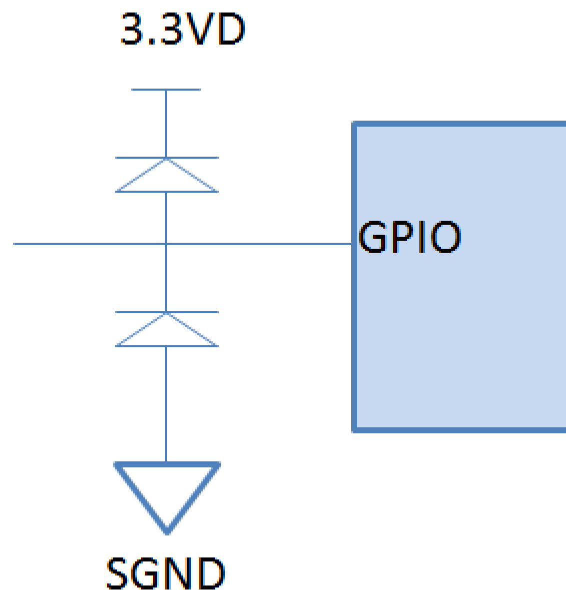

Figure 2-6. Clamping Diodes for GPIO

2.8 DPWM Synchronization

For half bridge or full-bridge converter, where more than one DPWM modules are used to drive multiple pairs of MOSFETs, synchronization between DPWM modules is required. The synchronization can be achieved by using Master-Slave mode. A slaved DPWM can be synchronized with other Master DPWM or Slave DPWM. Without synchronization, the DPWM could go out of synchronization at large currents which can cause catastrophic damage.

Please note: For UCD3138ARMH and UCD3138ARJA, if the system use case is below -30C, DPWM fixed edge alignment should be avoided and at least a 4ns gap should be configured.

2.9 External Clock

On the UCD3138128A device, if the XTAL_IN (Pin 61) and XTAL_OUT (Pin 62) are not used for an external crystal, tie each one to 1.8V (Pin BP18) through a separate 1kohm resistor.

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UCD3138 Family Bias Supply and Grounding

3.1 3.3-V Supply Pins

+3.3 V bias normally is produced by a LDO or Buck converter. +5 V (or +12 V) normally are generated by a flyback converter and it is referenced to the Power Return. A 10 µF capacitor is locally used for LDO or buck between +3.3 V and Power RTN node. From there, use a single plane (SGND) for both digital ground and analog ground. A 1Ω resistor is needed between V33D and V33A. V33D and V33DIO should be shorted externally if they are available and have a wider trace or preferably through its own power plane to connect them. As an example, a 4.7-µF decoupling capacitor is used for V33A and V33D respectively and these decoupling capacitors should be placed close to the device pins. In addition, a 10nF capacitor is used for V33A, V33D and V33DIO respectively to filter out the high frequency noise and placed as close to the pin as possible, for example the distance is less than 25mils from the capacitor to the pin V33D (or V33DIO) and from the capacitor to the pin DGND. 10 nF uses smaller package such as 0402 and low ESR capacitor. Refer to section Section 3.4. There should not be any voltage delta between the DGND pins and AGND pins. Multiple vias are required to connect the extended power pad (for example, copper plane under the device power pad) to the internal single ground (SGND) plane layer. All digital and analog ground pins are directly connected to the extended power pad and connected to the internal SGND plane through vias.

3.2 BP18 Pin

Two parallel capacitors, 1µF and 10nF, are used between BP18 and SGND. The 10nF is placed closer to the pin than 1uF. Please note that only for the UCD3138 (40-pin and 64-pin) and UCD3138064 (40-pin and 64-pin) devices, it is required to have a 2.2-µF decoupling capacitor between V33D to BP18. The 2.2-µF capacitor is required to ramp BP18 when V33D is ramping up. Place the capacitors close to the device pins, and keep the return loop as small as possible.

3.3 Additional Bias Guidelines

- Apply multiple different capacitors for different frequency range on decoupling circuits. Each capacitor has different ESL, capacitance, ESR and different frequency response.
- Avoid long traces close to radiation components and place them into an internal layer. It is preferred to have grounding shield and add a termination circuit at the end of long traces.
- Do NOT use a ferrite bead or a resistor with a value of 3-Ω or larger resistor to connect between V33A and V33D.
- Avoid negative current/negative voltage (–0.3 V) on all pins. Avoid voltage spikes of more than 3.8V on all pins. Schottky diodes may be required to clamp the voltage on any pins that could have voltage spikes during surge tests. Note that Schottky diodes have relatively higher leakage current, which can affect the voltage sensing at high temperature.
- For UCD3138128 and UCD3138A64 80pin devices, pin 61 should be connected to BP18 through 1kΩ resistor.
- If the bias supply to the device is a switching supply, ripple should be minimized. The higher the peak-to-peak magnitude and frequency of the ripple, the more the oscillator frequency changes. section

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3.4 Schematics and Layouts

3.4.1 UCD3138 and UCD3138064 64 Pin

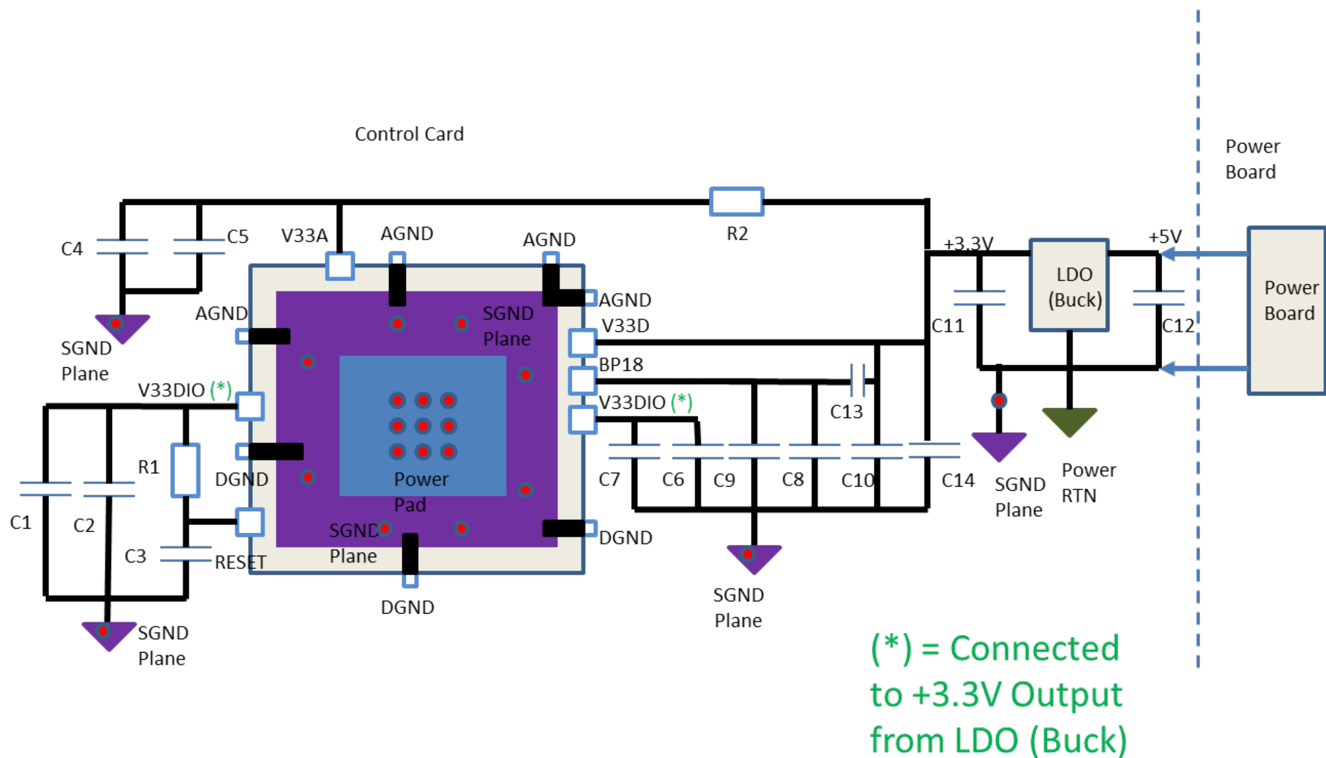

Figure 3-1. Power and Ground Schematic for UCD3138 and UCD3138064 64 Pin

Table 3-1. Power and Ground Connection Components for UCD3138 and UCD3138064 64 Pin

COMPONENT	VALUE
C1	4.7 µF
C2	10 nF
C3	2.2 µF
R1	2.2 kΩ
C4	4.7 µF
C5	10 nF
C6	4.7 µF
C7	10 nF
C8	1 µF
C9	10 nF
C10	4.7 µF
R2	1 Ω
C11	10 µF
C12	10 µF
C13	2.2 µF
C14	10 nF

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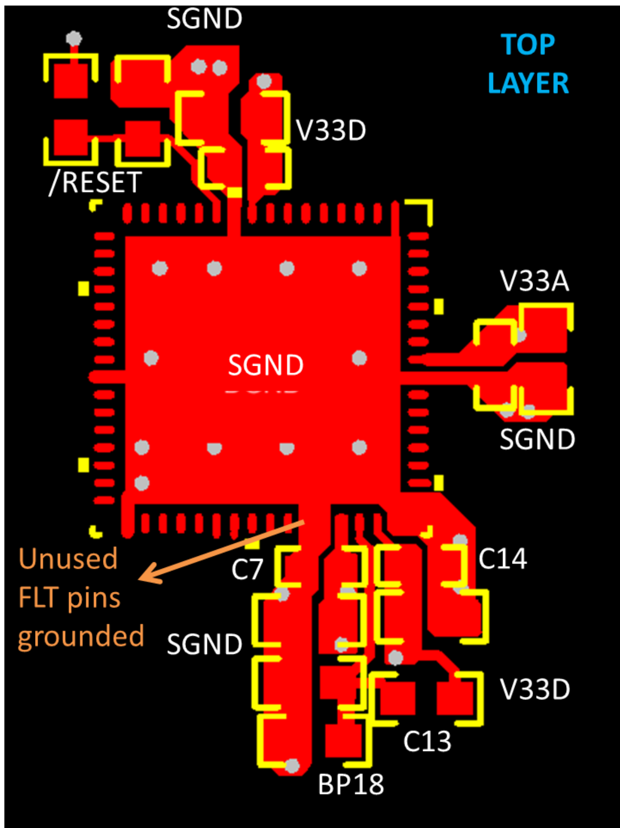

Figure 3-2. UCD3138 and UCD3138064 64 Pin Layout Top Layer

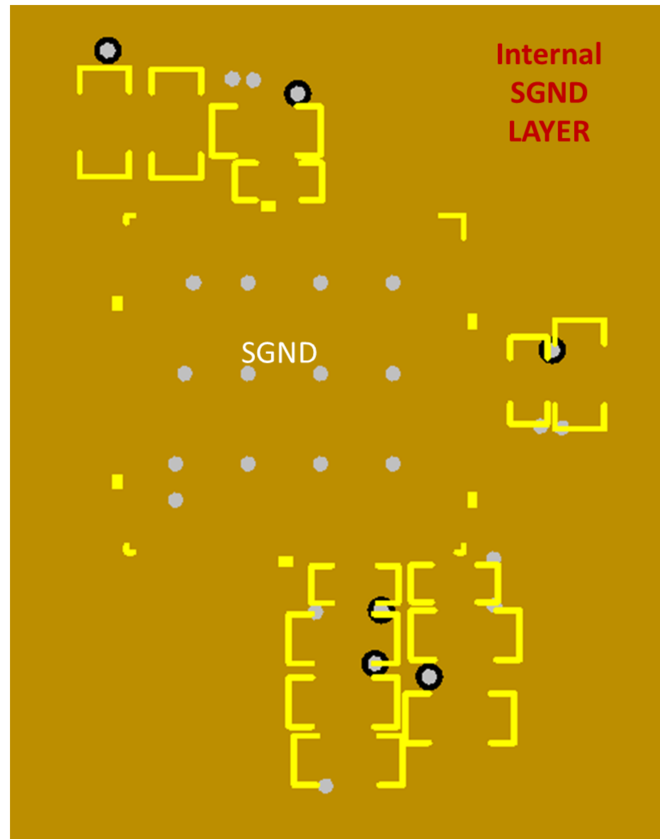

Figure 3-3. 64 Pin UCD3138 and UCD3138064 Layout Internal SGND Layer

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3.4.2 UCD3138 and UCD3138064 40 Pin

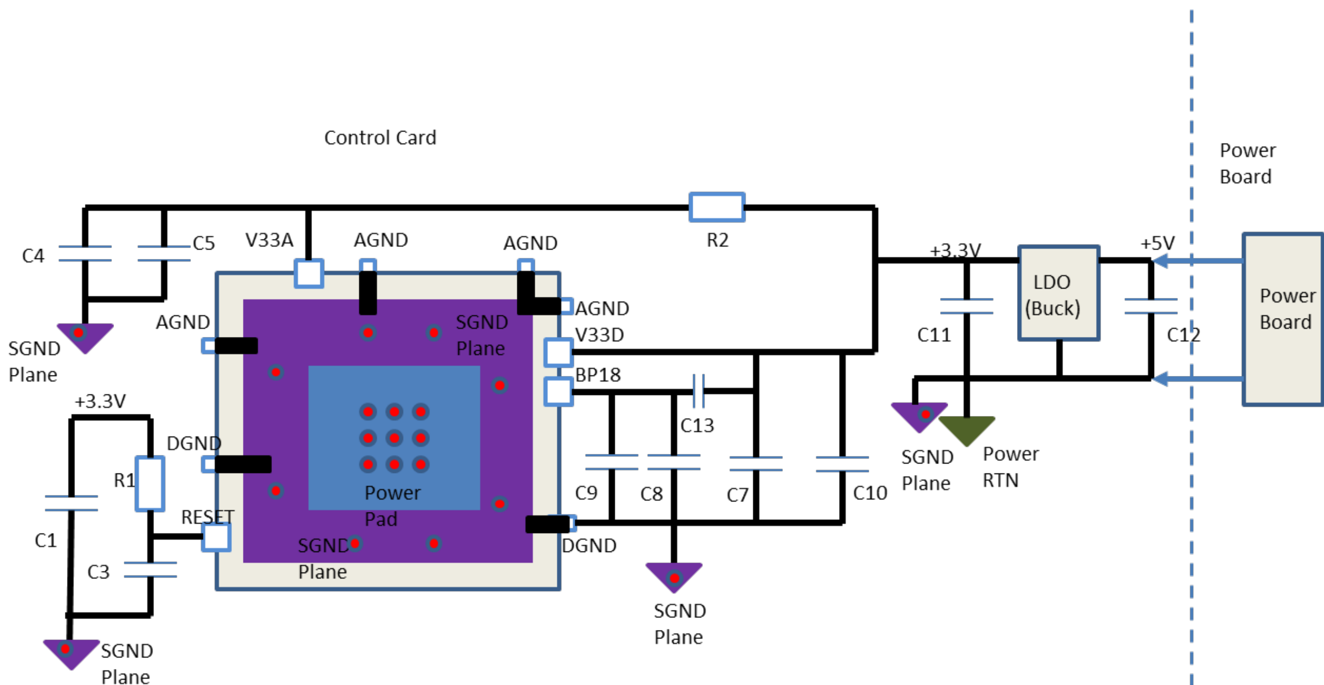

Figure 3-4. Power and Ground Schematic for UCD3138 and UCD3138064 40 Pin

Table 3-2. Power and Ground Connection Components for UCD3138 and UCD3138064 40 Pin

COMPONENT	VALUE
C1	1 µF
C3	2.2 µF
R1	2.2 kΩ
C4	4.7 µF
C5	10 nF
C7	10 nF
C8	1 µF
C9	10 nF
C10	4.7 µF
R2	1 Ω
C11	10 µF
C12	10 µF
C13	2.2 µF

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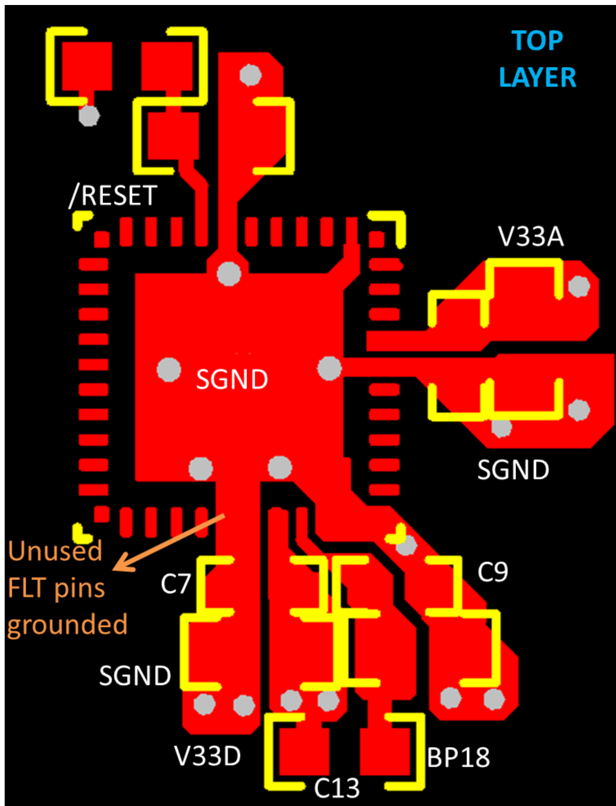

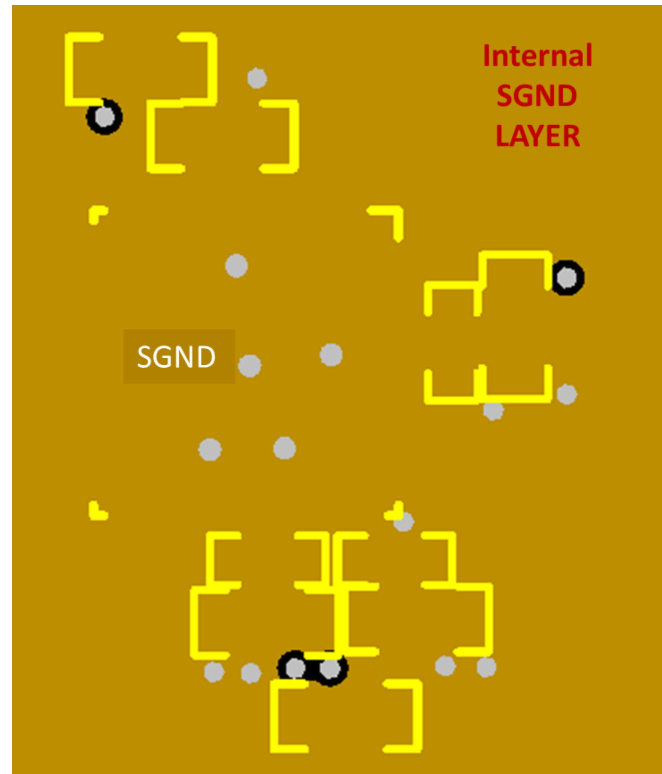

Figure 3-5. UCD3138 and UCD3138064 40 Pin Layout Top Layer

Figure 3-6. UCD3138 and UCD3138064 40 Pin Layout Internal SGND Layer

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3.4.3 UCD3138A and UCD3138064A 64 Pin

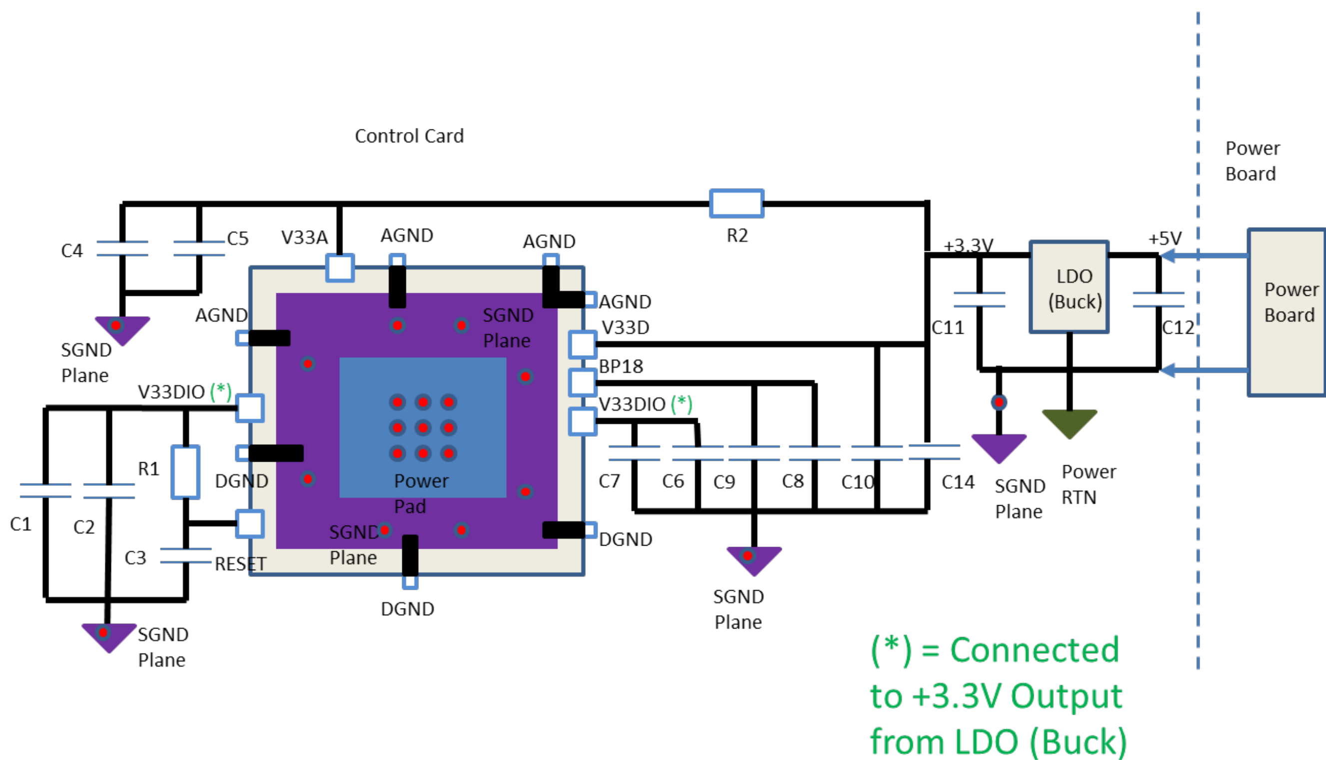

Figure 3-7. Power and Ground Schematic for UCD3138A and UCD3138064A 64 Pin

Table 3-3. Power and Ground Connection Components for UCD3138A and UCD3138064A 64 Pin

COMPONENT	VALUE
C1	4.7 µF
C2	10 nF
C3	2.2 µF
R1	2.2 kΩ
C4	4.7 µF
C5	10 nF
C6	4.7 µF
C7	10 nF
C8	1 µF
C9	10 nF
C10	4.7 µF
R2	1 Ω
C11	10 µF
C12	10 µF
C14	10 nF

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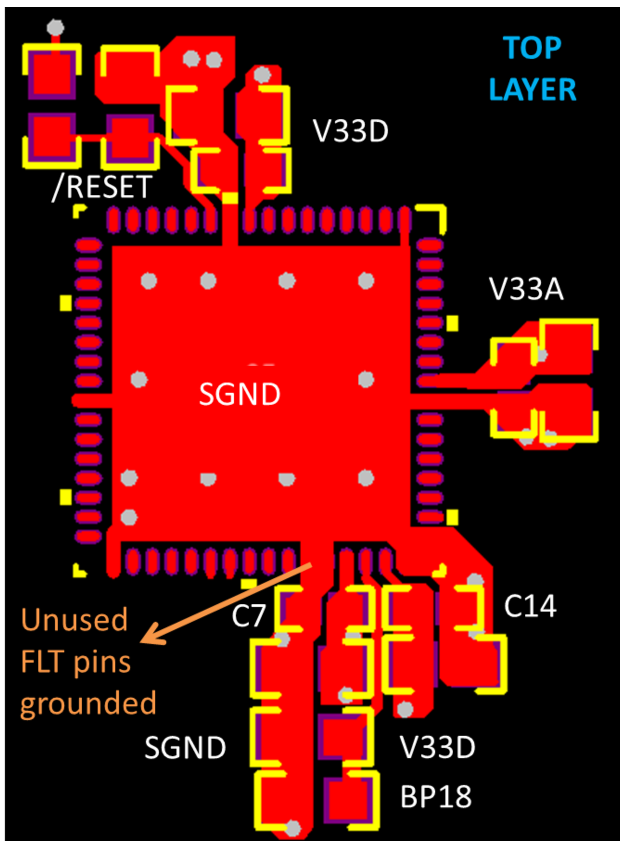

Figure 3-8. UCD3138A and UCD3138064A 64 Pin Layout Top Layer

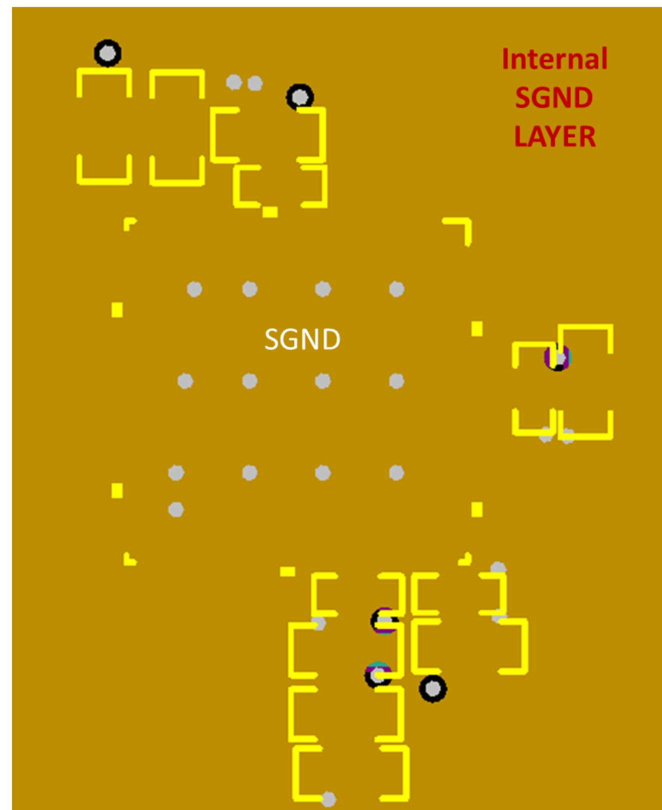

Figure 3-9. UCD3138A and UCD3138064A 64 Pin Layout Internal SGND Layer

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3.4.4 UCD3138A 40 Pin

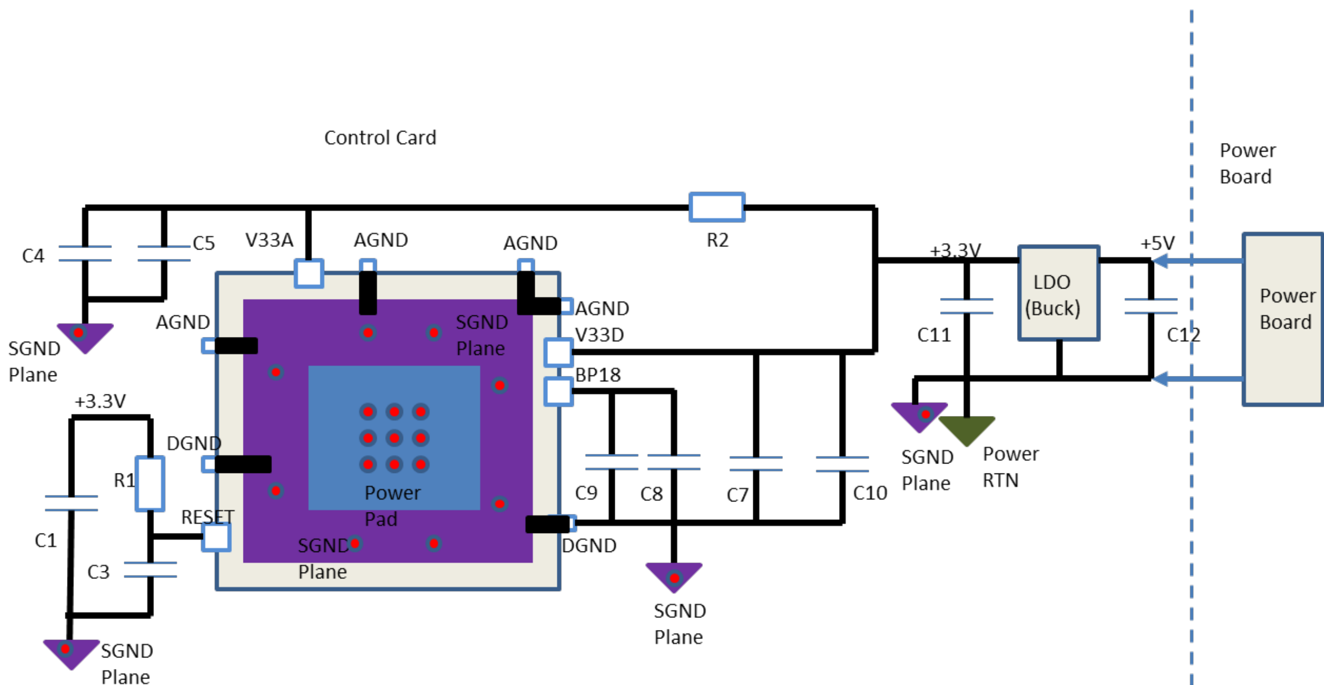

Figure 3-10. Power and Ground Schematic for UCD3138A 40 Pin

Table 3-4. Power and Ground for Connection Components UCD3138A 40 Pin

COMPONENT	VALUE
C1	1 µF
C3	2.2 µF
R1	2.2 kΩ
C4	4.7 µF
C5	10 nF
C7	10 nF
C8	1 µF
C9	10 nF
C10	4.7 µF
R2	1 Ω
C11	10 µF
C12	10 µF

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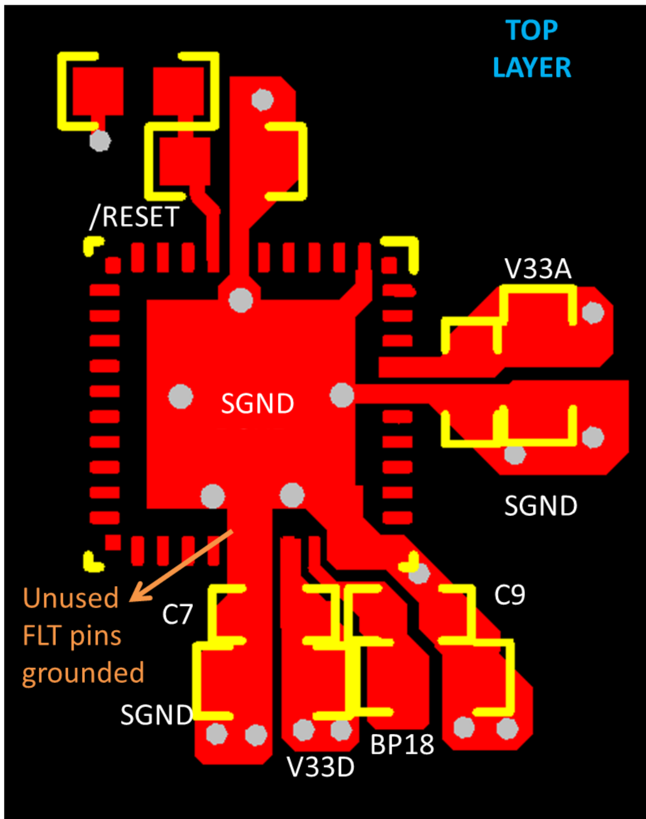

Figure 3-11. UCD3138A 40 Pin Layout Internal SGND Layer Top Layer

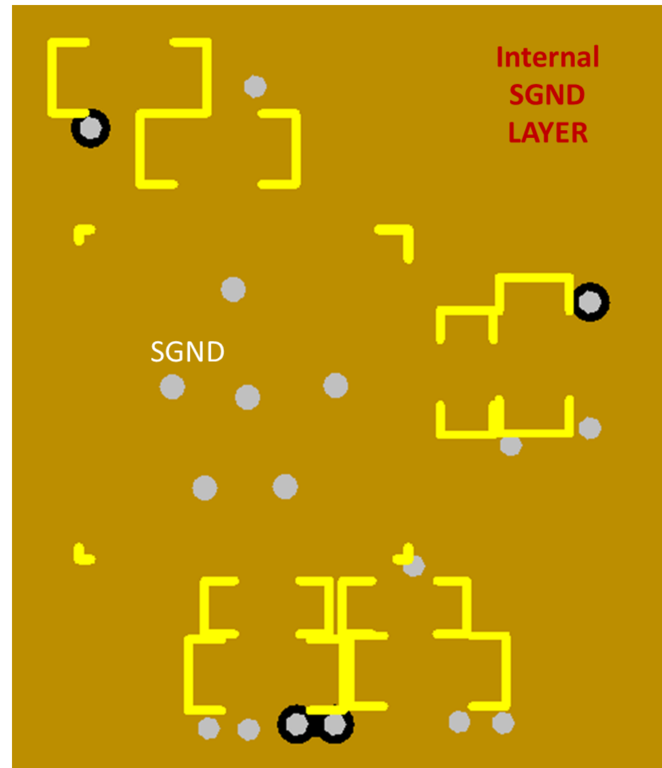

Figure 3-12. UCD3138A 40 Pin Layout Internal SGND Layer

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3.4.5 UCD3138128, UCD3138A64, UCD3138128A and UCD3138A64A 80 Pin

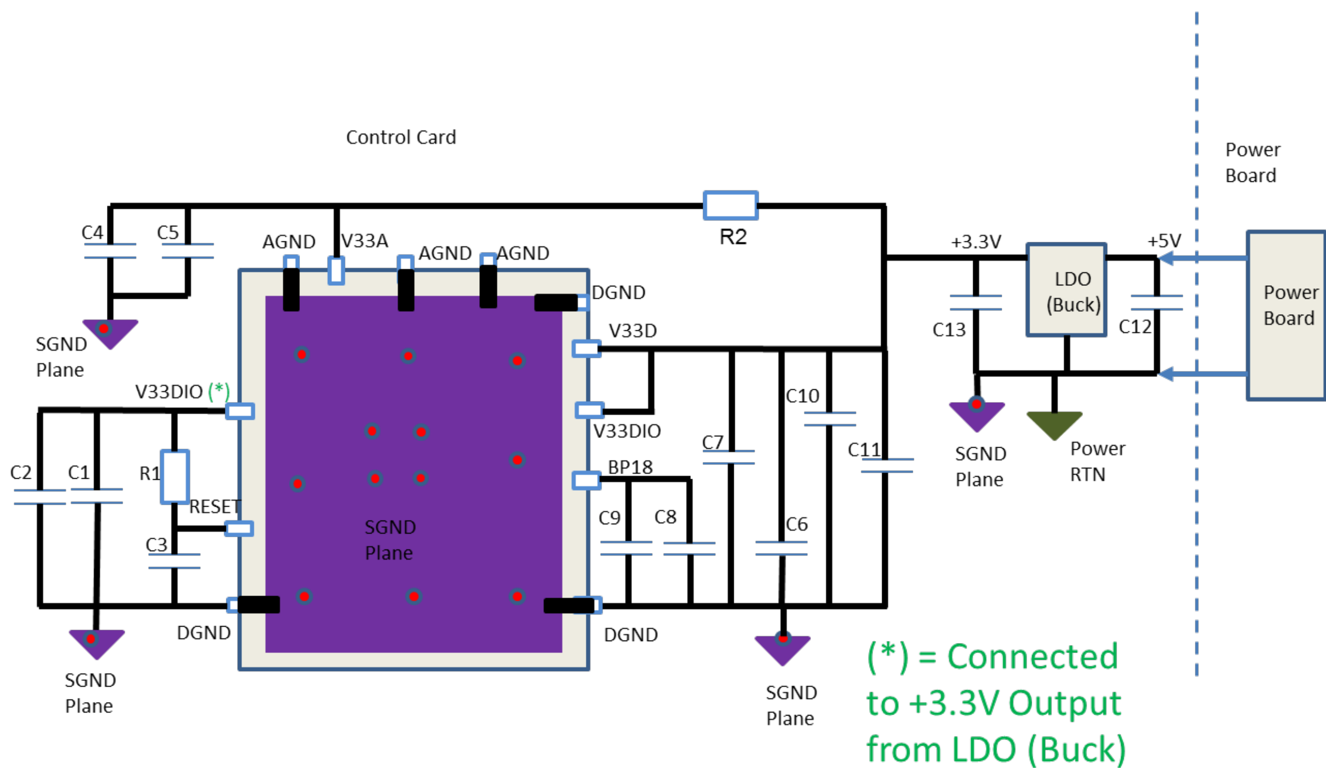

Figure 3-13. Power and Ground Schematic for UCD3138128, UCD3138A64, UCD3138128A and UCD3138A64A 80 Pin

Table 3-5. Power and Ground Connection Components for UCD3138128, UCD3138A64, UCD3138128A and UCD3138A64A

COMPONENT	VALUE
C1	10 nF
C2	4.7 µF
C3	2.2 µF
R1	2.2 kΩ
C4	4.7 µF
C5	10 nF
C6	4.7 µF
C7	10 nF
C8	1 µF
C9	10 nF
C10	4.7 µF
R2	1 Ω
C11	10 nF
C12	10 µF
C13	10 µF

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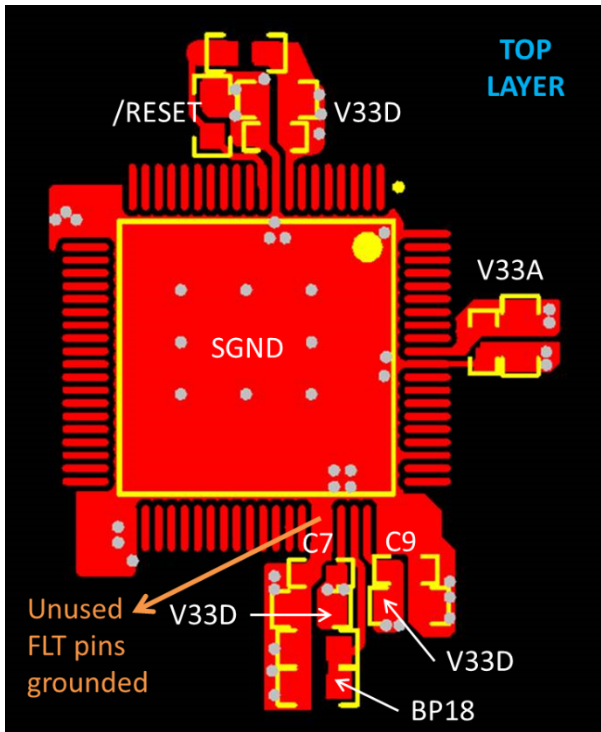

Figure 3-14. UCD3138128, UCD3138A64, UCD3138128A and UCD3138A64A 80 Pin Layout Top Layer

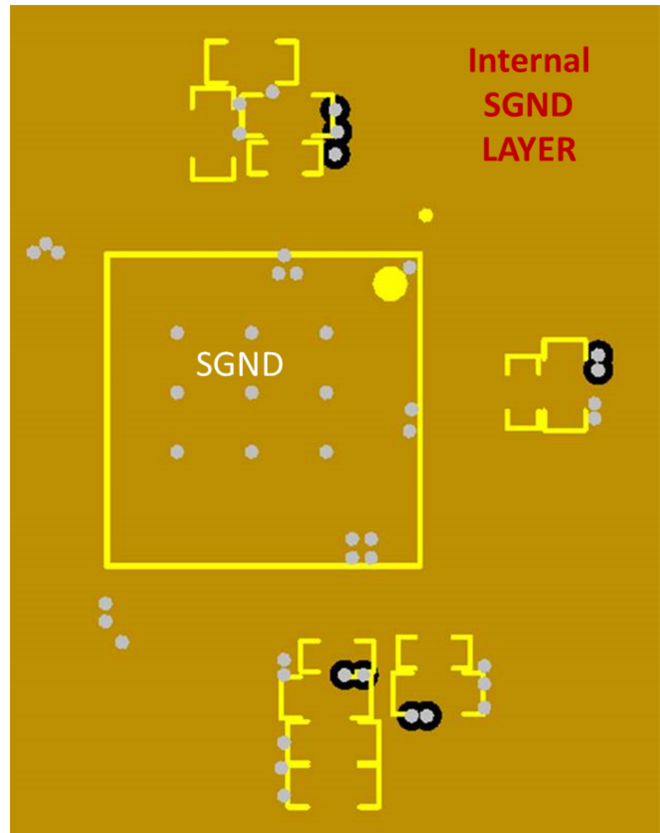

Figure 3-15. UCD3138128, UCD3138A64, UCD3138128A and UCD3138A64A 80 Pin Layout Internal SGND Layer

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Recommendation for V33 Ramp up Slew Rate and $\overline{\text{RESET}}$ Pin RC Time Constant

4.1 Recommendation for V33 Ramp up Slew Rate for UCD3138 and UCD3138064

UCD3138 and UCD3138064 need a 2.2-µF pullup capacitor from BP18 to V33 as described before. Capacitors with a value of 2.2 µF and 1 µF create a capacitor divider which pull BP18 up as V33 rises. Ensure that as V33 rises, the slew rate is not fast enough to cause BP18 to overshoot, resulting in a reliability issue. TI requires that the maximum voltage of BP18 does not exceed 1.95 V. By calculation, if V33 ramps up linearly, the maximum V33 slew rate should be less than 6 V/ms.

Also, the internal BP18 regulator is enabled when V33 is higher than V_{GH} and POR is activated. V33 charges the capacitor of BP18 through the internal regulator. This charge causes a voltage dip in the V33 pin as shown in Figure 4-1, and the charge may trigger a V33 undervoltage (POR) event, causing a chip reset. To prevent POR trigger signal oscillation and successive chip resets, TI recommends a minimum slew rate of 2.6 V/ms.

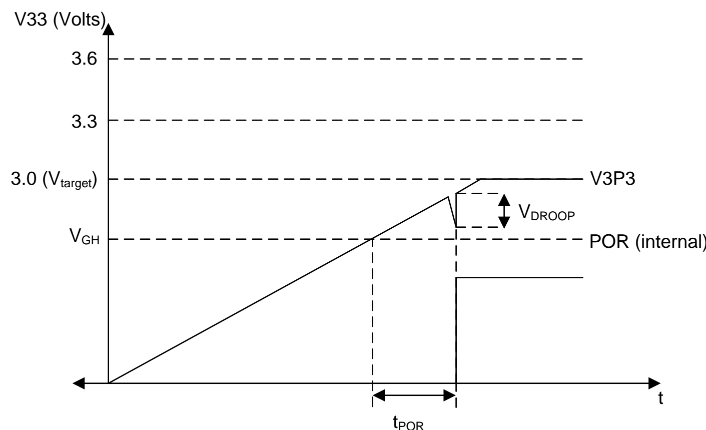

Figure 4-1. V33 Voltage Dip When POR is Activated

From the Figure 4-1 recommendations, the slew rate using the 2.2 uF/1uF capacitor combination requires that the slew rate must be as follows:

$$6\,V/ms \geq SR \geq 2.6\,V/ms \tag{1}$$

4.2 Recommendation for V33 Ramp up Slew Rate for UCD3138A, UCD3138064A, UCD3138A64, UCD3138128, UCD3138A64A, and UCD3138128A

In this group of UCD3138x, a 2.2 µF and 1 µF capacitor divider is unnecessary. Fast ramp up of V33 causes no voltage overshoot on BP18. Therefore, there is no requirement for maximum V33 slew rate.

These devices have the same minimum slew rate requirement as UCD3138 to avoid multiple chip resets given as follows:

$$SR \geq 2.6\,V/ms \tag{2}$$

If the minimum slew rate requirement cannot be met, use the $\overline{\text{RESET}}$ pin to delay the reset of the digital logic so that a clean power up is achieved. This process is described in the following sections.

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4.3 Recommendation for RC Time Constant of $\overline{RESET}$ Pin for UCD3138 and UCD3138064

Ideally, the ARM core should begin execution of ROM code only after V33>3V. The ROM code reads trim values and loads trim registers. Lack of sufficient voltage during this operation can result in unexpected device functioning. Depending on V33 slew rate, the duration for which there is insufficient voltage on V33 is varied. During this time, a reliable trim operation is not ensured. Applying an RC filter between V33 and the $\overline{RESET}$ pin can increase the delay from V33 power up to the device coming out of reset.

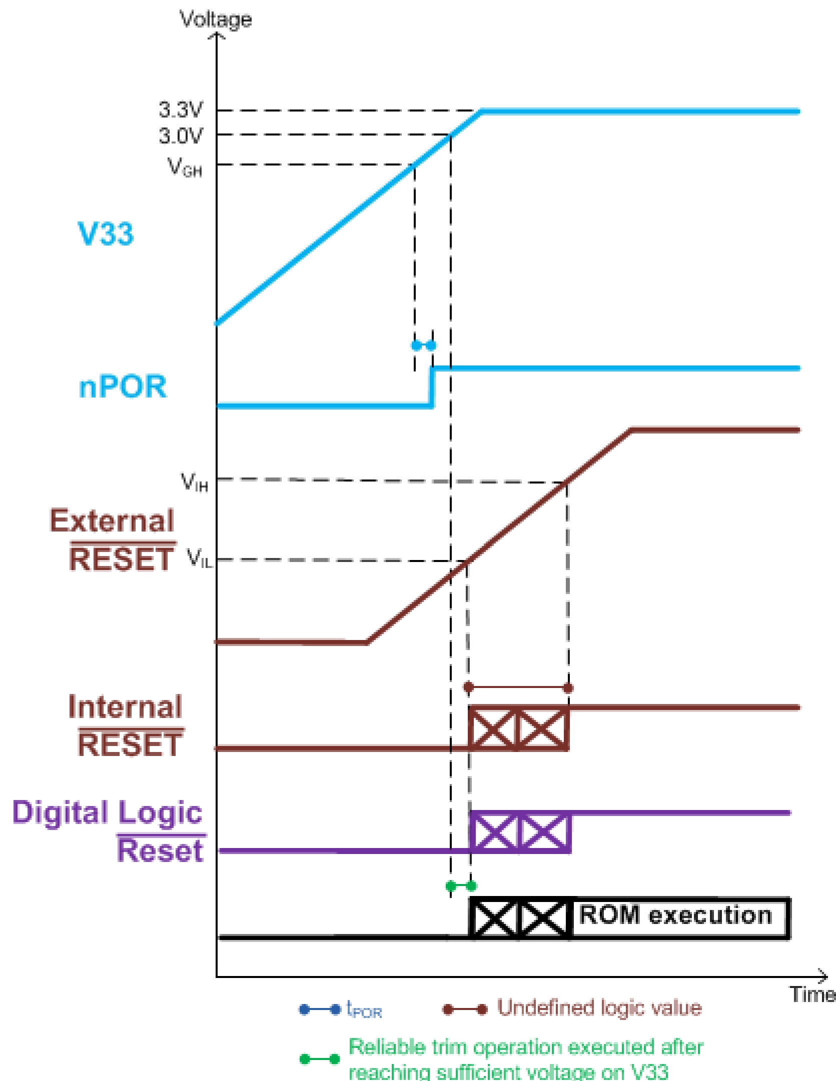

Figure 4-2. Recommended Timing Diagram of V33 and $\overline{RESET}$ for UCD3138 and UCD3138064

Example Solution:

If the V33 supply slew rate is 0.6 V/ms, then the minimum τ required is calculated as follows:

$$\tau_{RESET} = \frac{V_{target} - V_{IL}}{SR} \tag{3}$$

$$\tau_{RESET_min} = \frac{3V - 1.1\,V}{0.6\,V/ms} \approx 3.16\ ms \tag{4}$$

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If R and C are 2.21 k and 2.2 uF, then τ evaluates as:

$$\tau = R \times C \approx 2.21\,k\Omega \times 2.2\,\mu F = 4.862\,ms \tag{5}$$

These values of 2.21 kΩ and 2.2 μF will ensure that the $\overline{RESET}$ will be a logic-0 until V33 crosses 3V. [$\tau > \tau_{RESET_MIN}$]

4.4 Recommendation for RC Time Constant of $\overline{RESET}$ Pin for UCD3138A, UCD3138064A, UCD3138A64, UCD3138128, UCD3138A64A, and UCD3138128A

The timing diagram in Figure 4-3 is the recommended timing diagram of V33 and $\overline{RESET}$ for UCD3138A, UCD3138064A, UCD3138A64, UCD3138128 and UCD3138128A. The voltage on the $\overline{RESET}$ pin starts to ramp after nPOR is high.

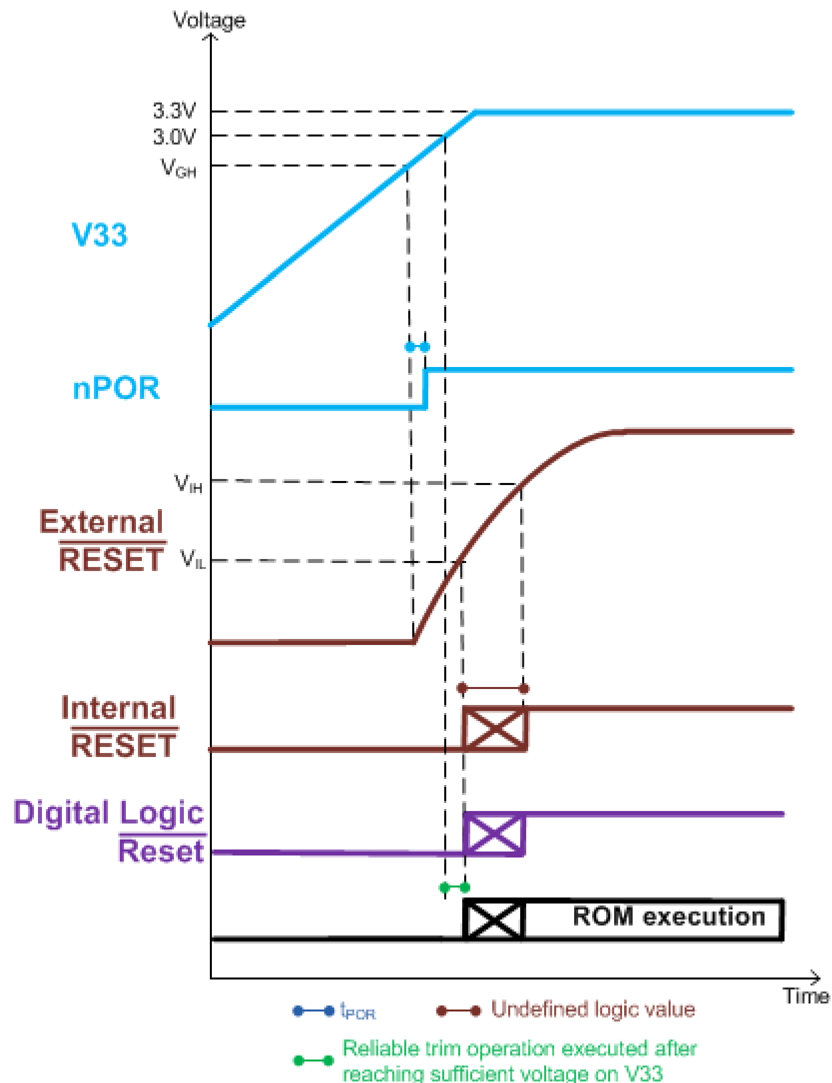

Figure 4-3. Recommended Timing Diagram of V33 and $\overline{RESET}$

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Example Solution:

If the V33 supply slew rate is 0.6 V/ms, then the minimum τ required is calculated as follows:

$$\tau_{RESET} = \frac{V_{target} - V_{POR}}{SR} \quad (6)$$

$$\tau_{RESET} \cong \frac{V_{POR} - V_{target}}{SR \times \ln\left(1 - \frac{V_{IL}}{V_{POR}}\right)} \cong \frac{1\ V}{SR} \quad (7)$$

If SR=0.6 V/ms, then:

$$\tau_{RESET_min} \cong 1.67\ ms \quad (8)$$

If R and C are 2.21 k and 2.2 uF, then τ evaluates as:

$$\tau = R \times C \approx 2.21\,k\Omega \times 2.2\ \mu F = 4.862\ ms \quad (9)$$

These values of 2.21 kΩ and 2.2 μF will ensure that the $\overline{RESET}$ pin will be a logic-0 until V33 crosses 3V. [τ > τRESET_MIN]

If the V33D does not ramp up linearly, the RC time constant is selected to ensure that the voltage of $\overline{RESET}$ is less than V_{IL} when V33D approaches 3.0 V. TI recommends to use scope to check the time sequence.

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EMI and EMC Mitigation Guideline

Every design is different in terms of EMI and EMC mitigation, and all designs require their own solution.

- Apply multiple different capacitors for different frequency range on decoupling circuits. Each capacitor has different ESL, capacitance and ESR, and different frequency responses.
- Avoid long traces close to radiation sources, and place them into an internal layer. It is preferred to have ground shielding and add a termination circuit at the end of the trace.
- TI recommends single ground: SGND. A multilayer such as 4 layers board is recommended so that one solid SGND is dedicated for return current path.
  – Use one whole layer (L2) for SGND plane as shown in Figure 5-1. Use many vias (such as 9 vias) to connect the extended power pad to the internal SGND plane layer. It is preferred to have the vias close to AGND pins and DGND pins of the device. For the 80-pin device, TI still recommneds a ground plane under the device even though there is no power pad on the device.

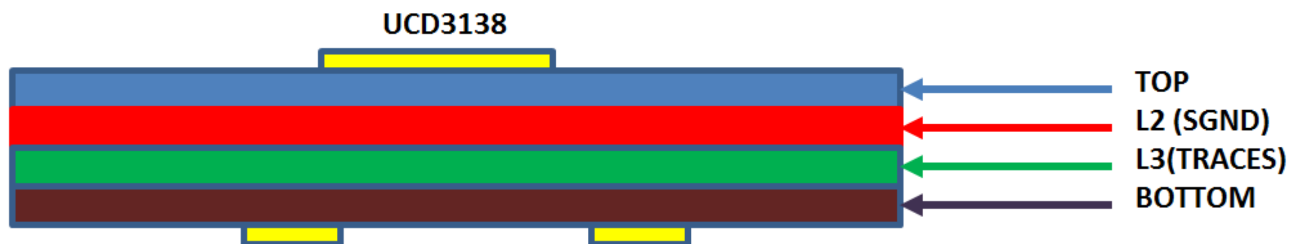

Figure 5-1. Optional Ground Layer Assignment

- Add LPF on analog signals close to the header connecting the control card and the power board.
- Do not use a ferrite bead to connect V33A and V33D instead of using 1-Ω resistor.
- Avoid negative current and negative voltage on all pins. Schottky diodes may be needed to clamp the voltage; avoid the voltage spike on all pins to exceed 3.8 V or below –0.3 V; add Schottky diodes on the pins which could have voltage spikes during surge test; be aware that Schottky diode has relatively higher leakage current, which can affect the voltage sensing at high temperatures. The need for external Schottky diodes is conditional. For example, the DPWM pins only need external Schottky diodes when there is a long distance, for example, more than 3 inches, between the control card and main power stage because in this case, the trace can pick up noise and cause electrical overstress on the device pins. The same is true for GPIO and PMBus pins.
- The auxiliary supply is normally a flyback converter, and its power transformer can generate a large electromagnetic field which can interfere with other electronic circuitry. By shielding the primary side windings, the EMI can be effectively reduced so that the surrounding circuit can have a quieter working environment.

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Special Considerations

- The first thing that must be done in any layout is to set up the basic grounding strategy and the placement of the decoupling capacitors. This needs to be prioritized over anything else, even the routing of sensitive feedback signals.
- If a gate driver device such as UCC27524 or UCC27511 is on the control card and there is a PGND connection, a net-short resistor or large copper trace must be used to tie the PGND to the Power RTN by multiple vias. Also, the net-short element between Power RTN and PGND must be close to the driver IC.
- Unused ADC pins must be tied to SGND.
- Avoid putting V33D and V33A long traces or planes close to radiation components. Place them into an internal layer. It is preferred to have ground shielding.
- Avoid putting bias supplies or SGND or Power RTN directly to across the switching power train where they can couple switching noise. If the grounds are coupled with noise, the decoupling capacitors may not be effective at filtering the noise out.
- Local capacitors are preferred to provide a short path for switching current, and be careful to select a quiet RETURN point to connect.
- In a power module or a tiny PCB design, a single solid plane without the grounding separation is shown in Figure 6-1 and has a single point connection with power RTN or SGND near the connector. Ensure there is no current flow from power train into the signal ground plane.

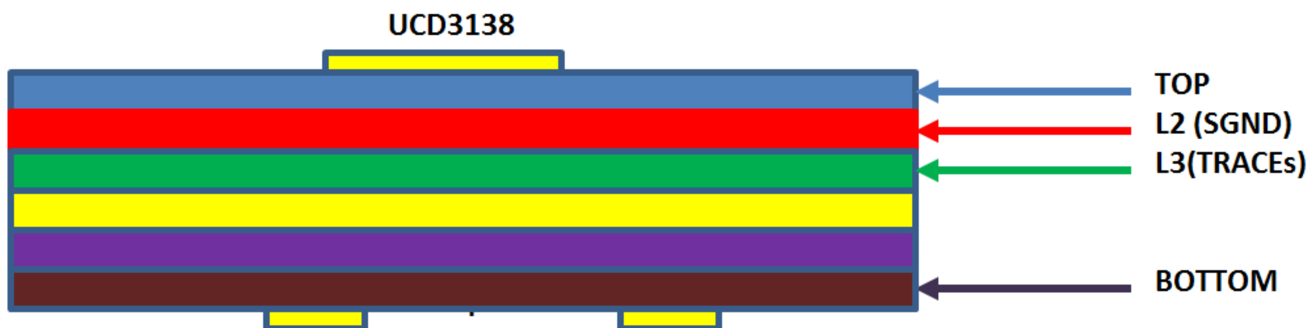

Figure 6-1. Single Ground Plane for a Power Module Design

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (January 2017) to B Revision	Page
• Remove all references to AGND or DGND planes throughout the document. Use only SGND	5
• Updated $\overline{RESET}$ pin description and Figure 2-1	6
• Updated text and figures in Section 2.4	7
• Updated and reorganized the *Chapter 3*, including the schematics and layouts	10
• Added guidelines for bias ripple to *Section 3.3*	10
• Moved SGND from level 3 to level 2 and moved traces from level 2 to level 3 in Chapters 5 and 6	25

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